Introduction: special issue on evolvable hardware challenges

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Evolvable Hardware, the application of evolutionary techniques as hardware design techniques, is still in its infancy despite a 15 year lifespan. After the initial excitement in the late 1990s there have been many successes but perhaps not at the rate or to the extent of the original expectations.

There are many challenges inherent in Evolvable Hardware, not least the identification of suitable applications. Such challenges need to be addressed so as to unlock the true potential of the field.

In putting together this special issue, it seemed timely, not only to have a special issue collecting quality papers from the field, but also to provide a collection where each contribution either addressed ongoing challenges and/or illustrated application areas where Evolvable Hardware can achieve results that are challenging for today's more traditional hardware design techniques.

This collection, although only a taste of many strong ongoing projects in the field, is thus intended to provide a clearer definition of the field together with examples of real world application areas so as to pave a future path for Evolvable Hardware.

A number of potential authors submitted abstracts based on the call for papers. However, despite a number of interesting projects, a number of potentially strong submissions were turned down at this stage so as to ensure that the special issue stayed focused on the special issue goals towards challenges and real world applications of Evolvable Hardware. Of the 12 full paper submissions received, 6 were accepted for publication and two of these accepted papers were invited contributions. All papers, including the invited contributions, were subject to the regular review and editorial standards of the journal.

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The first paper by Haddow and Tyrrell provides a critical review of the field. Despite highlighting many successes, it also considers why the field is far from reaching the expected goals identified by the earliest pioneers of the field. It further identifies many of the challenges being faced and ways in which such challenges may be addressed and/or are currently being addressed. The authors further redefine the field of Evolvable Hardware as well as a future path in terms of today's expectations.

The second paper, by Lohn, Becker and Linden is one of the invited contributions. This paper addresses a new exciting real world application area for the field, that of wireless network security. In particular, the paper applies evolutionary algorithms to adaptive beamforming, enabling wireless signals to be dynamically tracked and blocked.

The third paper, by Walker et al., is the second invited contribution. This work addresses the issue of intrinsic variability, a major issue facing the semiconductor industry. An evolutionary algorithm is applied to circuits from a standard cell library, to create solutions optimised for speed and power and with increased tolerance to random fluctuations present in both current and future technology cells.

The fourth paper, by Cawley et al., presents both the design, implementation and testing of a spiking neural network (SNN) device and associated SNN training and configuration tools. A number of challenges facing Evolvable Hardware devices for SNNs are addressed and discussed in this work including adaptive hardware, on-chip fitness evaluation (applied to the evolution of the SNN parameters) and on-line dynamic reconfiguration (supporting fault repair).

The fifth, paper by Djupdal and Haddow, explores the application of evolutionary algorithms to defect tolerance (tolerance to production faults), with respect to Field Programmable Gate Arrays (FPGAs). Defect tolerance is a major concern for the semiconductor industry. This application highlights Evolvable Hardware challenges with respect to scalability and fitness specification.

The final paper by Vasicek and Sekanina addresses the Evolvable Hardware scalability challenge in terms of the fitness evaluation time for optimisation tasks. The task is post-synthesis optimisation and the results illustrate the significant advantage of the Evolvable Hardware approach for reducing the number of gates compared to conventional tools. Further, it illustrates that the inclusion of formal verification methods in fitness evaluation provides a substantial improvement in evaluation time compared to traditional fitness measures for such tasks.

Thanks goes to all the authors who submitted their work for consideration, either as an abstract or as a full submission and to the reviewers, who through their thorough review of the work submitted ensured the high quality of this special issue. The guest editor would further like to thank Lee Spector, Editor-in-Chief, Melissa Fearon and Anitha Selvaraj, Springer for their support and professional advice during the entire process of creating this special issue.

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