

Preface of the Special Issue in Memoriam Helmut Veith

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Published online: 14 November 2017
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This special issue of the Journal on Formal Methods in System Design is dedicated to Prof. Helmut Veith, who unexpectedly passed away in March 2016. Helmut Veith was a brilliant researcher, inspiring collaborator, passionate mentor, generous friend, and valued member of the formal methods community. Helmut was not only known for his numerous and influential contributions in the field of automated verification (most prominently his work on Counterexample-Guided Abstraction Refinement [1,2]), but also for his untiring and passionate efforts for the logic community: he co-organized the Vienna Summer of Logic (an event comprising twelve conferences and numerous workshops which attracted thousands of researchers from all over the world), he initiated the Vienna Center for Logic and Algorithms (which promotes international collaboration on logic and algorithms and organizes outreach events such as the LogicLounge), and he coordinated the Doctoral Program on Logical Methods in Computer Science at TU Wien (currently educating more than 40 doctoral students) and a National Research Network on Rigorous Systems Engineering (uniting fifteen researchers in Austria to address the challenge of building reliable and safe computer systems). With his enthusiasm and commitment, Helmut completely reshaped the Austrian research landscape in the field of logic and verification in his few years as a full professor at TU Wien.

This special issue features six articles that are closely related to Helmut's contributions and achievements. The first two articles are extensions of conference papers previously

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published by Helmut and his collaborators and students, and are therefore co-authored by Helmut himself.

The first paper, entitled *Para²: Parameterized Path Reduction, Acceleration, and SMT for Reachability in Threshold-Guarded Distributed Algorithms* (co-authored by Helmut's doctoral student Marijana Lazić and his postdoctoral researchers Igor Konnov and Josef Widder), represents the efforts of Helmut's research group to formalize and model check distributed algorithms. The automated verification of distributed algorithms was a recent research interest of Helmut and very important him; notably, he was posthumously awarded an ERC Advanced Grant on this topic.

The second paper, *On Compiling Boolean Circuits Optimized for Secure Multi-party Computation*, describes the application of Bounded Model Checking techniques to secure multi-party computation, allowing two parties to jointly compute a function over inputs that are kept private. The paper, co-authored by Helmut's former doctoral students Andreas Holzer and Stefan Katzenbeisser (among others), is the result of Helmut's striving to push the limits of formal methods and apply them in other fields such as security.

One of the main goals of the National Research Network on Rigorous Systems Engineering (RiSE), which is coordinated by Roderick Bloem and—before his passing—Helmut Veith, is to provide techniques to generate reliable systems that are correct by construction. The third paper, titled *Shield Synthesis* and co-authored by Roderick Bloem and his students and collaborators, is an important step in this direction and describes an approach to automatically generate software shields which enforce which enforce safety properties of unverified systems at runtime.

In 2015, Helmut and his colleagues and collaborators Edmund M. Clarke, Orna Grumberg, Ronald H. Hardin, Somesh Jha, Yuan Lu, Robert P. Kurshan, and Zvi Harel received the Computer-Aided Verification Award for their work on counterexample-guided abstraction refinement [1, 2] and localization-reduction. The fourth and fifth paper are co-authored by joint recipients of this award. The article *Program Synthesis for Interactive-Security Systems* introduces techniques to synthesize programs that follow given security and functionality requirements. The paper *A Methodology to Take Credit for High-Level Verification During RTL Verification* describes the application of abstraction and automated verification of high-level hardware models in industry.

The education of graduate students in the field of logic was an important concern to Helmut, as evidenced by the Doctoral College on Logical Methods in Computer Science which he established. The sixth and final paper, entitled *Keeping Logic in the Trivium of Computer Science: a Teaching Perspective* and contributed by Anna Zamansky and Janos Makowsky, takes up this topic and discusses the current state, shortcomings, and challenges of teaching logic in computer science.

All six contributions to this special issue were presented by their authors at the Helmut Veith Symposium, which took place on October 6, 2017 at TU Wien as part of the International Conference on Formal Methods in Computer-Aided Design (FCMAD). The Symposium was organized by Helmut Veith's research group Formal Methods in Systems Engineering (FORSYTE) to honor his memory. The event also featured a *LogicLounge* with Michael Huth and Janos Makowsky on the topic of Teaching Logic in Computer Science. The LogicLounge, conceived by Helmut Veith and Oliver Lehman and first held at the Vienna Summer of Logic in 2014, is a series of public outreach events in the form of one-hour discussions with eminent scientists in the fields of logic, philosophy, mathematics, computer science and artificial intelligence. The Symposium and the LogicLounge were sponsored by the Vienna Center of Logic and Algorithms, which was also co-founded by Helmut Veith.

Helmut Veith's untimely death was a great loss to the research community, his colleagues and friends, and his family. Helmut is sorely missed, but his legacy is kept alive through the doctoral program he established, the many collaborations he sparked, the public outreach events he initiated, the successful students and researchers he trained and mentored, and his outstanding research contributions.

References

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