Preface

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This collection of articles are extended versions of original papers presented at the Hardware Verification Workshop (HWVW'10), affiliated to the Federated Logic Conference (FLoC'10). The workshop took place in Edinburgh Scotland on July 15 in 2010.

HWVW'10 was the first workshop devoted to formal verification of hardware design. Formal verification methods, and model checking in particular, are extensively used in the industry where they are relied upon to ensure quality and robustness. However, design size and complexity are growing faster than verification capacity.

This phenomenon, known as the “verification gap”, is one of the biggest concerns in the industry; yet we saw a steady dwindling in the number of publications that specifically target hardware. The purpose of this workshop was to rekindle the interest in and enthusiasm for hardware verification. We aimed to encourage new and daring directions, provide a stage for ideas in early developmental stages, and initiate discussions defining the challenges that remain to be tackled. The scope of the workshop included both general research in formal verification techniques for hardware as well as specific issues related to the development of model checking tools.

The workshop also included the Hardware Model Checking Competition (HWMCC'10), which was the third event in this series. Researchers from both academia and industry were invited to submit solvers and benchmark examples. Tool descriptions describing unique features and implementation details of model checkers submitted to the competition were also welcome.

A total of 21 solvers from 9 research teams participated in HWMCC'10. The results were presented at the workshop. See the competition page of HWMCC'10 (<http://fmv.jku.at/hwmc10>) for more details. Remarkably 4 teams participated for the first time with 6 new

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model checkers respectively variants of model checkers. Among the 21 participating model checkers there were 8 new versions of already existing model checkers. The competition prompted model checking researchers in academia and industry to contribute about 173 new benchmarks in addition to the 645 benchmarks collected for the previous edition.

From 9 submitted papers, 7 were selected for presentation. Beside the presentation of the competition results the workshop also included two invited talks. Cindy Eisner from IBM Haifa Research Lab (Israel) asked “Why work on hardware verification”, and Sharad Malik from Princeton University (USA) gave a second invited talk on “Managing State Explosion through Runtime Verification”.

The two workshop chairs Armin Biere (JKU, Austria) and Karen Yorav (IBM, Israel), were joined by Koen Claessen (Chalmers University of Technology, Sweden) who acted as competition chair together with Armin Biere. Beside the workshop and the competition chairs, the program committee consisted of Roderick Bloem (Graz University of Technology, Austria), Alessandro Cimatti (FBK-IRST, Italy), Zurab Khasidashvili (Intel, Israel), Daniel Kröning (University of Oxford, United Kingdom), and Sanjit Seshia (University of California, Berkeley, USA).

The reviewing process for this collection of extended papers followed the peer review principle and was performed by asking the submitting authors for mutual (blind) reviews.