SBESC 2014 guest editors' introduction

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In 2014, the Embedded Systems track of the Brazilian Symposium on Computing Systems Engineering (SBESC) received 43 full submissions. According to the ranking produced by the Program Committee, six submissions have been identified as Best Paper Candidates and thus have been invited to appear in this special issue of DAEM. We invited the authors of all six papers to submit an extended and revised paper for consideration in this journal. After a strict review process we selected three papers for inclusion in this special issue. The excellent result is now available to the readers of DAEM!

The first paper is “Verification of Fixed-Point Digital Controllers Using Direct and Delta Forms Realizations” by Iury Bessa, Hussama Ismail, Lucas Cordeiro, and João Edgar Chaves Filho. In this paper the authors describe a novel verification methodology, which employs Bounded Model Checking (BMC) based on Satisfiability Modulo Theories (SMT) to verify the occurrence of the design errors in fixed-point digital controllers. The experimental results show that the delta-form realization substantially reduces the digital controllers’ fragility when compared to the direct-form realization.

The second paper is “System-Level Design based on UML/MARTE for FPGA-based Embedded Real-Time Systems” by Marcela Leite and Marco Aurélio Wehrmeister. In this paper the authors propose a novel approach to automatically generate VHDL descriptions from UML/MARTE high-level models of embedded real-time systems. By using concepts and techniques of Model-Driven Engineering (MDE) and Aspect-Oriented Software Development (AOSD), this approach improves the separation of concerns related to the crosscutting concerns introduced by non-functional requirements. Results show an improvement in system design in terms of an increase in system performance as well as a better utilization of FPGA reconfigurable resources.

The third paper is “Potential analysis of a superscalar core employing a reconfigurable array for improving instruction-level parallelism” by Marcelo Brandalero and Antonio Car-

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los Schneider Beck Filho. This paper discusses a new organization for x86 processors by adding a tightly coupled reconfigurable array. Results show that the proposed approach has a potential to improve the performance up to 2.5x with respect to the traditional superscalar x86 architecture.

We would like express our gratitude to the Program Committee of SBESC for their hard work on reviewing the papers for the conference, the additional reviewers who helped us with the review process of this special issue, as well as the authors themselves for their excellent contributions.

Guest Editors and Technical Program Chairs, SBESC 2014