CODES+ISSS 2009 guest editors' introduction

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We are pleased to bring you extended versions of the two best papers from CODES+ISSS 2009. The first paper “LOP: A packet classification architecture with higher throughput and lower power consumption than TCAM” by Xin He, Jorgen Peddersen, and Sri Parameswaran, describes how packet classification is implemented in modern network processors used in embedded systems such as routers. This contribution presents an approach which overcomes some disadvantages of the state of the art systems especially with respect to power consumption. Currently often Ternary Content Addressable Memory (TCAM) to improve the performance of rule matching is used. This paper presents an SRAM-based architecture where incoming packets are compared against parts of all rules simultaneously until a single matching rule is found for the compared bits in the packets. As the authors demonstrate, this new approach reduces power consumption as only a segment of the memory is compared against the incoming packet. In addition the parallel comparison of multiple packets improves bandwidth over TCAM approaches compensating the additional time penalty for matching single packets.

The second paper entitled “Squashing Code Size in Microcoded IPs while Delivering High Decompression Speed” by Chengmo Yang, Mingjing Chen, and Alex Orailoglu proposes a fast code compression technique. This could improve microcoded customized IPs which offer superior performance and direct programmability of microarchitectural structures compared to instruction-based processors, but at the cost of drastically enlarged code sizes. The presented approach takes especially advantage of the fact that the microcodes contain a sizable amount of unspecified bits. The proposed compression strategy is linear in time and therefore enables the development of a decompression engine generating at runtime the decompressed code in such a way that all the specified bits can be filled as required

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by a fixed-bandwidth XOR network resulting in very low performance and hardware overhead.

We hope readers will enjoy both of these great papers focusing on different important aspects of embedded systems.

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