Introduction to the special issue on Low-power circuit techniques

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This special issue of “Low-power circuit techniques” in the Springer Journal of Analog Integrated Circuits and Signal Processing is published with six papers, which are selected from presented papers at the 2012 International Conference on Analog VLSI Circuits (AVIC 2012). This conference is believed to be the only conference that bares the key word “Analog VLSI”, and have accepted very wide range of papers concerning analog circuits. Among them, we called for papers related to low-power circuit techniques for this special issue.

The Research Committee on Electronic Circuits of the Institute of Electrical Engineers of Japan (IEEJ) was sponsoring and cooperating with Analog Devices Inc., the University of Valencia and the Polytechnic University of Valencia to hold the 2012 International Conference on Analog VLSI Circuits in Valencia, Spain, on October 24–26, 2012.

This conference is the successor of former International Analog VLSI Workshop, which had been successfully held for 14 years. The purpose of the conference is to exchange information, ideas and recent research results on analog VLSI circuits and their applications. This workshop has formed a long-standing community for various analog

VLSI circuit specialists from both industry and academia worldwide, and promoted active brainstorming among them at the site.

The first two papers are related to power supply circuits and DC–DC converter circuits. The first paper by Nomura et al. presents photovoltaic cell design, oscillator, and bootstrap charge pump circuit integrated on an 0.18 μm CMOS chip, to provide power generation and voltage boost functions on stand-alone microsystems.

Sato et al. present a theoretical analysis of efficiency in charge pumps for LED drivers and describe a novel procedure to minimize power loss by applying adiabatic process to charge pump circuits.

The third paper by Tanimoto et al. presents a fully-differential OTA operating from 1-V power supply. The OTA consists from CMOS cascode inverters to obtain a high voltage gain while maintaining rail-to-rail input common-mode range at 1-V power supply. They also fabricated a test chip by using 0.15 μm CMOS technology and confirmed the design techniques to be useful.

The fourth and the fifth papers are concerning to high speed communication signal processing. Nakagawa et al. present a passive complex filter design approach, which is relevant to low power analog signal processing at very high frequency. The concept is exemplified with two complex filters operating at 100 kHz and 10 MHz but maybe extended beyond tens of GHz.

The fifth paper by Yazaki et al. presents a design of a 20-Gbps CMOS optical receiver, which does not require inductor to suppress power supply noise by a unique design of power supply noise canceling circuit. The designed chip was fabricated in 90 nm CMOS technology and demonstrated effectiveness of the design.

The last paper by Carbajo et al. presents a new version of the well known Goertzel algorithm for discrete Fourier

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transform that can save area and reduce power consumption at the expense of accuracy. This might be particularly useful for analog front ends involving low frequency signals and sigma delta ADC.

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