Introduction to the special issue “2011 International Analog VLSI Workshop”

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Published online: 12 February 2013
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This special issue of the SPRINGER Journal of Analog Integrated Circuits and Signal Processing is published with 9 papers selected from presented papers at the 2011 International Analog VLSI Workshop (AVLSIWS2012). The conference was held in Bali, Indonesia on October 2–4, 2011. This conference was organized by the Research Committee on Electronic Circuits of the Institute of Electrical Engineers of Japan (IEEJ) in cooperation with the Bandung Institute of Technology. The purpose of the conference is to exchange information, ideas and recent research results on analog VLSI circuits and their applications.

The first 4 papers are related to power supply and power management circuits. The first paper by Eiichi et al. presents a low power wake-up receiver with CMOS operating in the subthreshold current region. The paper is focusing on the development of low-power envelope detector, high-gain amplifier and PWM CDR. The fabricated detector and high-gain amplifier only consumes 6.8 μ W from a 1.5-V power supply voltage.

The second paper by Zachary et al. presents a design of boost regulator for energy harvesting applications. The proposed circuit uses two different control schemes for

startup and steady-state operation. At the startup operation, a fixed-frequency oscillator is used to increase the output voltage up to sufficient level for steady state operation. At the steady state operation, a constant-on-time hysteretic control system is used to increase the efficiency. The proposed circuit can start up with an input voltage of 240 mV and achieve a maximum efficiency of 97 %.

Toshiko discusses the design concepts of wireless sensor network system constructed with autonomous sensing nodes, which operates at extremely low power levels. The paper reviews a structure health-monitoring system, monitoring methodology with a focus on quantitative measurement accuracy, and issues of node synchronized sampling, multi-layer cluster, node distance and integrated sensor node module. Design example using a Wheatstone bridge strain sensor is demonstrated.

Bin Shao presents a design of buck converter utilizing a low quiescent current PFM switching method. The proposed method improves the efficiency of the converter at a light load condition. An adaptive accurate zero-cross comparator for discontinuous mode and very low quiescent current circuit technique in skip period operation are introduced. The proposed circuit improves the efficiency at a 5-V input, 3-V output and 10-mA load by 60 % compared to a conventional circuit with PWM switching method.

The fifth paper by Antaryami et al. presents a novel four quadrant voltage multiplier using bulk input for low-power low-voltage applications. The proposed circuit uses a current mirror operated in weak inversion region as an input stage where the bulk of MOSFETs are used as input terminals. The proposed circuit achieves a 5.8 % THD for 80 mV input voltage amplitude under 0.5 V power supply voltage. The power consumption of the proposed circuit is 714.3 nW.

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Takahide et al. present a design of low distortion active inductor with OTA based gyrators and its applications. The work is focusing on the linearity deterioration caused by dependency of OTA's transconductance to input voltage. The authors improve the linearity of their proposed circuit using an adaptive bias current control for the gyrators. A band-pass filter and VCO are designed to demonstrate the application of the proposed active inductor.

A MOS transconductor with improved linearity is presented by Takeshi et al. in the seventh paper. The proposed circuit utilizes two local feedbacks to a conventional differential pair. The first one is a local feedback using a super source follower, which has been proposed by the same research group. In their new design, they add source degeneration to the differential pair using MOSFETs in subthreshold region to improve the linearity of the transconductor. The application to a low-pass filter is shown to demonstrate the performance of the proposed transconductor.

Renyan et al. presents their work on the development of a hardware-efficient on-line-learnable processor for the K-means clustering of highly dimensional vectors. They develop an analog fully parallel self-converging circuitry for the K-means algorithm to improve the speed of learning process. The proposed analog based hardware only needs 20,000 of transistors while the learning speed is 10 M vectors/s, compared to digital based hardware which needs 414,000 gates and only have a learning speed of 1.38 M vectors/s.

The last paper, by Yuki et al. proposes the use of vector filter in the feedback path of CT delta-sigma modulator to reduce the effect of clock jitter and excess loop delay. The vector filter simultaneously realizes a low-pass and a high-pass characteristic. A simulation with 0.1 % clock jitter shows that the proposed circuit improves the SNR by 22.5 dB.

Acknowledgments We would like to express our gratitude to all reviewers who have been a great help in the selection of the papers. We believe that the quality of the papers has been improved by their invaluable comments.

Akira Yasuda was born in Tokyo, Japan, in 1962. He received the B.E., M.E., and Ph.D. degrees in electronics engineering from Hosei University, Tokyo, in 1986, 1988, and 2000, respectively. In 1988, he joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan. From 2000 to 2001, he was a Member of Technical Staff with Burr-Brown Japan Ltd. (Texas Instruments Japan Ltd.) research and development department. Since 2001, he

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