

# A 5th-order $\Sigma\Delta$ modulator with combination of op-Amp and CBSC circuit for ADSL applications

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**Abstract** In this letter, a 5th-Order single-loop low distortion Sigma-Delta Modulator (SDM) is implemented with the combination of the comparator-based switched-capacitor (CBSC)-based and op-amp-based techniques for asymmetric digital subscriber line (ADSL) applications. This structure, which uses integrator (CBSC-based) and IIR filter (op-amp-based) concurrently, has relatively fewer feed-forward paths and modulator coefficients for sensitivity reduction to mismatch. To lower the power consumption of the modulator, the integrators are implemented with CBSC, the IIR filter block is implemented by single OTA, and a passive adder is used to realize the adder at the input of the 5-bit quantizer. The design purpose is minimizing the power consumption while the dynamic performance maintains high. As shown in the simulation result, for a 2-MHz signal bandwidth, the modulator achieves a dynamic range (DR) of 86.5 dB and a peak signal-to-noise and distortion ratio (SNDR) of 85 dB with an oversampling ratio of 8. In addition it consumes 18.75 mW from a 1.8-V power supply at 32 MS/s, which obtains a figure of merit of  $1.6e-3$ .

**Keywords** Analog-to-digital data converter (ADC) · Sigma delta modulator · Comparator-based switched-capacitor circuit · ADSL

## 1 Introduction

Nowadays, new generation communication systems are imposing two challenges in designing the analog-to-digital converters (ADCs). One challenge is increase of input signal frequency because of entering in several MHz bandwidth applications and the other is the high resolution ADCs, while the size of transistors and the circuit supply voltage are becoming smaller [1]. The design of an ADC oriented to ADSL application becomes a difficult task with technology scaling. Technology scaling, which is the most challenging factor in nano-scale processes, makes some issues on design of high performance op-amps, which are one of the crucial analog building blocks in the switch-capacitor (SC)-circuits ADCs. It decreases intrinsic gain (lower output resistance), voltage headroom and SNR while it increases device leakage, nonlinearity and mismatch [2, 3]. The most important problem is decreasing the device gain. It causes that, the precision in the feedback circuits is dramatically reduced, because in the traditional SC circuits a high gain op-amp determines the accuracy of the charge transfer. A method for achieving higher gain without reducing voltage swing is to cascade several gain stages, but it leads to the stability problem. Furthermore, high gain op-amp can be realized by cascoding transistors, but voltage headroom will be reduced. With decreasing the signal amplitude a larger capacitance and also more power consumption is needed to maintain the same SNR [4]. Different solutions have been introduced to deal with the power issue such as the time-to-digital converter (TDC)

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[5], incomplete settling [6] and switched op-amps [7]. Recently, a comparator-based switched-capacitor (CBSC) technique was reported in [8, 9] to replace the op-amp with comparator and current sources, which has the same operation like as op-amp-based architecture. In CBSC technique, a comparator and switched current sources are used to sense the virtual ground condition, instead of forcing it with an op-amp. One of the issues, which conventional architecture [8] suffers from it, is overshoot at the end of the coarse phase which decreases the speed and accuracy. The implementation of the SC overshoot correction circuit helps us to increase the speed (fastest settling) and decrease power consumption. In this paper design of high resolution and bandwidth sigma-delta modulator, which uses CBSC-based integrators and an op-amp-based IIR filter in its architecture, is investigated. The effectiveness of this hybrid architecture is justified through simulation using HSPICE in a 0.18 μm CMOS process and compared with the state-of-the-art SDMs.

### 2 Modulator architecture

There are two architectures for designing a Sigma-Delta modulator: Single-loop high-order and MASH (Cascade) SDM. In this article, we utilize single-loop high-order architecture for implementation of the modulator. In SDMs with traditional architecture the OTA employed in integrator needs a large swing, and must have a large DC gain and slew rate (SR) in order to overcome against nonlinear effects. High OTA DC gain results in high power consumption of the modulator. To solve this problem, we use CBSC structure instead of OTA in integrators. Moreover for decreasing the integrator swing, we applied a structure sigma-delta known as low-distortion [10], which uses feed-forward paths to decrease the integrator swing. This low-distortion modulator, illustrated in Fig. 1, just employs one digital to analog convertor (DAC) in main feedback path. In this structure, that uses feed-forward paths, the integrators in the modulator loop process only the quantization noise and prevent generation of large Swing. The single-loop high order.

SDMs may become unstable on large inputs; therefore in high-order structures we use the multi-bit quantizer. This

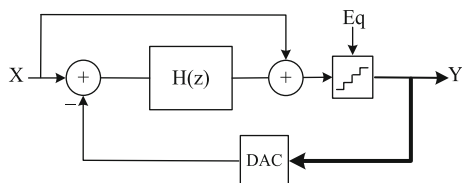


Fig. 1 Low-distortion sigma-delta modulator architecture

causes settling in integrator to be relaxed more and decreases instability conditions. The proposed architecture is applied to a 5th-order single-loop SDM, with combination of CBSC-based integrators and Op-amp-based IIR filter. Figure 2 shows the modulator structure in which we used a 2nd-order IIR filter block instead of two integrators. The transfer function of the filter is represented in Eq. 1.

$$H_{IIR} = \frac{b_1z^{-1} + b_2z^{-2}}{1 - c_1z^{-1} - c_2z^{-2}} \tag{1}$$

This method provides attractive results [11]; first the modulator architecture has less complexity in comparison with traditional structures. Second, the relation between in-band zeroes and noise transfer function (NTF) of SDM is simpler. In this manner, modulator coefficients spread is decreased and finally modulator sensitivity with respect to coefficient mismatching is reduced. The NTF has IIR structure with reverse chebyshev pole and zero. NTF for a 5th-order modulator with OSR = 8 is expressed as follows:

$$\begin{aligned} \text{NTF}|_{\text{OSR}=8}(z) &= \frac{(z - 1)(z^2 - 1.875z + 1)(z^2 - 1.955z + 1)}{z^5 - 1.2z^4 + 1.119z^3 - 0.495z^2 + 0.276z - 0.0331} \end{aligned} \tag{2}$$

With some simple calculation, we can achieve coefficients values, which are presented in Fig. 2.

### 3 Design of key building blocks

#### 3.1 CBSC gain stage

Figure 3 shows the complete CBSC-based integrator, along with its timing diagram. In  $\phi_1$  phase, the input is sampled by the input capacitors ( $C_{S1}$  and  $C_{S2}$ ). The charge transfer phase  $\phi_2$  is divided into four following sub-phases: (a) preset phase for preset switches ( $P_{rst}$ ), (b) coarse transfer phase (E1), (c) fine transfer phase (E2) and (d) settling phase ( $S = P_{rst} + E1 + E2$ ). After sampling, the outputs ( $V_{op}$  and  $V_{on}$ ) are preset to  $V_{REFP}$  and  $V_{REFN}$ . Preset phase ( $P_{rst}$ ) sets the output nodes to preset levels away from the common voltage level ( $V_{CM}$ ). After preset phase, coarse charge transfer phase is started. Ia current source charges the positive half circuit and discharges the negative half circuit simultaneously. As a result, input nodes of the comparator ( $V_c$  and  $V_d$ ) are charged in opposite directions to cross each other to make the first decision as seen in Fig. 3(b). However, there is overshoot in the output due to the delay in the comparator and ramp rate ( $V_{ovp}$ ). Overshoot in the coarse phase is one of the most important limiting factors on the performance of the CBSC circuits. To reduce the primary overshoot at the end of the coarse phase, an SC

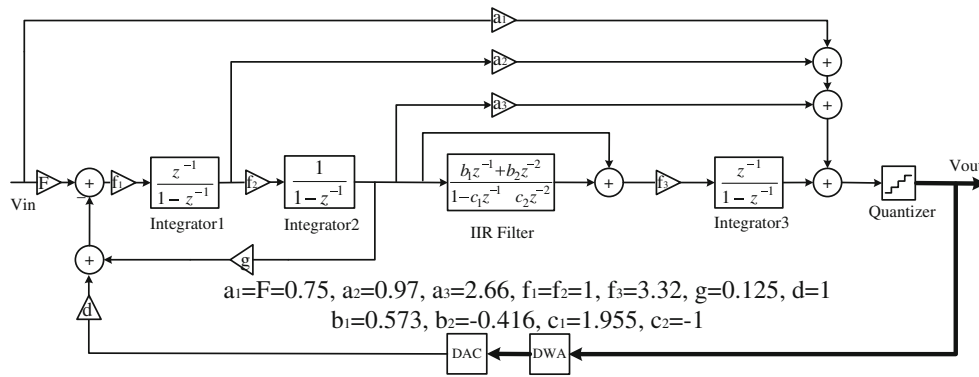
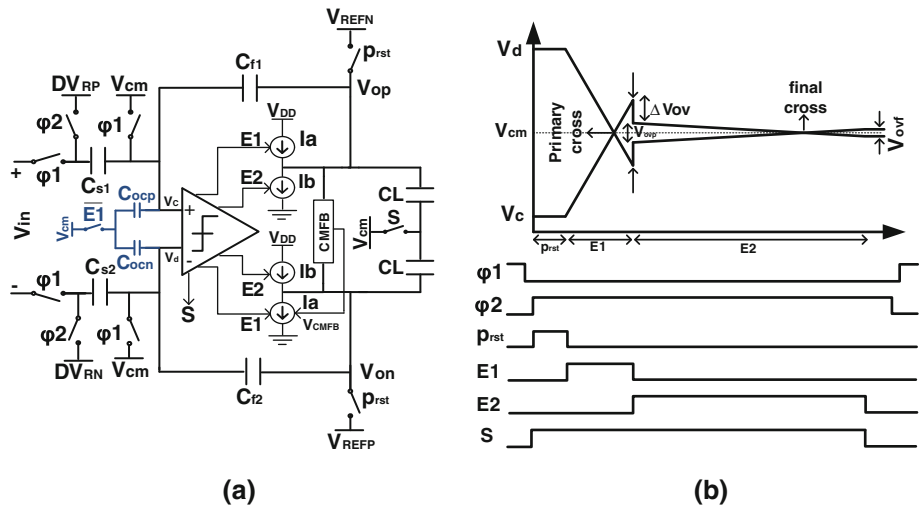


Fig. 2 The proposed 5th-order sigma–delta modulator architecture

Fig. 3 a CBSC-based integrator b timing diagram



overshoot correction circuit is introduced which shown in Fig. 3(a). For instance, at the end of the coarse phase, the amount of the primary overshoot is subtracted from  $V_c$  and is stored in  $C_{ocp}$ . This leads to the reduction of overshoot voltage, which has been produced in the coarse phase for saving power. After correction, the output voltage at the end of the coarse phase is defined as below:

$$V_o = V_{IN} - D \cdot V_{REF} + \frac{2I_a \cdot t_{d1}}{C_T} - \Delta V_{OV} \quad (3)$$

where  $I_a$  is the coarse current,  $D$  is the digital code determined by the quantizer and logics,  $C_T$  is the total loading capacitance at the output of the gain stage and  $t_{d1}$  is the delay of the comparator for a coarse ramp input. The term  $\Delta V_{OV}$  is correcting factor, which decreases the overshoot voltage produced at the end of coarse phase (E1). To achieve more accurate output, the fine transfer phase is used. During this phase, fine current sources (Ib) are turned on to reduce the overshoot voltage and also achieve to the second detection as seen Fig. 3(b). The voltage comparator [12], is depicted in Fig. 4, consists of three stages: an input

pre-amplifier (M1–M7), a decision stage (M8–M12) and an output buffer (M13–M17). The input stage (low-gain, high-bandwidth amplifier) converts the input voltages to currents level needed to drive the decision stage. The decision stage is a bistable cross-coupled circuit which switches from one state to another in accordance with the magnitude of the input currents. The positive feedback speeds up the switching. The output stage is used to convert the output voltage of the decision circuit into the digital logic signal. To reduce static power consumption, the comparator is controlled by signal  $S$ . When signal  $S$  is active ( $S = 1$ )  $V_{bias}$  is connected to the circuit and the comparator is in the operation mode. If  $S$  is not active, ( $S = 0$ ) path between  $V_{bias}$  and circuit is disconnected and the comparator turns off. For coarse current sources which generate a large amount of current we used cascade current sources to achieve high output resistance for increasing the accuracy and linearity. A PMOS current source was used for the pull-up current, and a NMOS current source was used for the pull-down current during the coarse charge transfer phase. Also the effective open-loop gain  $A_o$  of a CBSC circuit [8] is modeled as:

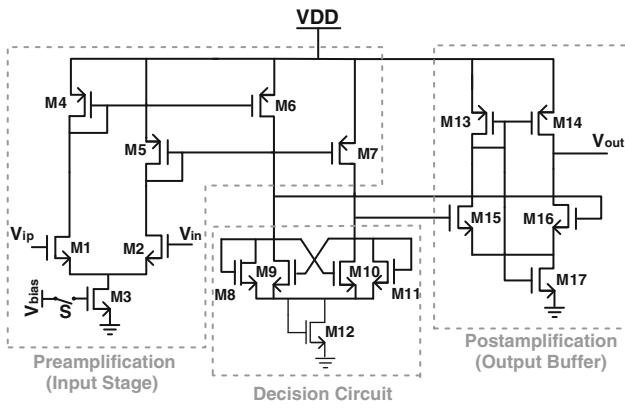


Fig. 4 Threshold-detection comparator

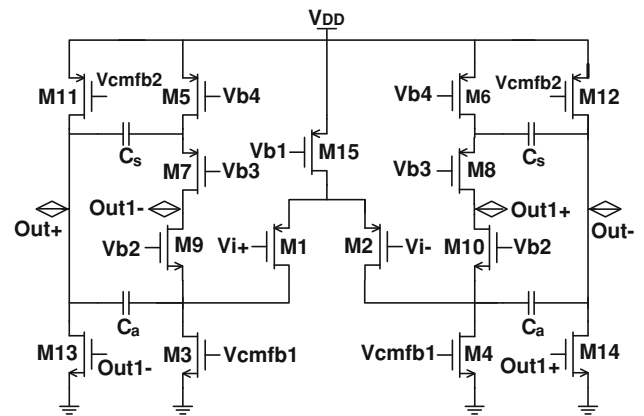


Fig. 7 The OTA structure used in 2nd-order IIR filter

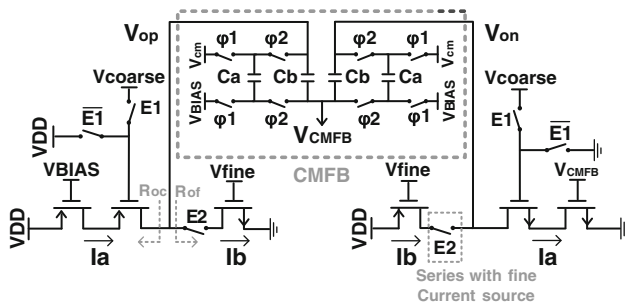


Fig. 5 Current sources with CMFB circuit

$$A_O = \frac{C_T \cdot R_O}{\alpha \cdot t_d} \quad (4)$$

where  $C_T$  is the total capacitance at the output of each stage,  $R_O$  is the finite output resistance of the current source,  $t_d$  is the delay of the threshold-detection comparator, and  $\alpha$  denotes the feedback factor. For enhancing the accuracy in the fine

current source [13] the controlling switch is connected to the drain. As a result when E2 is active ( $E2 = 1$ ), it makes a cascade combination. So we have good accuracy in accordance with Eq. 4. During the transfer phase ( $\varphi_2$ ), a switched-capacitor common-mode feedback (CMFB) is used to control the pull down coarse current source. The CMFB circuit and current sources are shown in Fig. 5.

### 3.2 IIR filter

2nd-order IIR filter block is implemented as illustrated in Fig. 6(a). Because of low output swing of 2nd-order filter, 1st part can be made with single OTA that has the same accuracy and performance of 2nd-order filter with two OTAs [14] as depicted in Fig. 6(b). The p-path part of Fig. 6(b) is realized by capacitor  $C_{h1}$ , which samples output in  $\varphi_1$  and transfers the relative charge to the capacitor  $C_{13}$  in  $\varphi_2$ . The q-path part achieves by delayed-sampling at

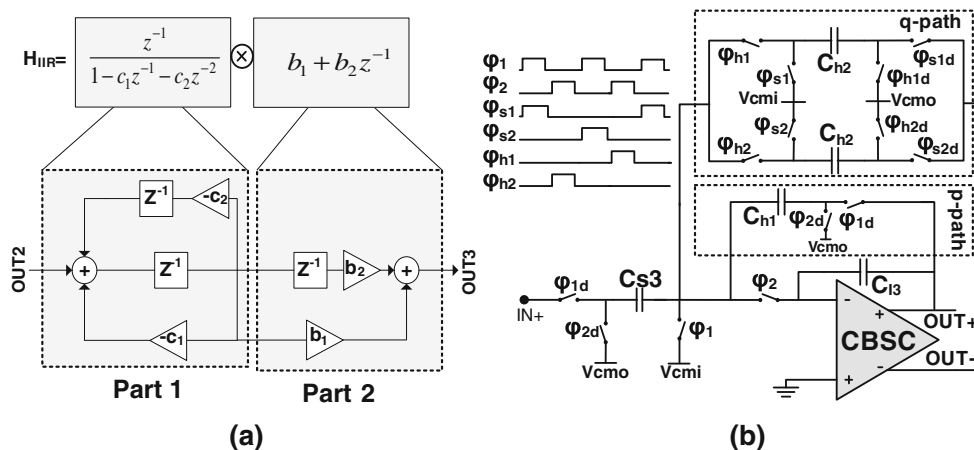


Fig. 6 a The segregated diagram of 2nd-order IIR filter transfer function b 1st part implementation of IIR filter

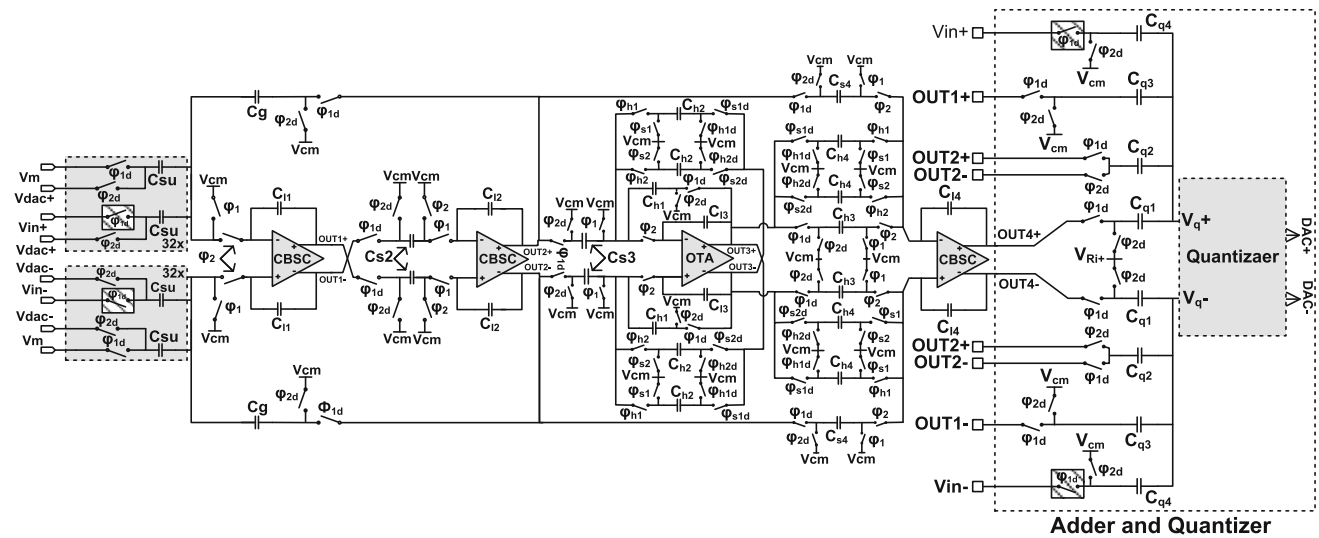


Fig. 8 Fifth-order switched-capacitor delta-sigma modulator

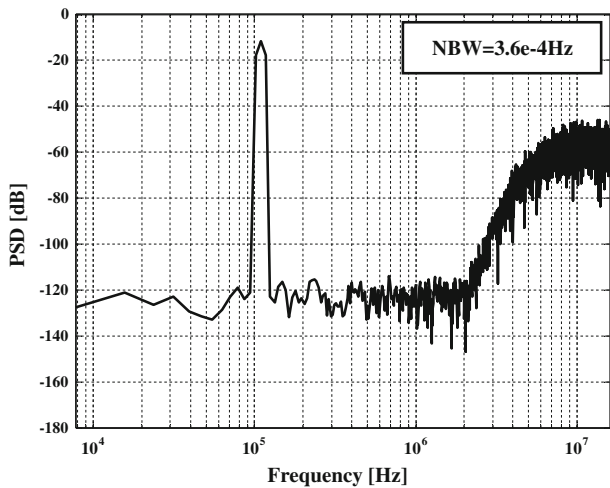


Fig. 9 Simulated output spectrum of CBSC-based SDM at the transistor level

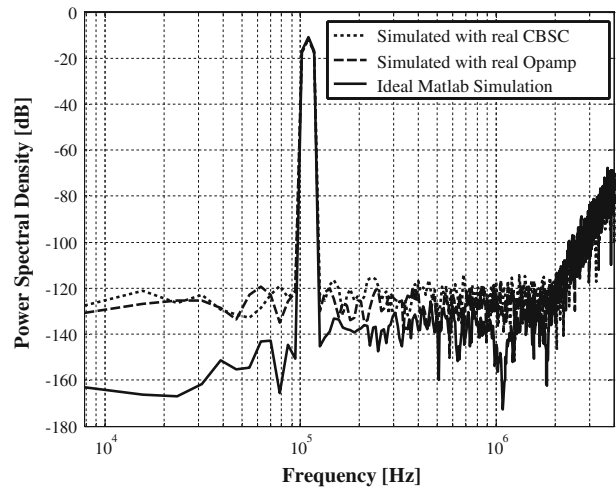


Fig. 10 PSD comparison between the approaches

feedback paths with two sampling capacitors ( $C_{h2}$ ). The mismatching between q-path capacitors causes to limit the attenuation of the quantization noise. Because of placing the IIR filter block in back-end stages, the error is shaped by previous stages, and with 0.4 percent capacitance mismatch, the SNDR remains above 85 dB. The second part of Fig. 6(a) can be combined with the last integrator of the modulator in order to perform the implementation of IIR filter block by means of single OTA. As shown in Fig. 7, a 2-stage folded-cascade class A OTA is employed to implement the IIR filter block [15]. In this structure, in addition to  $C_s$  compensation capacitor, the  $C_a$  capacitor is employed to keep circuit poles further away from zero frequency in order to attain higher rate and bandwidth with respect to conventional structures.

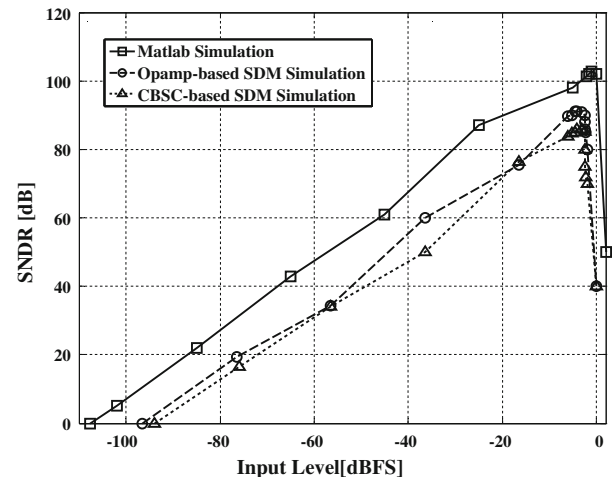


Fig. 11 SNDR versus normalized input signal amplitude of the modulators

**Table 1** Performance comparison

Reference	BWN (MS/s)	SNDR (dB)	CLK@OSR (MHz)	Topology	Power (mW)	Process ( $\mu\text{m}$ )	DR (dB)	FOM (10 <sup>-3</sup> )
[10]	4	82	32@8	4-Bit S.C. 5th Single-loop	150	0.18	83	0.09
[16]	2.5	89	40@16	4-Bit S.C. Cascade 2-1-1	87	0.25	–	0.4
[18]	2.5	90	40@16	4-Bit S.C. 4th Single-loop	40	0.13	92.5	1.8
[19]	30	62.5	300@10	4-Bit C.T. 4th Single-loop	70	0.13	67.5	0.04
[20]	25	72	200@8	4-Bit S.C. 5th Single-loop	200	0.18	84	0.52
[21]	5	80.5	60@12	4-Bit C.T. 4th Dual-loop	50	0.25	85	0.53
This work	4	85	32@8	5-Bit S.C. 5th Single-loop	18.75	0.18	86.5	1.6

$$\text{FOM} = (4\text{KT} \cdot \text{DR} \cdot \text{BWN}) / P_{\text{diss}}$$

SC switched capacitor, CT continuous time

### 3.3 Other parts of SDM

Figure 8 shows the switched capacitor implementation of SDM. As shown in Fig. 8, a passive adder at the input of quantizer is utilized for adding the feed-forward paths of the modulator [16]. This method does not need extra OTA, but causes the adder gain to be less than one. For alleviating this problem, we must use the scaling technique of reference voltage at quantizer input. After preparing the quantizer output that has 33 quantization levels, it is fed back to a DAC and the DAC output is subtracted from the input signal of the modulator. Because of DAC nonlinearity effects, we used a linearization algorithm called Data-Weighted Algorithm (DWA), in front of the DAC.

## 4 Simulation results

In this section, results obtained from system level simulation (MATLAB) and circuit level simulation using Hspice in 0.18  $\mu\text{m}$  CMOS process are compared. Figure 9 shows the output power spectrum density (PSD) of the CBSC-based modulator with input signal amplitude -4 dBFS and input frequency  $f_{\text{in}} = 109.375$  kHz. Sampling frequency and Oversampling ratio are  $f_s = 32\text{MS/s}$  and  $\text{OSR} = 8$ , which yields a signal bandwidth (BW) of 2 MHz. This spectrum, which computed via a 4096-FFT point, confirms the performance of this technique through comparison with conventional op-amp-based modulators as shown in Fig. 10. With a noise bandwidth (NBW) of  $3.6 \times 10^{-4}$  Hz [17], the maximum values for the SNDR are 101 dB in the SIMULINK, 91.2 dB for the op-amp-based SDM and 85 dB for the CBSC-based SDM. Figure 11 shows the simulated SNDR versus the input signal amplitudes normalized by reference voltage ( $V_{\text{ref}}$ ). The dynamic range

(DR) of CBSC-based modulator is 86.5 dB, which shows good agreement to the modulator simulated in MATLAB. The simulated power consumption is 18.75 mW from 1.8 V power supply, which obtains a figure of merit of  $1.6 \times 10^{-3}$ . Table 1 shows the performance comparison of state-of-the-art SDMs.

## 5 Conclusions

This letter addresses a 5th-order high resolution and broadband delta-sigma modulator with hybrid utilization of op-amp and CBSC circuit for ADSL applications. High performance low-distortion SDM is obtained by combination of integrator and IIR filter, which has less feed-forward paths and modulator coefficients for sensitivity reduction to mismatch. Furthermore, we have employed CBSC gain stage to implement integrators which shows efficient architecture can be achieved for this application. In comparison with similar ones, the power dissipation is lower because of using CBSC integrators and decreasing number of OTA in 2nd-IIR filter block. With  $\text{OSR} = 8$ , the peak of SNDR is 85-dB, the bandwidth is about 2 MHz and the power is 18.75 mW. Simulation results verify the usefulness in implementation and fabrication of the proposed architecture.

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