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Inverter-based 1 V analog front-end amplifiers in 90 nm CMOS for medical ultrasound imaging

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Abstract In this paper, we present the design and experimental evaluation of 1 V analog front-end amplifiers designed in 90 nm CMOS technology for capacitive micro-machined ultrasound transducers (CMUTs) for medical ultrasound imaging systems. We propose two front-end amplifier topologies based on an inverter-based cascode amplifier; the first is a continuous time amplifier and the second is a charge sampling amplifier (CSA). The proposed front-end amplifiers are designed to amplify the signals from CMUTs in the frequency bandwidth from 15 to 45 MHz with a centre frequency of 30 MHz. From the measurements, the continuous time single-ended transimpedance amplifier achieves a voltage gain of 19 dB, an output noise power spectral density of 0.042 (μV)/SQRT(Hz) at a centre-frequency of 30 MHz, and a total harmonic distortion of −23 dB at 450 mV p–p output voltage at 30 MHz input signal frequency. It draws only 598 μA per amplifier from a 1 V power supply. Its area measured only about 32 μm × 32 μm per amplifier. On the other hand, a sampling based front-end amplifier [CSA] achieves a transfer gain of 17.4 dB at an input signal frequency of 30 MHz and an upper 3 dB cut-off frequency of 46 MHz at a sampling clock frequency of 100 MHz. It consumes 586 μA per amplifier from a 1 V power supply and achieves a signal-to-noise (SNR) ratio of 45.7 dB with a peak-to-peak output signal amplitude of 500 mV at a sampling frequency of 100 MHz. It occupies an area of 1470.2 μm^2 (which is equivalent to 38 μm × 38 μm), which also includes the area of the switches for the CSA that will be used for the single CMUT element.

Keywords Inverter-based amplifier · Ultrasound front-end · Charge sampling · Self-biased CSA · Medical imaging · CMOS

1 Introduction

Ultrasound imaging has been in use since the 1970s for medical diagnosis for a wide variety of medical investigation purposes [1]. It has also become common practice to use ultrasound imaging during surgery, including intravascular ultrasound (IVUS) imaging. Compared to general purpose ultrasound imaging systems, IVUS imaging system requirements are quite challenging and in particular the probe in IVUS imaging systems is based on a catheter with a diameter of the order of 1 mm or less. The combination of high frequency, small form factor, and good performance requires ultrasound transducers and interface electronics to be tightly integrated [2, 3]. In such catheter based IVUS imaging systems, the latest ultrasound sensors, capacitive micro-machined ultrasound transducers (CMUTs), fit best compared to conventional piezoelectric transducers, as CMUTs are compatible with the well known CMOS process. These CMUTs are replacing the long-established piezoelectric transducers in high frequency and high resolution ultrasound imaging due to their attractive features of micro-fabrication, wide bandwidth, very high level of integration, and batch fabrication [4–6]. CMUTs can easily be integrated with CMOS front-end

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electronics either through flip-chip bonding [7–9] or monolithically through CMUTs on the CMOS process [2, 3, 10, 11]. The integration of CMOS electronic circuits with CMUTs will greatly cut down the cost of ultrasound imaging systems as the mass production of CMOS electronic integrated circuits is very cheap. Such integration of CMUTs with CMOS front-end electronics fits best with the requirements of IVUS imaging system probes. All these best features of CMUTs along with low-cost high-performance CMOS interface electronic circuits enable us to make a very cost effective integrated ultrasound system [2–11].

For ultrasound imaging systems like catheter based IVUS ultra sound systems [12] it is obvious that the CMOS front-end electronic circuits should be very compact in size and should have low power to avoid heating the blood too much. One way to meet such design goals, is to design area optimized analog front-end circuits by introducing novel circuit architectures to meet small area, low power, and performance requirements. A second approach is to design the front-end electronic circuits in deep submicron CMOS technologies to take advantage of their small feature sizes and low supply voltages. Using such scaled down deep submicron CMOS technologies after analog-to-digital (ADC) conversion in the signal processing chain will greatly improve the overall ultrasound system performance in terms of area and power. From the integration aspects, it is better to also design the front-end analog amplifiers in deep submicron technologies, although this imposes many challenges in the design of analog integrated circuits in scaled down deep submicron CMOS technologies because of low supply voltages [13–17].

The existing ultrasound analog front-ends reported in the literature are the continuous time type with resistive feedback or a combination of resistive and capacitive feedback [2, 3, 5–9, 11, 18]. However, most of these front-ends target much lower frequencies and are not designed in state-of-the-art deep submicron technologies to achieve small area requirements. These continuous time mode ultrasound front-ends are also not best suited for high frequency catheter based ultrasound systems. To achieve the low area and low power requirements of the ultrasound analog front-end for catheter based ultrasound systems [12], we propose a single-ended transimpedance amplifier topology by utilizing an inverter-based cascode amplifier in 90 nm CMOS technology as compared to the circuits designed in older CMOS technologies [2, 3, 5–9, 11, 18].

The closer we move the ADC block to the sensors in any system, the more efficient the system will become as there will be less loss. To lay the foundation in those lines, we propose a charge sampling architecture as an ultrasound analog front-end. Recently, charge sampling has been demonstrated as an attractive alternative compared to the usual well known voltage sampling in high speed applications, even with low supply voltages [19–24]. Charge sampling has also been proved to have better immunity to clock jitter for certain ranges of input signal frequency [25–27] and better performance at high speed and low voltage operation compared to voltage sampling [19–24]. Although high speed charge integrating mode architectures [23, 28, 29] have been reported, these were not used as ultrasound front-ends and also were not designed in state-of-the-art deep submicron technologies. To achieve the low power, low area, and high speed requirements of the ultrasound analog front-end for a catheter based ultrasound system, self-biased CSA that utilizes an inverter-based folded cascode amplifier is proposed in a 90 nm CMOS technology. The performance of the self-biased CSA is also compared with the recently reported similar sampling architectures [23, 28, 29].

This paper is organized as follows. The second section describes the two front-end amplifier topologies for CMUTs. In the third section, the design of the single-ended transimpedance amplifier and self-biased CSA in state-of-the-art 90 nm CMOS technology is presented. In the fourth section, simulation and measurement results are presented in detail. Finally, the conclusions of this paper are given in Sect. 5.

2 Description of the proposed front-end topologies for CMUTs

In this section, two front-end amplifier topologies (single-ended transimpedance amplifier and self-biased CSA) are presented. Section 2.1 describes the single-ended transimpedance amplifier and Sect. 2.2 describes the self-biased CSA.

2.1 Single-ended transimpedance amplifier

The regular transimpedance amplifier consisting of an OTA (dotted lines) with resistive feedback is shown in Fig. 1, which also shows the single-ended transimpedance amplifier topology (if OTA is replaced with a single-ended amplifier block). Here, the signal source is represented by its Norton-equivalent. There are some advantages to using this single-ended topology over the regular topology, as explained below.

From Fig. 1, it can be observed that the regular OTA based transimpedance amplifier requires an additional biasing voltage at the positive input of the OTA; on the other hand single-ended amplifier input will be biased to the output DC voltage through the feedback resistor.

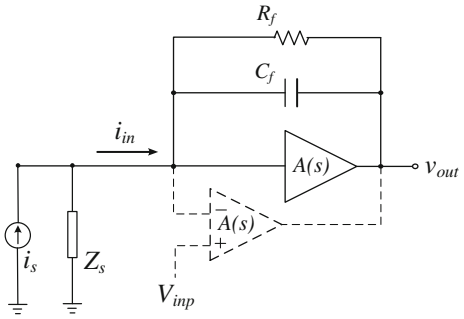

Fig. 1 Proposed single-ended transimpedance amplifier and the regular transimpedance amplifier (*dotted lines*)

As the output DC voltage will be biased at the input, there is a design requirement to match the DC levels at the input and output in the case of a single-ended amplifier.

The closed loop transimpedance gain of the above amplifier is $-Z_f$ if the parasitic capacitances at both ends of the off chip feedback resistor, R_f, are ignored and A(s) is very large. This off chip feedback resistor will be integrated into the chip later on. Here, Z_f is the impedance in the feedback path.

2.2 Self-biased CSA

In this section, first a simple CSA is presented as an analog front-end for CMUTs, and then CMUT is described in detail. Analysis of the CSA and proposed self-biased CSA topology follows after description of the CMUT.

2.2.1 *CSA as an ultrasound analog front-end for CMUTs*

Figure 2 shows a simple CSA [20, 21, 25–27, 30, 31]. As shown in Fig. 2, the CMUT electrical equivalent circuit is used as a signal source. Here, A(s) is the transfer function of the OTA and C_f is the sampling feedback capacitor. In the section below, CMUT is described in detail.

2.2.2 *CMUT*

Advances in Micro Electro-Mechanical Systems (MEMS) fabrication techniques have enabled high performance CMUTs to be constructed. CMUTs are best suited to high frequency ultrasound imaging applications compared to their piezoelectric counterparts, as CMUT technology allows a fine-pitch array of small elements to be fabricated.

CMUT converts ultrasound signals into electric signals and vice versa. The first batch of CMUTs with a centre frequency of 30 MHz and a bandwidth from 15 to 45 MHz has already been fabricated [32]. A cross sectional view of the fabricated CMUT with specifications is shown in Fig. 3.

Basically, CMUT has two modes of operation:

- Transmit mode
- Reception mode

2.2.2.1 Transmit mode In this mode, a DC potential is applied between the two electrodes shown in Fig. 3 to activate the CMUT. When an AC signal is superimposed over the applied DC potential, the membrane oscillates and produces high frequency ultrasound signals. The frequency and bandwidth of the ultrasound signals generated depend on the CMUT physical parameters and bias conditions.

2.2.2.2 Reception mode In this mode, when an incoming acoustic wave hits the CMUT it generates an equivalent electrical signal. Here, the AC signal is replaced with the front-end amplifier (single-ended transimpedance amplifier or self-biased CSA) to amplify the signals generated by the CMUT.

Typical model parameters of the designed CMUTs (see the CMUT electrical equivalent circuit in Fig. 2) are tabulated in Table 1 and used in the single-ended transimpedance amplifier and self-biased CSA design optimization.

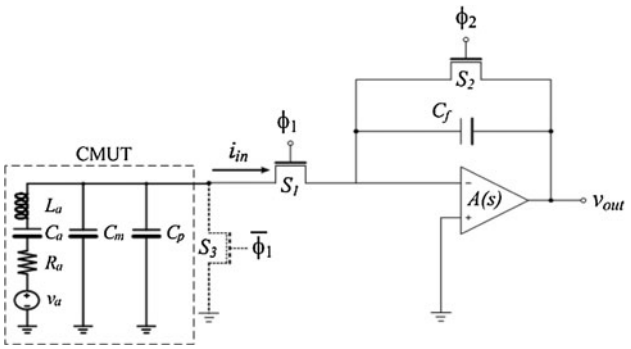

Fig. 2 A simple Charge Sampling Amplifier (CSA) based on an OTA

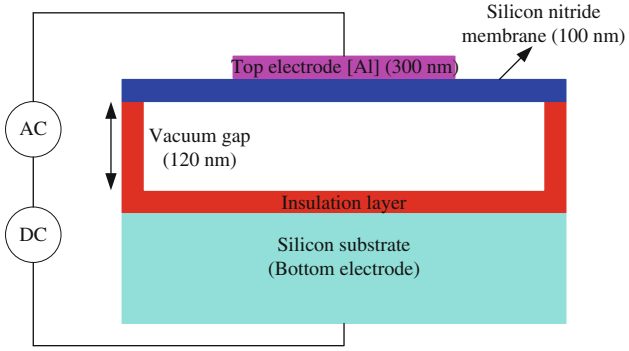

Fig. 3 Cross sectional view of the CMUT [32]

Table 1 Typical CMUT electrical model parameters

Parameter	Set #1	Set #2	Units
L_a	0.29	0.937	mH
C_a	140	30	fF
R_a	106	159	kW
C_m	60	30	fF
C_p	30	25	fF

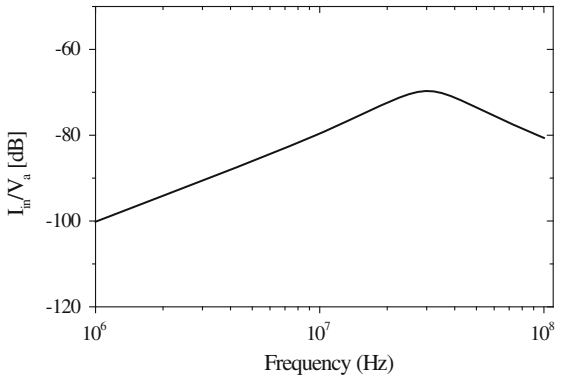

Fig. 4 I_{in}/V_a versus frequency for 52 CMUT elements connected in parallel (set #2 in Table 1)

In the CMUT electrical equivalent circuit shown in Fig. 2, R_a is the acoustic resistance, C_a is the acoustic capacitance, L_a represents the mass of the membrane and some mass effect of the water outside the membrane, C_m is the electrostatic capacitance of the CMUT element, and C_p is the parasitic capacitance between the CMUT–CMOS interconnection node and the small signal ground, dominated mainly by the interconnect parasitics. Here, V_a is an electrical voltage generated by an incoming acoustic wave. For noise analysis, V_a is replaced by a noise source representing the thermal noise of R_a.

Figure 4 shows I_{in}/V_a versus frequency when 52 CMUT elements are connected in parallel for the second set of CMUT parameters shown in Table 1. It can be observed from this figure that there is a centre frequency of 30 MHz with a bandwidth of 30–45 MHz.

2.2.3 *Analysis of charge sampling amplifier*

Figure 5 shows the timing of the signals on switches S_1 and S_2 for the CSA shown in Fig. 2. The timing of the signal on switch S_3 inverts to the timing of the signal on switch S_1. According to the timing of the signals on switches S_1, S_2, and S_3 shown in Fig. 5, there are three phases (reset, integration, and hold) in the operation of the CSA.

The three phases are explained in detail below.

(i) *Reset phase:* each clock period starts with this phase. During this phase, switch S_1 is switched off, switch S_2 is switched on, and voltage across the feedback capacitor C_f is set to zero.

(ii) *Integration phase*: During the integration phase, switch S_1 is switched on and switch S_2 is switched off. This configures the circuit into a transimpedance amplifier with the input signal current as the signal source and C_f as feedback capacitance. During this phase, the input current i_{in} is integrated on C_f and provides an output voltage that is proportional to the integral of the input current.

(iii) *Hold phase*: During the hold phase, both switches S_1 are S_2 are switched off. The integrated signal during the integration phase on the feedback capacitor C_f is held constant during this phase.

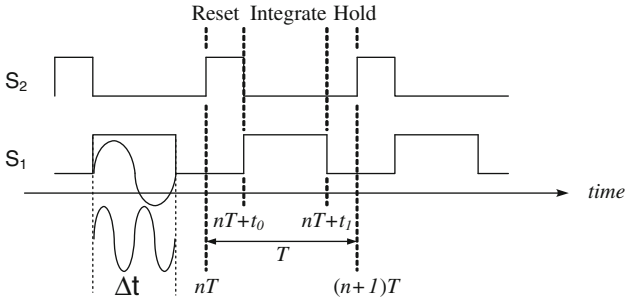

Fig. 5 Timing of the switches S_1 and S_2

To evaluate the performance of the CSA with the CMUT serving as a signal source (see Fig. 2), a time domain transient analysis is performed in ELDO (Mentor Graphics) [33] by using ideal circuit blocks (OTA and switches) with and without switch S_3 (see Fig. 2) at a sampling clock frequency of 125 MHz (1.5 ns for the reset phase, 5 ns for the integration phase, and 1.5 ns for the hold phase). Here, OTA is modelled with an open loop gain of 40 dB and switches are modelled with an on-resistance of 1 kΩ. The model parameters tabulated in Table 1 are used for the CMUT electrical equivalent circuit parameters shown in Fig. 2.

Figure 6 shows the transfer gain from the CMUT signal source, V_a, to the output of the CSA (see Fig. 2) by varying the input signal frequency and keeping the clock frequency at 125 MHz for both cases with and without switch S_3 as shown in Fig. 2. It can be seen from Fig. 6 that the transfer function from the CMUT signal source V_a to the output of the CSA is the sinc function as discussed in [20, 21, 25–27, 30, 31]. As reported in [20, 21, 25–27, 30, 31], the 3 dB bandwidth of the CSA (with switch S_3) transfer function is $(0.44/\Delta t)$. Here Δt is the pulse width of the timing wave of switch S_1 and is the same as the integration (or charging) time. Unlike in conventional voltage sampling, a 3 dB bandwidth in charge sampling is independent of process parameters or any component values in the circuit. It can

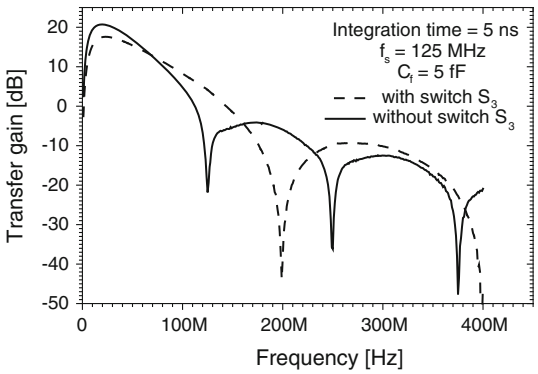

Fig. 6 Transfer gain from the CMUT signal source to the output of the CSA versus input signal frequency with and without switch S_3

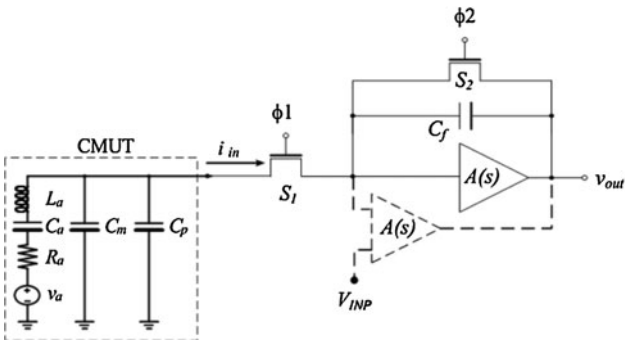

Fig. 7 A simple Charge Sampling Amplifier (CSA) based on a single-ended amplifier and based on an OTA (*dotted lines*)

easily be modified simply by changing the clock frequency and/or integration time (Δt).

It is clear from Fig. 6 that the transfer gain is higher when switch S_3 is not there in the circuit shown in Fig. 2. This is quite intuitive, as for the circuit topology with switch S_3 (see Fig. 2), during the reset phase (switch S_1 switched off and switch S_2 switched on), switch S_3 is switched on and the signal has a conducting path to ground. But when switch S_3 is not there in the circuit shown in Fig. 2, during the reset phase, the charge is integrated on the parasitic capacitance, C_p. As soon as the CSA enters the integration phase from the reset phase, the charge integrated on C_p during the reset is transferred onto the feedback capacitor, C_f. Thus for the circuit without switch S_3 shown in Fig. 2, the total accumulated charge on the feedback capacitor, C_f, is higher compared to the circuit with switch S_3 shown in Fig. 2 and so is the transfer gain.

It can also be observed from Fig. 6 that charge sampling (with switch S_3) has zeros in the transfer function at an integer multiple of $1/\Delta t$, as the accumulated charge on the feedback capacitor is zero at these input signal frequencies (see Fig. 5). On the other hand, charge sampling (without switch S_3) has zeros in the transfer function at an integer multiple of the sampling frequency. A dip in the transfer function around DC can be observed in Fig. 6 and it can be intuitively understood that the input current is blocked by the capacitor, C_a, for DC input, and hence the integrated charge on the feedback capacitor is almost zero if there is no leakage. The circuit topology without switch S_3 in Fig. 2 has better performance in terms of transfer gain and attenuates out of band signals much more effectively compared to the circuit with switch S_3 shown in Fig. 2. Because of the benefits associated with the circuit without switch S_3 in Fig. 2, it has been chosen to be implemented in 90 nm CMOS technology as an analog front-end for CMUTs.

2.2.4 *Proposed self-biased CSA*

Figure 7 shows the self-biased CSA based on a single-ended amplifier topology. If the single-ended amplifier block is replaced with an OTA then it becomes regular CSA which is based on an OTA. There are some advantages to using this single-ended topology over the regular topology as explained below.

From Fig. 7, it can be observed that the regular CSA based on an OTA requires an additional biasing voltage at the positive input of the OTA; on the other hand the proposed single-ended (self-biased) CSA input will be biased to the output DC voltage during reset mode, hence the name self-biased CSA. But this imposes a requirement to match the DC levels at the input and the output of the amplifier block used in the single-ended amplifier.

3 Design of the single-ended transimpedance amplifier and self-biased CSA in 90 nm CMOS

For the intended application [12], the front-end amplifier is required to have a transfer gain of 20 dB (here from the CMUT signal source to the output of a single-ended transimpedance amplifier or output of a self-biased CSA) as the signals generated from CMUTs have an amplitude of 20 mV. To achieve this transfer gain, the amplifier block should have high gain (45 dB and above) and high unity gain frequency (around 1 GHz) at 100 fF load capacitance, which is assumed to be the input capacitance of the following stage.

For the single-ended transimpedance amplifier topology, there is a design requirement to match the DC levels at the input and output of the amplifier. The proposed self-biased CSA shown in Fig. 7 is designed to operate at 125 MHz clock frequency and is required to have a slew rate of 333.3 V/μs if the reset phase is 1.5 ns and the CSA output peak-to-peak amplitude is 500 mV. As the output DC voltage will be dynamically biased at the input during

every reset phase of the CSA, there is also a design requirement to match the DC levels at the input and the output of the amplifier block used in the proposed self-biased CSA.

To meet the above design specifications for the amplifier block, a folded cascode topology based on an inverter shown in Fig. 8 is chosen [30, 34].

The inverter-based folded cascode amplifier [30, 34] is a slightly modified version of a conventional folded cascode amplifier. As shown in Fig. 8, the transistor Msb will not be there in an ordinary folded cascode amplifier, and thus transistor M10 would sink the biasing current for the input transistor Mi. Hence M10 would be a large device compared to M6–M9, depending on the biasing current of Mi. With the introduction of Msb in the proposed amplifier, M10 is designed as a nominal device with the same dimensions as M6–M9. Now the additional NMOS transistor Msb connected to Mi forms a CMOS inverter amplifier. Hence, as opposed to a common-source amplifier feeding a common-gate amplifier for a conventional folded cascode circuit [34], the proposed amplifier is actually a CMOS inverter feeding a common-gate amplifier [30]. It is easy to match the DC levels at the input and the output of this amplifier topology [30, 34] and it is essential for both of the proposed ultrasound analog front-ends.

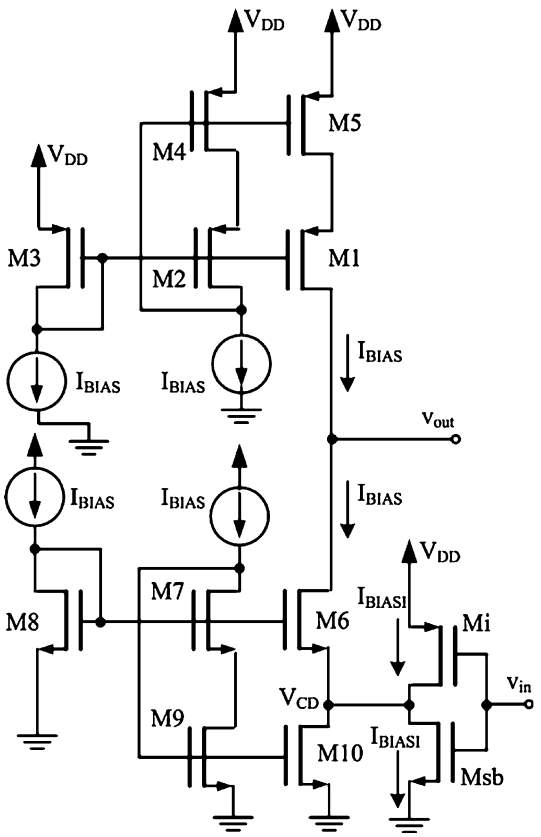

Fig. 8 Schematic of an inverter-based folded cascode amplifier

The inverter-based folded cascode amplifier has some advantages as explained below in detail.

1. Area advantage. For the folded cascode amplifiers, M10 turned out to be a very wide device (around five times the width of M6–M9). On the other hand, in the proposed amplifier, Msb is a very small device and M10 is a nominal device with the same dimensions as M6–M9.
2. Power consumption advantage. Since M10 is a very wide device in a folded cascode configuration, a larger amount of current would be needed through the cascode transistors to keep its drain voltage high enough to keep it in the active region.
3. Gain advantage. Using the inverter-based circuit with a similar input bias current resulted in a slightly higher gain (1–2 dB).
4. Ease in adjusting the Unity Gain Frequency (UGF) of the amplifier. It is easy to adjust the input transconductance (gmi + gmsb) without affecting the output resistance, and hence small adjustments in gain as well as in UGF could be made without affecting the amplifier bandwidth.

However, there are also some trade-offs in the proposed scheme as explained below.

1. Spread in input bias current. As the output DC voltage is biased at the input node, fluctuations in the output DC voltage cause a spread in the input bias current.
2. Lower Power Supply Rejection (PSR).

As 52 CMUT elements were connected in parallel, both the single-ended amplifier and the self-biased CSA have been designed accordingly, and hence the inverter-based amplifier block was also designed accordingly. It achieves an open-loop dc gain of 45 dB, a unity gain frequency of 1.5 GHz, and a phase margin of 66 degrees at a power consumption of only 433.5 μW under a slow-slow process corner defined in 90 nm CMOS technology. The chip layout and micro-photograph are shown in Fig. 9.

Switches (S_1 and S_2 as shown in Fig. 7) were designed as transmission gates as not only do they minimize any charge injection but also the use of transmission gates makes the switches have almost constant on-resistance throughout the operating voltage range (0.25–0.75 V). No charge injection at the output of the CSA was observed either in simulations or in measurements.

4 Measurement results and discussion

4.1 Single-ended transimpedance amplifier

In this section, we present the simulation and measurement results of the single-ended transimpedance amplifier. It is

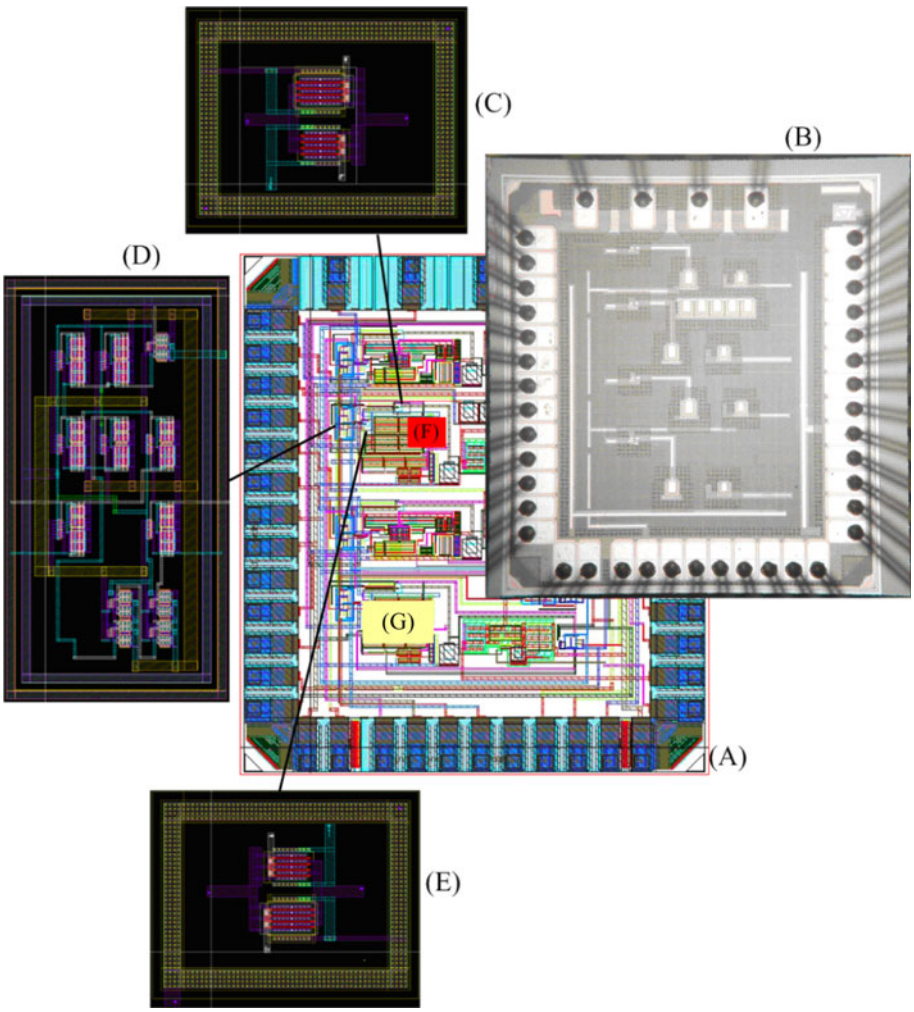

Fig. 9 Chip details: *A* chip layout, *B* chip micro-photograph, *C* feedback switch (S_2) for CSA, *D* clock generator, *E* input switch for CSA (S_1), *F* inverter-based folded cascode amplifier, and *G* single-ended transimpedance amplifier. Chip dimensions are 1230.56 μm × 1377.84 μm

characterized with a source resistance of 3.3 kΩ, which is nearly the same as the source resistance of 52 CMUT elements connected in parallel (∼3 kΩ for set #2 CMUTs in Table 1). An input coupling capacitance of 1 nF is used. Amplifier will be connected to CMUTs as soon as they are ready. To account for the parasitics on printed circuit board (PCB), 1 pF capacitance was used at the both ends of the 1 nF coupling capacitor and 2 pF capacitance was used at the both ends of the feedback resistor in simulations.

Figure 10 shows the gain versus input signal frequency from the signal source to the output of the transimpedance amplifier. It can be observed from this plot that it achieves a measured voltage gain of 19 dB at the centre-frequency of 30 MHz, which is a little higher than the simulated gain of 17.04 dB due to the parasitics that showed up from the off chip feedback resistor, parasitics that aroused from layout. Differences between the measurements and simulations are due to the various parasitics from PCB as well as parasitics from layout at different nodes in the circuit.

It was also observed from the measurements that it shows an output noise power spectral density of

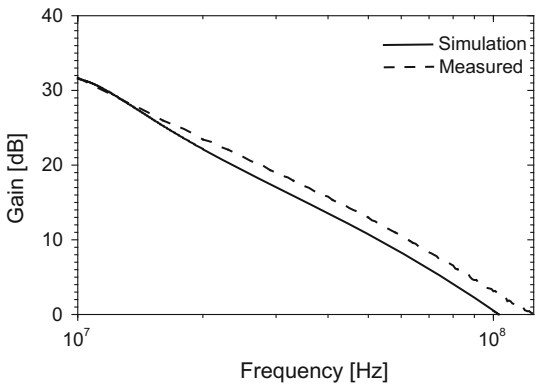

Fig. 10 Gain versus input signal frequency

0.042 (μV)/SQRT(Hz) at a centre-frequency of 30 MHz. Differences between simulation and measurement results are quite intuitive and understandable due to the parasitic capacitances that arise from the layout, and parasitic capacitances that arise from the off chip feedback resistor.

Table 2 presents a summary of the main performance parameters for both simulations and measurements.

From the distortion measurements, it shows a total harmonic distortion of −23 dB at 450 mV p–p output voltage and 30 MHz input signal frequency, which is a little more when compared to the simulated one because of the difference in output DC voltage between the simulation and measurements. The area measured only about 32 μm × 32 μm per amplifier. There is a considerable area and power reduction compared to the design presented in [18] for similar applications.

4.2 Self-biased CSA

In this section, the measured results of the self-biased CSA are discussed. It is characterized with a signal source resistance of 2.7 kΩ, which is nearly same as the source resistance of 52 CMUT elements connected in parallel (∼3 kΩ for set #2 CMUTs in Table 1), and an input coupling capacitance of 10 nF (to isolate the DC bias conditions from the amplifier side) is connected in series with source resistance as the CMUTs are not yet ready to be interfaced. Both of the components are placed on PCB. A parasitic capacitance value of 1 pF is used in simulations at both ends of the coupling capacitor to account for the parasitics that arises from the coupling capacitor. A feedback capacitance of 156 fF is used in the designed CSA for 52 CMUT elements.

Transfer gain is measured at 50 MHz clock frequency with the signal source discussed above. Figure 11 shows the transfer gain for both the measured and simulated cases from Va (from the bottom of the source resistance) to V_{out} of the CSA versus input signal frequency at a sampling frequency of 50 MHz.

It can be observed from this figure that the measured transfer gain is in close agreement with the simulated one. The slight difference between the measured transfer gain and the simulated one can be understood due to various parasitic capacitances that were not accounted for in simulations, for example layout parasitics and parasitics on the PCB at various nodes. It can also be observed from this figure that the transfer function has zeros at the sampling frequency and at an integer multiple of the sampling frequency in both simulated and measured cases. This is

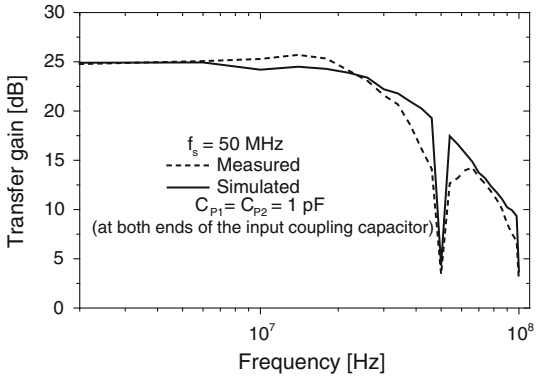

Fig. 11 Transfer gain of the self-biased CSA at 50 MHz sampling frequency

expected and quite intuitive, because as discussed in the previous sections the accumulated charge across the feedback capacitor, C_f, is zero when the input signal frequency is equal to the sampling frequency or an integer multiple of the sampling frequency.

Figure 12 shows the measured and simulated transfer gain from Va (bottom of the source resistance) to Vout at a sampling clock frequency of 100 MHz with the same signal source (2.7 kΩ source resistance and 10 nF coupling capacitor) as discussed previously.

From Fig. 12 it can be noted that the proposed self-biased CSA achieves a transfer gain of 17.4 dB at the input signal frequency of 30 MHz. It consumes 586 μA per amplifier from a 1 V power supply. The measured noise performance is shown in Fig. 13. Noise is measured at the output node of the CSA by grounding the input source. As can be observed from this figure, there is a total noise (which includes not only the hold phase but also the reset and integration phases) of −47.5 dBm in the bandwidth of 15–45 MHz at a sampling frequency of 100 MHz. This noise includes the noise from the amplifier block, switches, and input source resistance. This total noise is equivalent to an SNR ratio of 45.7 dB at a peak-to-peak output signal amplitude of 500 mV.

The performance of the self-biased CSA is compared with recently reported similar sampling architectures [23, 28, 29] and the results are summarized in Table 3. The

Table 2 Summary of the performance parameters

Parameter	Simulated	Measured	Units
Gain at 30 MHz input signal frequency	17.04	18.90	dB
Output noise PSD at 30 MHz	0.00386	0.00177	$(\mu V)^2$/Hz
Noise power in the pass—band (15 MHz–45 MHz)	0.1941	0.0665	$(mV)^2$
THD at full scale output (450 mV p–p) at 30 MHz	−26.99	−23.16	dB
Current consumption from a 1 V power supply	598		μA per amplifier
Area	32.4 μm × 32.4 μm		Per amplifier

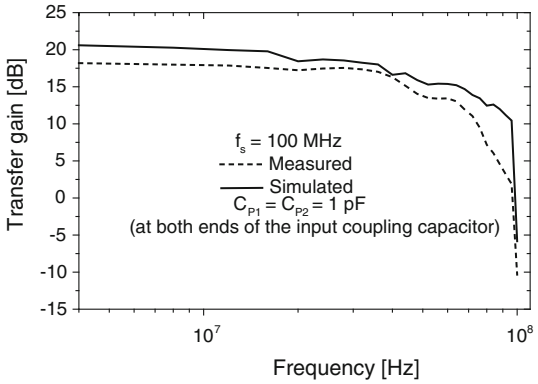

Fig. 12 Transfer gain of the self-biased CSA at 100 MHz sampling frequency

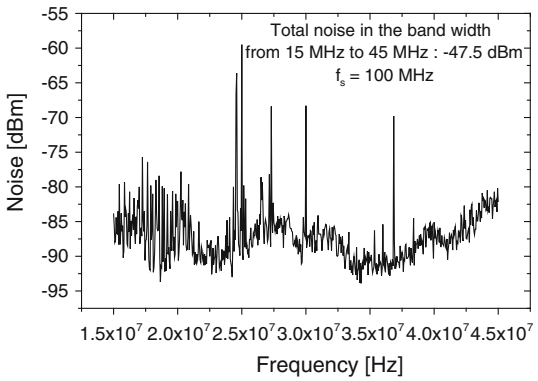

Fig. 13 Measured noise at the output of the self-biased CSA at 100 MHz sampling frequency

proposed CSA designed in state-of-the-art 90 nm CMOS technology has an area advantage over reported sampling architectures [23, 28, 29] which were designed in 0.35 and 0.6 μm CMOS technology. It can be noted from this table that the proposed CSA consumes only 586 μA per amplifier from a 1 V power supply, which is very small compared to the power consumption of the sampling schemes reported in [23, 28, 29]. The proposed CSA achieves an SNR of 45.7 dB and is better than the one reported in [29].

5 Conclusion

From the measurement results we conclude that the single-ended transimpedance amplifier designed in 90 nm CMOS achieves a voltage gain of 19 dB, an output noise power spectral density of 0.042 (μV)/SQRT(Hz) at a centre-frequency of 30 MHz, and a total harmonic distortion of −23 dB at 450 mV p–p output voltage and 30 MHz input signal frequency. It draws only 598 μA current per amplifier from a 1 V power supply and occupies only 32 μm × 32 μm per amplifier in 90 nm CMOS technology.

The proposed self-biased sampling scheme does not require an additional biasing voltage compared to a conventional charge sampling scheme based on an OTA. The concept of the charge sampling is proved by making measurements in the time domain and observed zeros in the transfer function as intuitively expected at the sampling frequency and at an integer multiple of the sampling frequency. The proposed sampling scheme for ultrasound front-ends will further enable ADCs to be directly integrated with the ultrasound sensors (CMUTs) to enhance the overall performance of ultrasound systems. From the measured results, the self-biased CSA achieves a transfer gain of 17.4 dB at an input signal frequency of 30 MHz and at a sampling clock frequency of 100 MHz. It consumes 586 μA per amplifier from a 1 V power supply. It achieves an SNR ratio of 45.7 dB at a peak-to-peak output signal amplitude of 500 mV and a sampling frequency of 100 MHz. It occupies an area of 1470.2 μm^2 (which is equivalent to 38 μm × 38 μm), which also includes the area of the switches for the CSA that will be used for the single CMUT element in 90 nm CMOS technology. The clock generator occupies an area of 92.5 μm × 49.9 μm and the switches occupy an area of 16.45 μm × 12.78 μm each. The switches will become smaller when they are scaled to be used in a CSA with a single CMUT element. The performance of the self-biased CSA designed in state-of-the-art 90 nm CMOS technology is compared with recently reported similar sampling schemes.

Table 3 Comparison of the proposed CSA with other reported sampling schemes

	This work	[23]	[28]	[29]
Sampling scheme employed	Charge sampling	Charge sampling	Voltage domain	Current domain
Technology	90 nm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.6 μm CMOS
Power supply	1 V	3.3 V	3.3 V	1.5 V
Sampling frequency	100 MHz	1.85 MHz	150 MHz	30 MHz
Input signal frequency	15–45 MHz	100 MHz	70 MHz	15 MHz
SNR	45.7 dB	66 dB (SFDR)	65 dB (SFDR)	45 dB
Power consumption	586 μW per amplifier @ 1 V	30 mW @ 3.3 V	70 mW @ 3.3 V	2.3 mW @ 1.5 V

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