A high dynamic range ultralow-current-mode amplifier with pico-ampere sensitivity for biosensor applications

Lei Zhang · Zhiping Yu · Xiangqing He

Abstract A novel ultralow-current-mode amplifier (ULCA) serving for on-chip biosensor signal pre-amplification in the integrated biosensing system (IBS) has been presented and verified in SMIC 0.18 µm CMOS technology by elaborately considering gain, bandwidth, noise, offset, and mismatch. The proposed ULCA solved the noise, bandwidth, and current headroom dilemma in the reported works, and can completely satisfy the specifications of IBS. It provides a current gain of 20 dB, 3 dB bandwidth of 7.03 kHz and input dynamic range of 20 bit, with only 1 nA of DC quiescent current, while the input offset current and noise current are less than 16.0 pA and 4.67 pArms, respectively.

Keywords Integrated biosensing system (IBS) · Ultralow-current-mode amplifier (ULCA) · Subthreshold · Noise · Mismatch

1 Introduction

Biomedical technology emerges since the past century and is believed to be one of the most promising industries in the 21st century together with micro and nano-electronics industries. Recently, DNA molecule based biosensors are being reported by many famous literatures [1–3]. Naturally, the integrated biosensing system (IBS) which monolithically integrates the biomedical sensor arrays and ASICs such as ultralow-current-mode amplifier (ULCA), ADC, and DSP in a single chip is avidly expected to be

L. Zhang (✉) · Z. Yu · X. He
Institute of Microelectronics, Tsinghua University, Beijing 100084, People's Republic of China
e-mail: zl99@mails.tsinghua.edu.cn

realized to greatly reduce the cost of common sensors used in the hospitals and markets. Actually, the proposed sensing schemes implemented on silicon-nanowire and golden surface [2, 3] are inherently compatible with modern CMOS process, however, the fastidious requirements as summarized in Table 1 of ultralow-current-mode operation and sensitivity (nA or sub-nA) for the following stages of ICs make great challenges to analog IC designers. Obviously, conventional transistor–saturation-based current-mode circuits are out of consideration due to the large noise background induced by the DC quiescent current and subthreshold-based current-mode circuits emerge to be the candidates [4, 5].

It is well known that since the subthreshold current appears an exponential function of the gate voltage in MOSFET, subthreshold circuits suffer from power fluctuations and process fluctuations between die to die seriously. Fortunately, they suffer little fluctuations on the same die [6] which makes it possible to realize ultralow-current-mode circuits by integrating all the circuit modules on a single chip [7, 8].

Some ULCA topologies have been reported in literatures [9–11], as shown in Fig. 1. The circuit in Fig. 1(a) uses a regulated current mirror to achieve current amplification whose quiescent currents are provided by current sources, while the bandwidth is limited by capacitor C0. However, since quiescent current I0 should be low enough to reduce the noise level and meet the requirement of sensitivity, the required current headroom (in both push and pull directions) can hardly be achieved. One can certainly use the complimentary topology in Fig. 1(b) to meet the headroom requirement and increase sensitivity by removing noise background introduced by quiescent current I0, however, at the cost of losing bandwidth on the low input cases.

Table 1 Specifications of integrated biosensor

DNA releasing voltage	0.9 V
DNA modulation voltage	±0.4 V
Current headroom	±100 nA
Current sensitivity	∼100 pA
Max. signal bandwidth	6 kHz
Dynamic range	10 bit
Temperature range	10–40°C

To meet the specifications in Table 1, in this paper, a ULCA in achieving biosensing pre-amplification purpose has been proposed, characterized and verified by using SMIC 0.18 μm CMOS mixed signal technology. The results show that proposed ULCA can completely satisfy the requirements of IBS application, which makes it a promising candidate for the purpose of pre-amplification of biosensor signals.

2 Circuit descriptions

The proposed topology of ULCA has been shown in Fig. 2. In this circuit, the current from DNA biosensors is input to a complimentary regulated current mirror composed of N type opamp AN0, P type opamp AP0, and transistor M0, M1, M3, M4, where it is amplified by a factor of 10 (20 dB). Opamp AN1, AP1, and M6–M11 compose a voltage limiter. Initially, due to the "virtual short" mechanism "in" is fixed at "clamp" by AN0 and AP0, and a quiescent current of I_{ref} is constructed in M0 and M3 by AN1 and AP1. When a push input is applied, V_{vn} comes down and so does the output of opamp AN1, thus turns off M2, and the current of M0 and M1 is being sinked by AP0, on the other hand, since V_{vp} is also prone to decrease, current provided by AN0 become smaller, while M5 is turned on by AP1 and compensates the current at node "vp", which limits V_{vp} from decreasing and assures the quiescent current of M0 and M3 exactly equals to the reference current I_{ref} provided by M6–M9 even if the input current I_{in} is much larger than the quiescent current I_{ref}. Similar conclusion can also be made for the pull input cases. It can be seen that M2 and M5 alternatively sustain a quiescent current of I_{ref} for the input current mirror, which in turn keeps a constant bandwidth when input varies between push and pull (positive and negative) directions. Furthermore, I_{ref} can be designed small enough to achieve

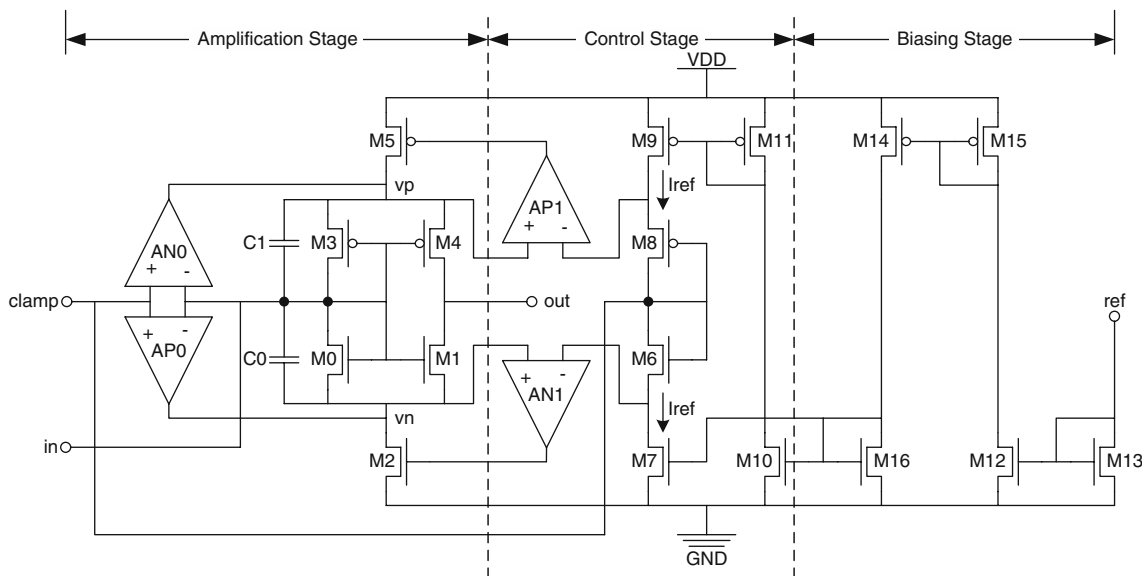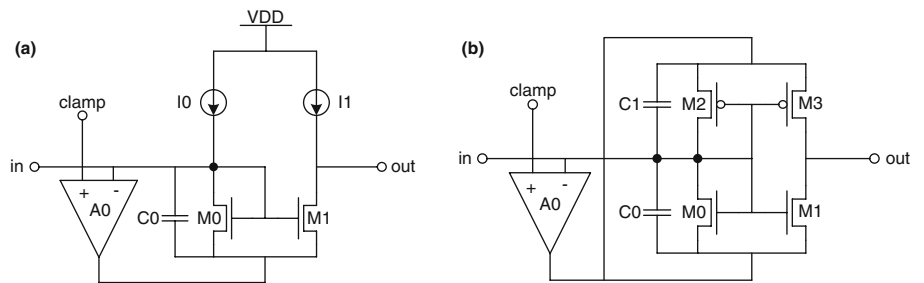**Fig. 1** Conventional ULCA topologies

Fig. 2 Circuit diagram of proposed ULCA

the required sensitivity and noise level without restricted by the current headroom any more, since the current headroom is no longer depending on the magnitude of quiescent current of the input stage in the proposed ULCA. Therefore, the circuit can provide an extremely high sensitivity and large current headroom at the required bandwidth. Due to the variation and pad leakage issues, I_{ref} is unpractical to be provided off-chip. Therefore, in the design, the biasing stage composed of three steps of current mirroring (each step achieves a conversion factor of 0.1) realized by M12–M16 is introduced, from which a μA off-chip current is down converted by 1,000 times, thus relaxing these unwanted impacts. Capacitors C0 and C1 serve for frequency compensation and bandwidth confinement purposes in the circuit.

The topologies of auxiliary N and P type opamp are shown in Fig. 3(a) and (b). In the circuit, M0, M1, M3, and M4 compose a differential input stage, and are chosen as large dimensions to improve matching and reduce offset, meanwhile, they are biased in their subthreshold regions for the purpose of noise reduction. Transistor M5 and M6 compose a trans-conductance output stage providing current for the following circuits. Capacitor Cn and Cp are serving for frequency compensation in the circuit, thus ensuring the AC stability.

3 Circuit analysis

As found from Fig. 2, when a push input is applied, the conversion gain is provided by regulated current mirror composed of M0, M1, and opamp AP0, while M3–M5 and opamp AP1 are serving as current sources providing the quiescent current for the stage, which can be simplified to the circuit shown in Fig. 4(a). Complimentary discussion of the pull input case leads to the topology shown in Fig. 4(b).

3.1 AC small signal analysis

The small signal equivalent circuit for AC analysis is shown in Fig. 4(c). In this circuit, the trans-conductance of opamp is modeled as $g_{ma}(s)$ considering delays introduced
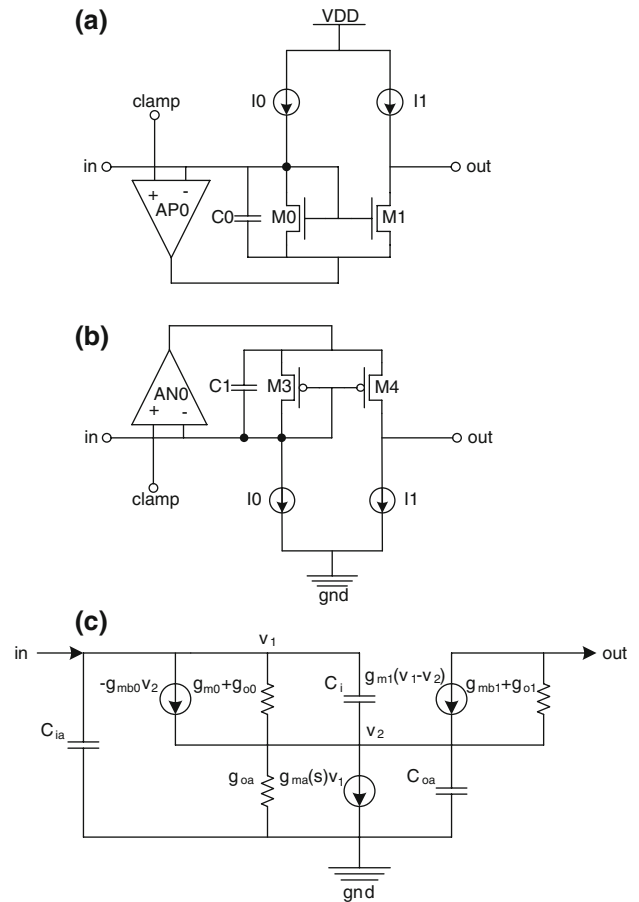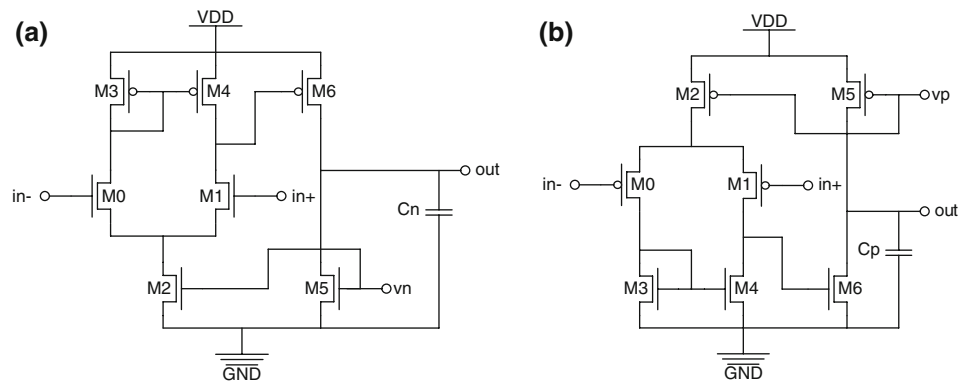

Fig. 4 a Simplified circuit of ULCA when a push input is applied. b Simplified circuit of ULCA when a pull input is applied. c Small signal equivalent circuit of simplified ULCA

Fig. 3 a The auxiliary N type opamp. b The auxiliary P type opamp

by parasitic capacitances of its internal nodes. As suggested by [12], $g_{ma}(s)$ can be written as:

$$g_{ma}(s) = g_{ma}\left(1 - \frac{s}{\omega_a}\right) \tag{1}$$

where g_{ma} is the DC trans-conductance and ω_a models the delay.

Detailed analysis of the equivalent circuit results in the characterization function of $as^2 + bs + c = 0$, where:

$$a = C_{ia}(C_i + C_{oa})\omega_a + C_i\left(C_{oa} - \frac{g_{ma}}{\omega_a}\right)\omega_a \tag{2}$$

$$b \approx C_{ia}(g_{m0} + g_{m1} + g_{oa})\omega_a$$
$$+ (g_{m0} + g_{o0})\left(C_{oa} - \frac{g_{ma}}{\omega_a}\right)\omega_a \tag{3}$$

$$c \approx g_{mb0}(g_{ma} - g_{m1})\omega_a + g_{m0}(g_{mb1} + g_{oa} + g_{ma})\omega_a \tag{4}$$

and the parameters are defined as follows:

C_{ia}: Input capacitance of opamp.
C_{oa}: Output capacitance of opamp (C_n or C_p).
C_i: $C_{gs0} + C_{gs1} + C_0$ (or C_1).
g_m: Trans-conductance of MOSFET.
g_{mb}: Body trans-conductance of MOSFET.
g_o: Output conductance of MOSFET.
g_{oa}: Output conductance of opamp.

In order to maintain the AC stability, $a > 0$, $b > 0$, and $c > 0$ must be satisfied, resulting in the conditions of $g_{ma} > g_{m1}$ and $C_{oa} > g_{ma}/\omega_a$. Moreover, it can be found that provided the quiescent current I_{ref}, by adjusting the capacitance of C0 and C1, the bandwidth of proposed ULCA can be confined at the expected value.

3.2 Noise characterization

Generally, three kinds of noises are considered in CMOS circuit: thermal noise and shot noise, which are white noise, and flicker noise or 1/f noise. According to the subthreshold noise characterization in [6, 7] and the discussions in [11], the low frequency noises (flicker noise and some low frequency components of white noise) are being substantially canceled in the input node due to the quiescent current substraction and the symmetrical topology, resulting in that white noise appears more remarkable than flicker noise over the required bandwidth. Furthermore, white noise in the subthreshold MOSFET is basically contributed by shot noise, and the noise power density is given by: $S_I = 2qI$, where I is the DC current and q is the unit charge [6, 7].

The noise performance of proposed ULCA can be characterized by two noise sources, "vn" and "in" with the corresponding power densities of S_{vn} and S_{in}, which can be calculated as usual: by evaluating the output noise current with input open or shorted to ground and dividing by the gain. Meanwhile, considering the practical noises from V_{clamp} and I_{ref} sources, the simplified expressions are reported as:

$$S_{in} = 4qI_{ref}\left(1 + \frac{1}{A}\right) + 4kTM^2 G_S \tag{5}$$

$$S_{vn} = \frac{4qAI_{ref} + 4kTM^2 A^2 G_S}{g_{ma}^2} + 2S_{va} + 4kTR_S \tag{6}$$

where A is the current gain, S_{va} is the input–referred noise power density of opamp, $M = 0.001$ is the conversion factor of biasing current mirrors, R_S and G_S represent the source resistance and conductance of the voltage and current sources, k and T are the Boltzman constant and absolute temperature, respectively. In practical implementation, the values of R_S and G_S are 50 Ω and $<10^{-7}$ s, and the noise voltage and current from the sources over the specified the bandwidth are 76 nVrms and 3.4 fArms, much smaller than the typical noises of opamp and transistors in the application, thus being insignificant for the overall noise performance. From (5) and (6), S_{in} and S_{vn} can be reduced by decreasing the input–referred noise of the opamp and the quiescent current I_{ref}, however, trading with the power consumption and the bandwidth of ULCA.

4 Verification and discussion

The proposed ULCA is verified by using SMIC 0.18 μm CMOS mixed signal technology over the specified temperature range of 10–40°C at all process corners of TT, FF, SS, FS, and SF. Meanwhile, mismatching issues are also analyzed by Monte Carlo simulations over 30 different samples.

As stated in Sect. 3, the DC quiescent current of ULCA comes from the trade-off between noise and bandwidth requirement. From the simulation, the optimized quiescent current is given as $I_{ref} = 1$ nA, transistor channel length is chosen as $L = 1$ μm, and the aspect ratios (W/L) of basic N and P transistor cells are 10 and 20, respectively, while all the capacitances are designed as 1 pF.

4.1 Process corners analysis

Figure 5(a) shows the gain–bandwidth–product (GBW) and input–referred–noise–current (IRNC) as functions of DC input current I_{in} at all process corners, and the data at $I_{in} = 0$ is summarized in Table 2. It can be seen that within an input range of ±100 pA, GBW and IRNC virtually

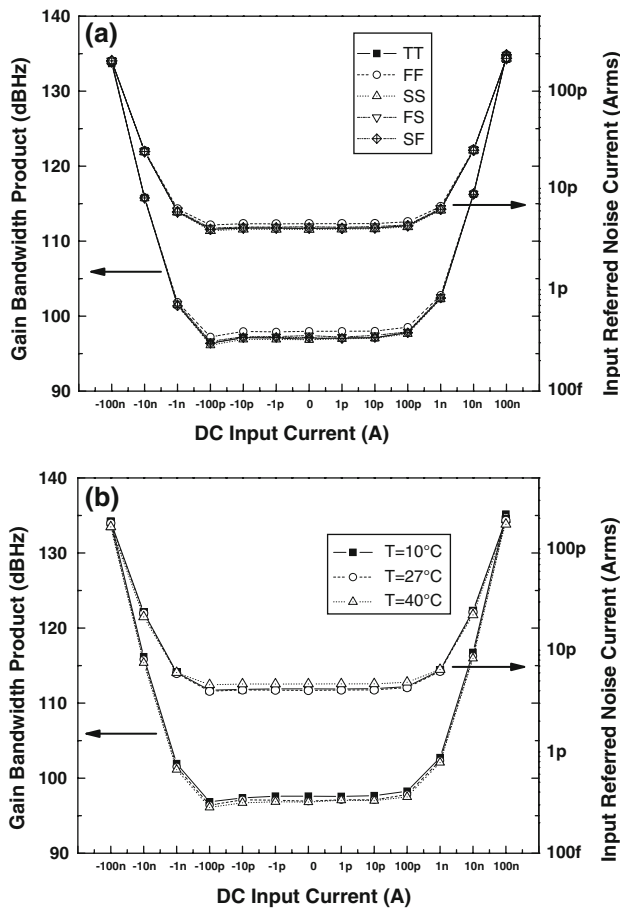the noise level still remains constant, SNR linearly ascends with $|I_{in}|$ to 27.5 ± 0.9 dB. For larger input current, the following equation holds until the input current mirror becomes saturated:

$$SNR \propto \frac{I_{in}}{\sqrt{(I_{in} + I_{ref})B}} \propto \frac{I_{in}}{I_{in} + I_{ref}} \to const. \qquad (7)$$

where B is the bandwidth of the circuit at the input current of I_{in}.

The SNR when the input current mirror becomes saturated can be formulated as follow considering the first order pole of the circuit:

$$SNR \propto \frac{I_{in}}{\sqrt{\sqrt{I_{in}}B}} \propto \sqrt{I_{in}} \qquad (8)$$

Equation (7) suggests that SNR tends to converge before the input current mirror saturates, which indicates that the increase of IRNC does not worsen the SNR. This has been verified by the linear part of IRNC curve in Fig. 5(a) when $|I_{in}| > 1$ nA. The saturation value of SNR is calculated as 54.6 ± 0.3 dB over the five corners. Along with the increase of I_{in}, the input current mirror becomes saturated, and the SNR should follows (8). However, since the second order conjugate pole gradually becomes dominant and extends the bandwidth as suggested by simulation, the increasing of SNR is slower than (8).

4.2 Temperature dependencies

The temperature dependencies of GBW and IRNC as functions of DC input current I_{in} within the specified temperature range of 10–40°C are illustrated in Fig. 5(b), while the data at $I_{in} = 0$ is also summarized in Table 2. It is concluded from Fig. 5(b) that both the GBW and IRNC exhibit slightly larger dependencies on temperature with respect to process corners, and vary around ± 0.4 and $\pm 7.4\%$, respectively, within the required temperature range of 10–40°C.

Similar conclusion can be made for SNR as analyzed in the previous section, the SNR at $|I_{in}| = 100$ pA is 27.2 ± 0.9 dB, and the saturation value of SNR is 55.0 ± 0.8 dB within 10–40°C.

Fig. 5 GBW and IRNC versus DC input current varying from −100 to 100 nA. **a** GBW and IRNC at various process corners. **b** Temperature dependencies of GBW and IRNC of proposed ULCA

remain constant at 96.9 dBHz and 4.02 pArms, respectively, while increase monotonously for larger input levels. The minimal bandwidth is 7.03 kHz, a little bit larger than the specified 6 kHz, and the DC gain holds constantly at 20 dB. Meanwhile, GBW and IRNC are suffering little variations from different process corners, and the relative fluctuations are within ± 0.3 and $\pm 5.5\%$, respectively.

Moreover, for -4.67 pA $\leq I_{in} \leq 4.67$ pA the input current is sinked by the noise floor, and the signal-to-noise-ratio (SNR) is less than 0 dB. When $|I_{in}|$ increases up to 100 pA (the sensitivity level of IBS specification) where

Table 2 Process corners data and temperature characteristics of GBW, 3 dB bandwidth, and IRNC at $I_{in} = 0$

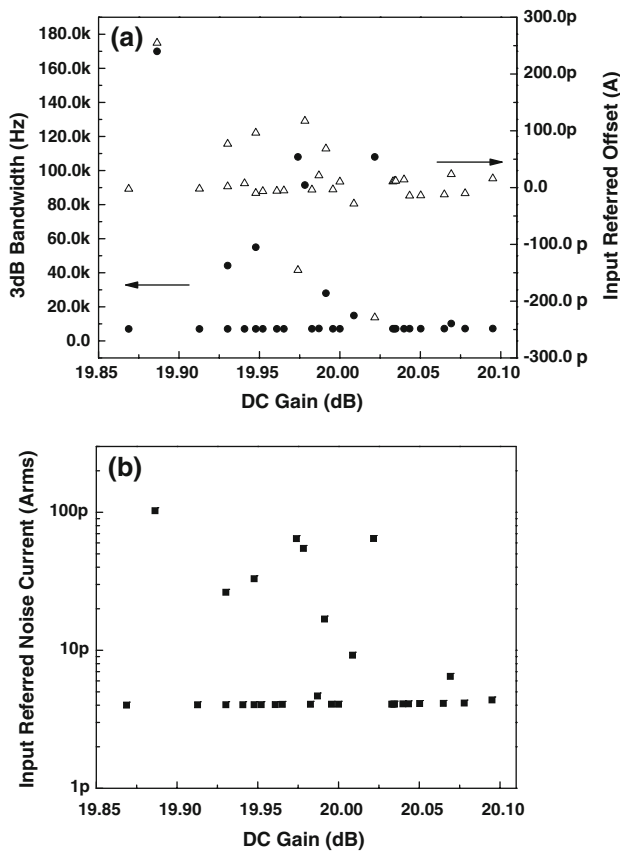|	TT	FF	SS	FS	SF	10°C	27°C	40°C
GBW (dBHz)	96.94	97.99	96.85	97.41	97.13	97.60	96.94	96.86
3 dB bandwidth (kHz)	7.03	7.93	6.96	7.42	7.19	7.59	7.03	6.97
IRNC (pArms)	4.02	4.49	3.94	4.19	4.06	4.17	4.02	4.66

Fig. 6 Monte–Carlo simulation results of DC gain, 3 dB Bandwidth, IRO, and IRNC considering device mismatches. **a** Monte–Carlo simulation of 3 dB Bandwidth and IRO as functions of DC gain over 30 samples. **b** Monte–Carlo simulation of IRNC as a function of DC gain over 30 samples

4.3 Mismatch considerations

In reality, the performances of practical circuit also suffers from process fluctuations due to transistor mismatches. To characterize these impacts, Monte–Carlo simulations on gain, 3 dB bandwidth, input–referred–offset (IRO), and IRNC of proposed ULCA are applied over 30 different

Table 3 Summary of post simulated circuit performances of proposed ULCA

DC gain	20 dB
3 dB bandwidth	7.03 kHz
Phase margin	>90°
Max. output current	0.384 mA
Input referred offset	−14.3 to 16.0 pA
Input referred noise current	4.02 pA
Input dynamic range	>20 bit
DC power dissipation	26.97 μW
Power supply	1.8 V
Layout area	220 μm × 80 μm

samples. According to the design kits of SMIC 0.18 μm CMOS mixed signal technology, the standard deviations σ due to threshold voltage V_T and aspect ratio W/L mismatches are 1.85 mV and 0.5% for the applied transistor dimension. In the simulation, W, L, and V_T are randomly selected within the 3σ range at absolute Gaussian distribution, and are applied to the transistors. The results are shown in Fig. 6. It can be seen that the DC gain distributes from 19.8–20.1 dB, and 21 results of 3 dB bandwidth, IRO, and IRNC within the all 30 samples appear good consistency and randomly distribute in the ranges of 7.03–7.27 kHz, 14.3–16.0 pA, and 4.00–4.67 pArms, while other 9 samples are expressing large deviations.

Specifically, the bandwidth and IRNC deviations are mainly induced by the input–referred offsets V_{off} of opamp AN1 and AP1, and IRO deviation is due to the V_{off} of opamp AN0 and AP0, and mismatches of M0, M1, M3, M4. If the offsets of opamp AN1 and AP1 due to transistor mismatches are as large as hundreds millivolts, the quiescent current of M0 and M3 might considerably differ from I_{ref}, which in turn leads to the large deviations on the 3 dB bandwidth and IRNC. Similarly, if offsets of opamp AN0 and AP0, and mismatches of M0, M1, M3, M4 are considerably large, a large DC output current will be observed in the quiescent state, thus worsening the IRO of the circuit. For further improvement of circuit performances and yield, transistor M0, M1, M3, and M4 in Figs. 2, and 3(a) and (b) have to be carefully laid out or even larger areas are applied to these transistors in the design, however, trading with the bandwidth of the circuit.

The summarized circuit performances from post simulation are listed in Table 3. In the worst case, the input sensitivity is 20.7 pA, which determines the lower rail of input dynamic range, while the higher rail restricted by the maximal input current is 38.4 μA. Therefore, the proposed ULCA is capable of achieving an input dynamic range larger than 20 bit, thus satisfies the IBS specification. The SNR at $I_{in} = 38.4$ μA is 62.3 dB, roughly 10 dB lower than the value following the square-root law in (8) as a result of the second order conjugate pole of the circuit.

5 Conclusion

In this paper, a novel ULCA aiming at the application of signal pre-amplification in the integrated biosensing system has been proposed and verified by using SMIC 0.18 μm CMOS technology. The proposed ULCA can completely satisfy the prescribed specifications of input current headroom, sensitivity, bandwidth, as well as input dynamic range for IBS applications. The proposed ULCA can also be used for ultralow current amplification in other types of

biosensor interfaces, nanoscale device sensing, and optical sensing in the future.

References

1. Gregory Drummond, T., Hill, M. G., & Barton, J. K. (2003). Electrochemical DNA sensors. *Nature Biotechnology, 21*(10), 1192–1199.
2. Li, Z., Chen, Y., Li, X., Kamins, T. I., Nauka, K., & Williams, R. S. (2004). Sequence-specific label-free DNA sensors based on silicon nanowires. *NANO Letters, 4*(2), 245–247.
3. Guiducci, C., Stagni, C., Zuccheri, G., Bogliolo, A., Beninil, L., Samor, B., & Ricc, B. (2002). A biosensor for direct detection of DNA sequences based on capacitance measurements (pp. 479–482). *ESSDERC 2002.*
4. Mead, C. (1989). *Analog VLSI and neural systems*. Reading, MA: Addison Wesley.
5. Zhang, L., He, X., & Yu, Z. (2007). Design and implementation of ultra low current sensing amplifer with pico-ampere sensitivity aiming at bio-sensor applications. *Chinese Journal of Electronics, 2*, 247–251.
6. Linares-Barranco, B., & Serrano-Gotarredona, T. (2003). On the design and characterization of femto-ampere current-mode circuits. *IEEE Journal of Solid-State Circuits, 38*(8), 1353–1363.
7. Linares-Barranco, B., Serrano-Gotarredona, T., Serrano-Gotarredona, R., & Serrano-Gotarredona, C. (2004). Current mode techniques for sub-pico-ampere circuit design. *Analog Integrated Circuits and Signal Processing, 38*, 103–119.
8. O'Halloran, M. O., & Sarpeshkar, R. (2004). A 10-nW 12-bit accurate analog storage cell with 10-aA leakage. *IEEE Journal of Solid-State Circuits, 39*(11), 1985–1996.
9. Serrano-Gotarredona, T., Linares-Barranco, B., & Andreou, A. G. (1999). Very wide range tunable CMOS/bipolar current mirrors with voltage clamped input. *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, 46*(11), 1398–1407.
10. Ramirez-Angulo, J., Carvajal, R. G., & Torralba, A. (2004) . Low supply voltage high-performance CMOS current mirror with low input and output voltage requirements. *IEEE Transactions on Circuits and Systems-II: Express Briefs, 51*(3), 124–129.
11. Steadman, R., Vogtmeier, G., Kemna, A., Quossai, S. E. I., & Hosticka, B. J. (2006). A high dynamic range current-mode amplifier for computed tomography *IEEE Journal of Solid-State Circuits, 41*(7), 1615–1619.
12. Linares-Barranco, B., Rodriguez-Vázquez, A., Huertas, J. L., & Sánchez-Sinencio, E. (1992). On the generation design and tuning of OTA-C high frequency sinusoidal oscillators. *IEE Proceedings of Pt G Circuits, Devices and Systems, 139*(5), 522–528.

Lei Zhang graduated with honors from the Department of Electronic Engineering in Tsinghua University, Beijing, China, in 2003, and received his MS and PhD degrees in Tsinghua University, Beijing, China, in 2008. Recently, he is working as a postdoctoral fellow in University of California, Los Angeles, USA. His research interests cover mixed-signal and radio-frequency integrated circuits, DNA sensor fabrication and characterization, CMOS integrated biosensing system, as well as the design and implementation of neuromorphic circuits and intelligent machines.

Zhiping Yu graduated from Tsinghua University, Beijing, China, in 1967 with BS degree. He received his MS and PhD degrees from Stanford University, Stanford, CA, USA in 1980, and 1985, respectively. He is presently the professor and deputy director in the Institute of Microelectronics, Tsinghua University, Beijing, China. From 1989 to 2002, he has been a senior research scientist in the Department of Electrical Engineering in Stanford University, USA, while serving as the faculty member in Tsinghua. He returned to Tsinghua full time since September 2002 and holds Pericom Microelectronics Professorship (2002–2004) established by Pericom Semiconductor Corp. in San Jose, USA. His research interests include device simulation for nano-scale MOSFETs, quantum transport in nanoelectronic devices, compact circuit modeling of passive and active components in RF CMOS, and numerical analysis techniques.

Xiangqing He received the BS degree from Tsinghua University, Beijing, China, in 1970. She is a Professor in the Institute of Microelectronics, Tsinghua University, Beijing, China. Her research interest focuses on design for analog circuit and memory.