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A 3 V 110 μW 3.1 ppm/°C curvature-compensated CMOS bandgap reference

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Abstract This paper presents design of a high-precision curvature-compensated bandgap reference (BGR) circuit implemented in a 0.35 μm CMOS technology. The circuit delivers an output voltage of 1.09 V and achieves the lowest reported temperature coefficient of ~3.1 ppm/°C over a wide temperature range of [−20°C/+100°C] after trimming, a power supply rejection ratio of −80 dB at 1 kHz and an output noise level of 1.43 μV $\sqrt{\text{Hz}}$ at 1 kHz. The BGR circuit consumes a very low current of 37 μA at 3 V and works for a power supply down to 1.5 V. The BGR circuit has a die size of 980 μm × 830 μm.

Keywords Bandgap reference · CMOS · Temperature coefficient · Power supply rejection ratio

1 Introduction

Bandgap Reference (BGR) circuits are basic functional circuit blocks widely used in many integrated circuit (IC) chips, such as, power management, temperature sensors, data converters, voltage regulators and memories, because of its excellent temperature stability and insensitivity to supply voltage. Since introduced in 1970s, BGR has been the most popular solution for precision reference source circuits. The basic idea of BGR in CMOS technology is to add a proportional to absolute temperature (PTAT) voltage to the emitter-base voltage (V_{EB}) of a parasitic pnp transistor, so that the first-order temperature dependency in V_{EB} is compensated by the PTAT voltage, resulting in a nearly temperature-independent output voltage. Typical output voltage of BGR is about 1.2 V at room temperature, which is close to the bandgap voltage of silicon. However, for conventional BGR circuits, the higher-order temperature dependency in V_{EB} still exists in output voltage. In order to further lower the temperature coefficient (TC), several curvature compensation schemes [1–4] have been reported to compensate the higher-order temperature dependency and to reduce the output voltage variation over the temperature.

This paper presents design of a current-mode curvature-compensated BGR fabricated in a commercial 0.35 μm CMOS technology. Several design issues were carefully studied to optimize the critical BGR specifications, such as temperature coefficient, power supply rejection ratio (PSRR) and power consumption. Section 2 explains the design details. Section 3 discusses the experimental results flowed by conclusions in Sect. 4.

2 BGR circuit design

2.1 Current mode BGR with curvature compensation

Current mode BGR [5] was originally introduced to implement a voltage reference circuit when power supply is <1.2 V. Figure 1 shows a simplified curvature-compensated circuitry based upon the current mode scheme that is capable of further reducing the BGR output voltage variation against temperature [6]. By connecting a resistor

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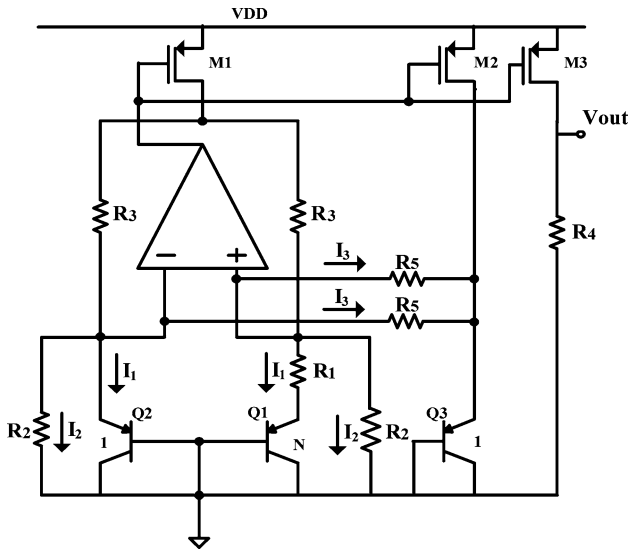

Fig. 1 Simplified schematic of current mode BGR with curvature compensation, where parasitic pnp transistors in CMOS are used

between the emitter and base of BJT transistor Q2, an extra current of $I_2 = \frac{V_{EB_{Q2}}}{R_2}$ is obtained, which is added to the PTAT current, $I_1 = \frac{V_{EB_{Q2}} - V_{EB_{Q1}}}{R_1}$, to generate a current with low sensitivity to the temperature variation.

From Fig. 1, given $\left(\frac{W}{L}\right)_{M1} = 2\left(\frac{W}{L}\right)_{M3}$, the V_{out} can be derived as:

$$\begin{aligned} V_{out} &= (I_1 + I_2 + I_3)R_4 \\ &= \left(\frac{V_{EB_{Q2}} - V_{EB_{Q1}}}{R_1} + \frac{V_{EB_{Q2}}}{R_2} + \frac{V_{EB_{Q2}} - V_{EB_{Q3}}}{R_5}\right)R_4 \\ &= \left(\frac{V_T \ln N}{R_1} + \frac{V_{EB_{Q2}}}{R_2} + \frac{V_{EB_{Q2}} - V_{EB_{Q3}}}{R_5}\right)R_4 \end{aligned} \quad (1)$$

where $V_T = KT/q$ and N is emitter area ratio of the BJT transistor Q1 and $Q2$. In (1), $I_1 = \frac{V_{EB_{Q2}} - V_{EB_{Q1}}}{R_1} = \frac{V_T \ln(N)}{R_1}$ is the PTAT current, which can compensate the first-order temperature dependence in I_2. Therefore, sum of I_1 and I_2 is almost constant over the temperature. Furthermore, the nonlinear relationship between V_{EB} and temperature can be expressed as [7]:

$$\begin{aligned} V_{EB}(T) &= V_G(T) - [V_G(T_r) - V_{EB}(T_r)]\frac{T}{T_r} \\ &\quad - (\eta - m)V_T \ln\left(\frac{T}{T_r}\right) \end{aligned} \quad (2)$$

where $V_G(T)$ is the bandgap voltage of Si as a function of temperature, T_r is the reference temperature, η is a temperature constant dependent on technology and m is the order of the temperature dependence of the collector current. Since the emitter currents of Q2 and Q3 are PTAT and temperature-independent, respectively, the third current term in (1) can be expressed as:

$$I_3 = \frac{V_{EB_{Q2}} - V_{EB_{Q3}}}{R_5} = \frac{V_T \ln\left(\frac{T}{T_r}\right)}{R_5} \quad (3)$$

where the term of $\frac{V_T \ln(T/T_r)}{R_5}$ can provide corrective current to compensate the higher-order temperature dependency in I_2. The value of R_5 is properly chosen for optimum curvature compensation as:

$$R_5 = \frac{R_2}{(\eta - 1)} \quad (4)$$

Theoretically, by properly adjusting the ratios of R_1/R_2 and R_5/R_2, one can obtain a simplified expression of the V_{out} as:

$$V_{out} = V_G(T)\frac{R_4}{R_2} \quad (5)$$

It is readily observed from (5) that the variation of V_{out} against the temperature originates from the bandgap voltage $V_G(T)$ only. Hence, further reduction the output voltage variation against temperature requires an accurate measurement and expression of $V_G(T)$.

2.2 Resistor trimming network and trimming methodology

Due to inevitable process variation and inaccuracy in device model of the parasitic pnp transistors, a fine resistor trimming network is necessary to achieve optimal temperature performance. Implementation of an accurate trimming network for R_1, R_2 and R_5 in this design is shown in Fig. 2.

In Fig. 2, the value for R is selected by circuit simulation. It is clearly observed that the resistor value can be increased by 16% with step of 1‰ of R by cutting off the fuses. Such trimming resolution is high enough to achieve the optimal temperature performance. It is noted that MOS switch might replace fuse for trimming purpose in general, which, however, has significant turn-on resistance that adversely affects the tuning accuracy desired for high-performance BGR.

The proper resistor network trimming method is given below using the output voltage versus temperature curves

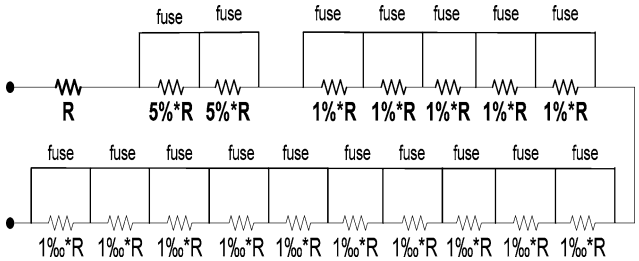

Fig. 2 An accurate resistor trimming network for R_1, R_2 and R_5

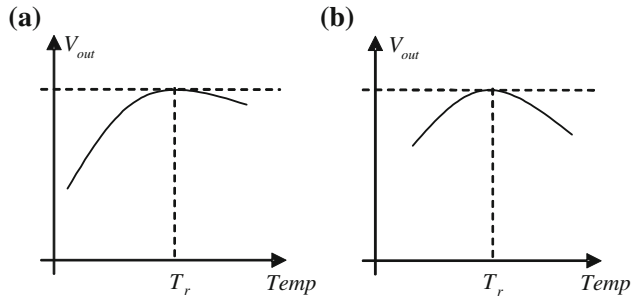

Fig. 3 **a** $V_{out}(T)$ curve after R_1 and R_2 trimming; **b** $V_{out}(T)$ curve after R_5 trimming

obtained from a two-step trimming procedure illustrated in Fig. 3.

In the first step trimming, the ratio of R_1 and R_2 is fine-tuned to compensate the first-order temperature dependency in $V_{EB_{Q2}}$ and to make the highest output voltage point occur around the reference temperature T_r, as shown in Fig. 3(a). In the second step trimming, accurate trimming of R_5 is conducted for higher-order compensation with the goal of achieving a symmetrical bell shape $V_{out}(T)$ curve around the T_r, which is desired to achieve the lowest temperature coefficient, as illustrated in Fig. 3(b).

2.3 Power supply rejection ratio (PSRR)

For the BGR circuit shown in Fig. 1, the power supply rejection ratio (PSRR) can be derived as:

$$\text{PSRR} = \left|\frac{v_{out}}{v_{dd}}\right| \approx \left|c\frac{1 - A_{dd}}{A}\right| \tag{6}$$

where c is a constant dependent on the values of R_1–R_4 and transconductance of Q1 and Q2 that is given as:

$$c = R_4\frac{2R_3 + (1/g_{mQ2})//R_2 + (R_1 + 1/g_{mQ1})//R_2}{R_3[(R_1 + 1/g_{mQ1})//R_2 - (1/g_{mQ2})//R_2]} \tag{7}$$

A_{dd} and A in (6) are power gain and open-loop gain of the operational amplifier, respectively, and A_{dd} is expressed as:

$$A_{dd} = \frac{v_{\text{output of Op-Amp}}}{v_{dd}} \tag{8}$$

Equation 6 clearly suggests that a large open-loop gain of the Op Amp will improve PSRR performance of BGR circuit. However, large A may also cause stability problem. Alternatively, one may choose to make the power gain A_{dd} as close to unity as possible without increasing the open-loop gain to achieve lower PSRR, which is a unique design technique introduced in this work where a large capacitance is placed between the output node of Op-Amp and the power supply to ensure a unity A_{dd}, especially at high frequency, hence achieve the lowest PSRR ratio. This novel design concept can be understood using the Op-Amp schematic shown in Fig. 4.

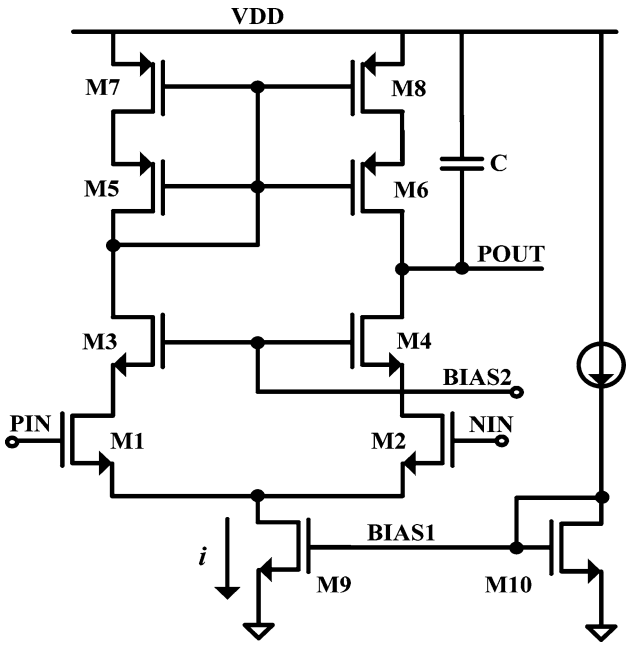

Fig. 4 New unity-A_{dd} Op-Amp schematic used in the BGR circuit

Assume that the bias current does not vary with v_{dd}, the power gain A_{dd} would be close to unity around DC. However, the A_{dd} starts to roll off as frequency increases when the equivalent impedance of C_{gdM6} of M6 is comparable to the DC resistance seen between VDD and POUT. Adding the capacitor C solves this problem. The power gain of the Op-Amp at high frequency region can be derived as:

$$A_{dd}(\omega) = \frac{g_{mM4}R_{oM4}R_{oM2}}{g_{mM4}R_{oM4}R_{oM2} + \frac{1}{j\omega(C+C_{gdM6})}} \tag{9}$$

where g_{mM4} is transconductance of transistor M4; and R_{oM4} and R_{oM2} are output resistance of M4 and M2, respectively. From (9), it is readily observed that a large C value is desired to ensure magnitude of A_{dd} close to unity. The capacitor C is also used to achieve the required frequency compensation for the Op-Amp circuit block. The Op-Amp performance can be further improved by eliminating the negative impact depicted in (10), which is associated with the non-ideal current source in practical circuit:

$$A_{dd} = 1 - \frac{i/2}{v_{dd}g_{mM7}} \tag{10}$$

where i is ripple in the tail current source due to v_{dd}. Equation 10 clearly indicates that the fluctuation in the

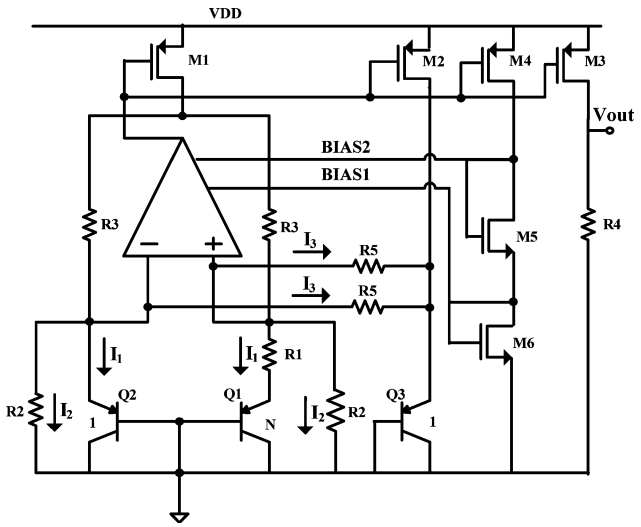

Fig. 5 BGR self-biased Op-Amp circuit in this design

Table 1 Op-Amp performance summary

Parameter	Value
DC gain	103 dB
Gain-bandwidth product	1.07 MHz
Phase margin	102°
Current consumption	2.4 μA

non-ideal tail current would drive the A_{dd} away from its preferred unity value. In order to suppress the undesired *i* variation effect, the curvature-compensated current generated by BGR circuit itself is used to bias the Op-Amp block in this design, as shown in Fig. 5. Careful design of the telescopic Op-Amp results in the optimal performance as summarized in Table 1. Simulation study shows that using self-biasing scheme, the PSRR can be reduced by 20 dB, compared to the BGR circuit with the Op-Amp biased traditionally.

2.4 Start-up circuit

The Star-up circuit used in this design is shown in Fig. 6. The start-up circuit operates as following: if the current in Q2 and R_2 is zero, the *p*-channel current sources (M1 and M7) are off. The gate of M8 is then pulled down to ground, hence injecting a significant current into Q2 and R_2. Once the circuit starts up, current in M7 and R_6 will cause the gate potential of M8 to increase and approach VDD, which, in turn, turns off the startup circuit. The same start-up scheme is also used for the Op-Amp biasing circuit.

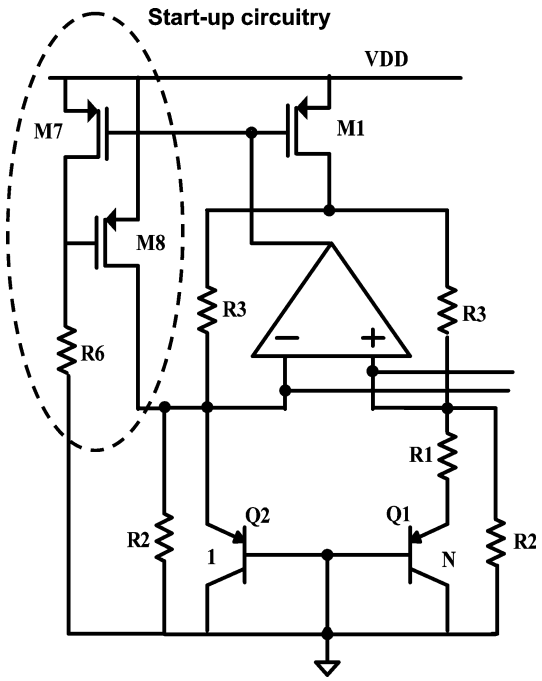

Fig. 6 Start-up circuit for the BGR in this work

3 Start-up circuitry

3.1 Experimental verification

This curvature-compensated BGR circuit is designed and fabricated in a commercial 0.35 μm CMOS technology. Extreme care was excised to ensure minimized resistor mismatching and Op-Amp offset voltage. Figure 7 shows the die photo of the BGR circuit with bonding pads and wires. The die size of the BGR circuit is 980 μm × 830 μm including bonding pads.

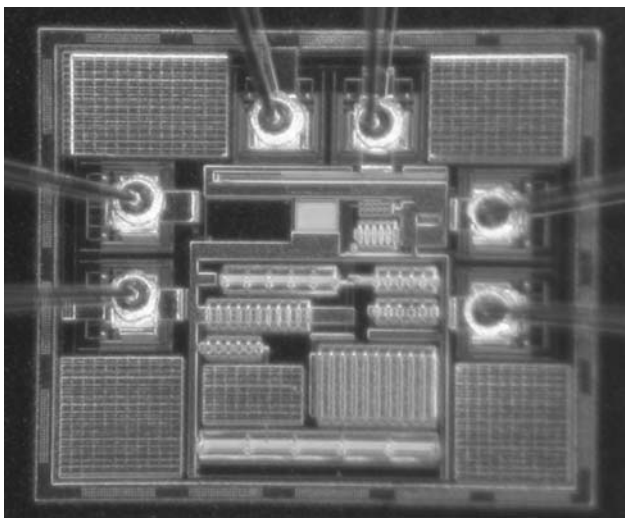

Fig. 7 Die photo of the BGR circuit in this work

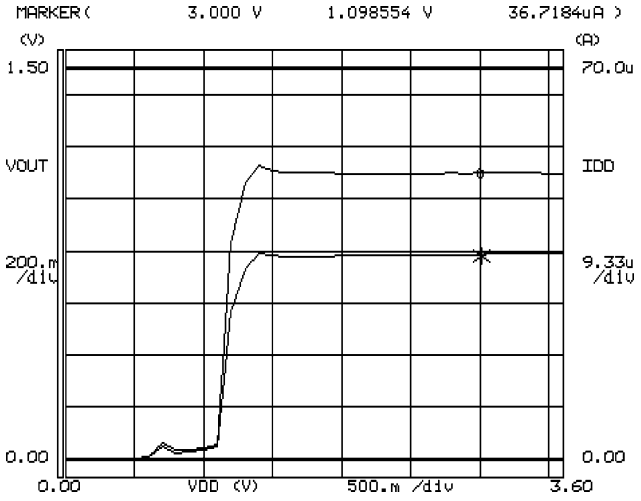

Fig. 8 Measured V_{out} and total current consumption for the BGR circuit

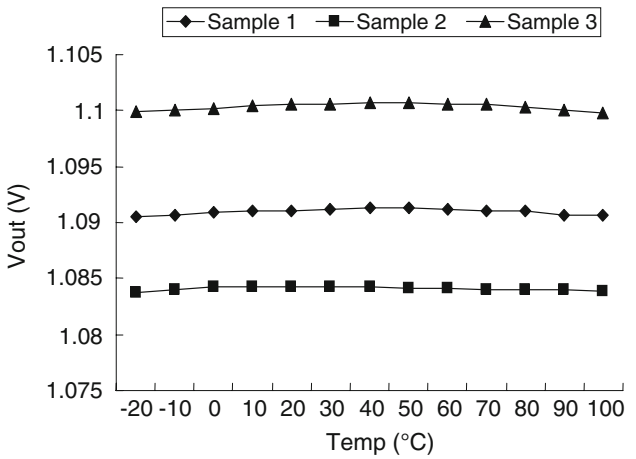

Fig. 9 Measured temperature variation for three BGR circuit samples

Testing results of packaged samples in ceramic DIP with removable lid are presented below. Die testing was somewhat affected by parasitic probing resistance. Full measurement was conducted for this BGR circuit over a wide temperature range from −20 to +100°C. Figure 8 gives the measured output voltage V_{out} and total current consumption, showing an output voltage of around 1.09 V and a very low current of only 37 μA at a supply of $V_{DD} = 3$ V, respectively. The lowest working supply voltage for this BGR circuit is 1.5 V. Figure 9 shows measured V_{out} variation over wide temperature range of [−20°C/+100°C]. The maximum measured variation of V_{out} is merely 0.4 mV over the full [−20 +100°C] temperature range after trimming, which translates into a very low TC of ∼3.1 ppm/°C in the worst case.

Figure 10 shows measured PSRR results of the BGR circuit that achieves a low PSRR of less than −80 dB at 1 kHz. Figure 11 shows the measured noise performance for the BGR circuit, which achieves a low output noise of about 1.43 μV $\sqrt{\text{Hz}}$ at 1 kHz that is mainly attributed to the Flicker noise generated by the MOS transistors in the circuit (e.g., M1 and M3 in Fig. 1; M1, M2, M7 and M8 in Fig. 6). The measured performance of the new BGR circuit is summarized in Table 2 for comparison with the state-of-art designs, which indicates that this design achieves the lowest worst case TC compared with reported works in similar CMOS technologies across similarly wide temperature ranges.

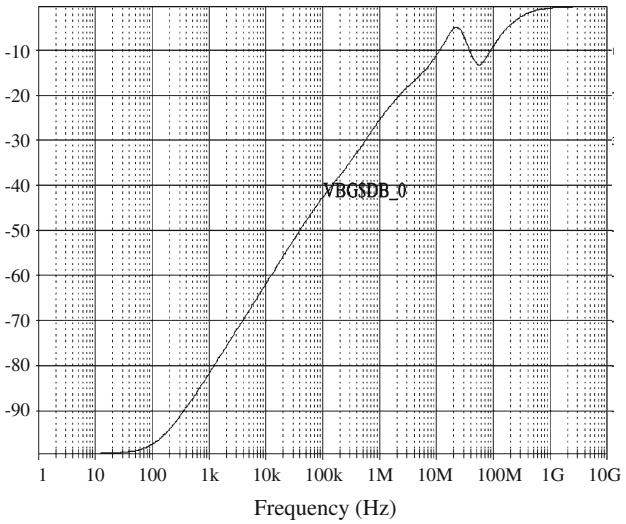

Fig. 10 Measured PSRR results for the BGR circuit

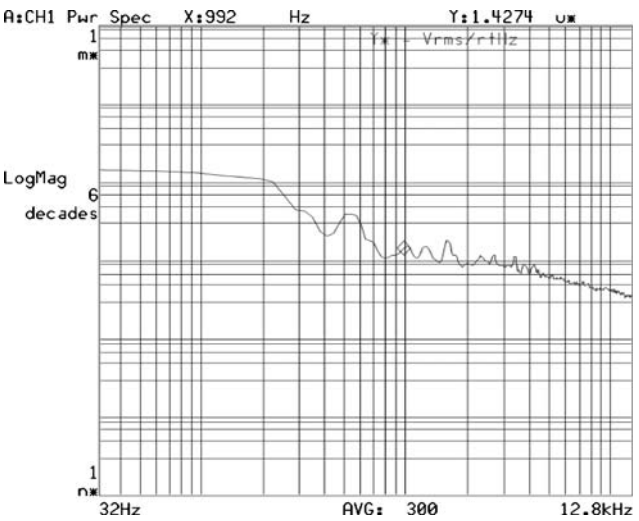

Fig. 11 Measured noise output of the BGR circuit

Table 2 Comparison of curvature-compensated Bandgap reference circuits

	This work	Reference [8]	Reference [9]	Reference [10]
Technology (μm CMOS)	0.35	2	0.6	0.35
V_{out} (V)	1.09	0.595	1.142	1.112
VDD_{min} (V)	1.5	1.1	2	1.5
DC Current (μA)	36.7	15	22	55
Temperature Range (°C)	−20/+100	−15/+90	0/+100	+25/+100
TC (ppm/°C)	3.1	20	5.3	10
PSRR	−80 dB at 1 kHz	N/A	−20 dB at 1 kHz	N/A

4 Conclusion

This paper reports design and implementation of a current mode curvature-compensated BGR in a 0.35 μm CMOS technology. The circuit features BGR self-biased Op-Amp, unity power gain technique to achieve low PSRR and resistor trimming for low temperature coefficient. Measurement results show that the BGR circuit delivers an output voltage of 1.09 V, achieves the lowest reported worst case TC of 3.1 ppm/°C over a wide temperature range of [−20°C/+100°C] and power consumption of 37 μA at 3.3 V, a low PSSR of less than −80 dB at 1 kHz, and a low output noise of 1.43 μV $\sqrt{\text{Hz}}$ at 1 kHz. The BGR circuit has a die size of 980 μm × 830 μm and works for a power supply down to 1.5 V.

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