



Si–Ge–Sn alloys grown by chemical vapour deposition: a versatile material for photonics, electronics, and thermoelectrics

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Abstract

Si–Ge–Sn alloys are offering unusual material properties with a strong potential to add a variety of functionalities to advanced CMOS technology. Being a group IV alloy, SiGeSn can be monolithically integrated on Si. The discovery of a direct band gap at Sn concentration above 8%, the extremely small effective mass for electrons and holes as well as the pronounced phonon scattering are opening new opportunities for Si photonics, high frequency devices and thermoelectrics. Si–Ge–Sn alloys with Sn concentration far beyond the solid solubility limit are metastable, artificial materials, which request challenging growth conditions. In this paper the epitaxial conditions for Si–Ge–Sn alloys to achieve precise control of the Sn content, to manage the lattice mismatch and defects, as well as to fabricate doped layers are discussed. The applied process control allows for epitaxy of group-IV heterostructures, required for typical devices for photonic and electronic applications. In this context, lasers and nanowires MOSFETs are discussed in this paper. In additions, the thermal conductivity is investigated as a critical material parameter to obtain a high thermoelectric figure of merit in GeSn alloys.

Keywords GeSn alloys · Silicon photonics · Gate all around FET · Thermoelectric · Photonic integrated circuitry · GeSn laser

1 Introduction

The advancement in crystal growth technology, allowing to grow group IV alloys like GeSn [1] and SiGeSn [2] far away from thermodynamic equilibrium enabled the fabrication of these materials with Sn concentration distinctively higher than the solid solubility limit. At Sn concentrations beyond 8% in GeSn alloys a direct bandgap was discovered and the first optical pumped laser was demonstrated [3]. The GeSn layers are grown monolithically on Si substrate via a relaxed Ge buffer layer. Thus, this technology allows fabricating electro-optical devices such as laser, photodiodes and modulators using solely group IV elements [4]. GeSn alloys are low bandgap semiconductors particular suitable for the SWIR-MIR region ranging from 1.5 to 4.2 μm wavelength (λ). Extensive studies of the optical properties and using the observation for bandgap simulations, revealed extremely low effective masses for electron

and holes [5] leading to high carrier mobility's, which surpass the values of Ge crystals at comparable doping levels. Alloy scattering, typical limiting the mobility of III/V semiconductors is not the limiting scattering mechanism in GeSn due to the peculiar band structure. This properties of GeSn alloys, namely high mobility and low contact resistance, is suitable for the development of high performance, low power nano-sized field effect transistors (FETs) [6]. The monolithic combination of these devices permits the design of electronic photonic integrated circuitry (EPIC) in Si. Moreover, the high carrier mobility, i.e. high conductivity, of GeSn and SiGeSn alloys in combination with the low thermal conductivity offers a new route for thermoelectric power generation at temperatures below 700 K. With the accelerated growth of computing and communication technologies, a new paradigm of life has emerged, the internet of things (IoT). Immediately it becomes clear, that GeSn and SiGeSn offers a platform for self-powered chips carrying electronic and photonic devices for sensing and data communication enabling applications for IoT. In these chips, functional compatibility between the different building blocks is required to ensure the optimal performance. To this end group IV alloys have the potential to expand the current silicon-based semiconductor technology substantially. Targeting,

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for example, for wearable smart devices taking advantage of the excellent electrical characteristics, efficient optoelectronic devices and capability to convert heat of the surrounding, for example body heat, into electrical energy to power the entire device. Furthermore, due to the direct bandgap of the $\text{Ge}_{1-x}\text{Sn}_x$ alloys, band-to-band tunnelling increases considerably, which is ideal for tunnelling-FETs [7]. Additionally, high Sn contents enhance the spin-orbit coupling that could potentially offer exciting properties such as superconductivity [8], large negative magnetoresistance [9], or a very rich spin physics [10, 11].

This paper discusses the challenges of epitaxial growth of GeSn alloys by chemical vapour deposition, putting particular emphasis on the optimization of growth parameters which enables growth of complex hetero- and quantum well structures with large variations in the composition among the individual layers in these structures. The distinct progress that has been achieved is applied in demonstrators for various GeSn devices. Currently, the biggest challenge for optoelectronic devices is the search for an electrically pumped GeSn laser operating at room temperature. Here we demonstrate optical pumping at 300 K as well as electrically pumped laser operating at 120 K. In terms of nanoscaled electrical devices challenges for improving device performance are low ohmic contact resistance as well as short channel effects like drain and gate induced band lowering. To this end, the impact of GeSn/Ge heterostructures on nanowire FET's are discussed. The nanowire FET's might be suitable candidates for low power cryoelectronics, an indispensable ingredient for quantum computation [12]. Finally, low values of thermal conductivity in $\text{Ge}_{1-x}\text{Sn}_x$ films are reported through Raman thermometry, demonstrating the possibility of using this material system for thermoelectric power generation in integrated Si-based applications [13].

The considerable achievements presented in this paper are governed by the capability to grow and control hetero- and quantum well structures in this group IV material system of high structural and electronic quality. Here we will introduce the main steps in the experimental methodology. In particular, the preparation of reactive molecules in the gas phase of a chemical vapour deposition (CVD) reactor to gear up chemical reactions at the substrate surface will be discussed. It is important to notice, that the understanding of this process, lead to a simplified process to grow heterostructures with abrupt interfaces. An isothermal growth process of heterostructures with layers of different Sn concentrations by controlling the carrier gas flow is introduced.

2 Si-Ge-Sn epitaxial challenges

The growth of unstrained GeSn with a Sn concentration exceeding 8% is required to obtain a direct bandgap and low effective masses of electrons and holes. The amount

of Sn can be reduced by adding additional tensile strain to the GeSn layer [14]. However, pseudomorphic GeSn layers grown on Ge harbour compressive strain. Moreover, using Si as a substrate and depositing a relaxed Ge buffer layer requires relaxing the compressive strain in the Ge layer due to the lattice mismatch of Ge and Si of approximately 4%. Thus applying tensile strain to GeSn demands for additional stressor layers. In addition to the large lattice mismatch between Si and GeSn, the low solubility of Sn on Ge adds challenges to the epitaxial growth. Thus, epitaxial growth of GeSn with high Sn concentration is only possible at a set of parameters permitting epitaxy of high quality films far from thermal equilibrium, such as low temperatures and simultaneously high growth rates. Typical CVD growth processes will lead to low quality films at those conditions and the films will harbour many point defects, rough surfaces or even amorphous layers. Conventional CVD processes use precursors of similar chemical stability to control the chemical composition of an alloy or compound semiconductor smoothly. III/V compounds like GaAs are grown by MOCVD typically in the diffusion regime at temperatures ~ 900 K to obtain superior crystal quality. Si and SiGe layers grown by CVD are deposited at even higher temperatures, beyond 900 K, still in the kinetic regime, since the diffusion regime kicks in at even higher temperatures. Generally, it can be stated that materials with high melting points have to be grown at higher temperatures to obtain crystalline perfection. Thus lower temperatures (700–800 K) can be used for the deposition of Ge using Ge_2H_6 [1] as precursor, however, also decreasing growth rates are required to avoid decreasing structural quality of the film at low temperatures. Obviously, a different approach has to be considered if GeSn should be grown at low temperatures and high rates to overcome the limits of the solid solubility of Sn in Ge and still getting high structural perfection of the films. By selecting precursors of very different chemical stability, but large reactivity among them, such an approach is achieved. First reports on GeSn by CVD with reasonable crystal quality and Sn contents above the solubility limit by using Ge_2H_6 and SnCl_4 hinted towards possible pathways [15]. In fact early reports on accelerated CVD growth using combinations of Hydride and Chloride precursors can be found in literature for the growth of GaAs [16] or As doped Si films [17]. However, a better understanding of this process was required in order to make it accessible for GeSn growth at deposition temperatures around 570 K maintaining growth rates > 0.2 nm/s.

The successful recipe for the growth of GeSn alloys with Sn concentration far beyond solubility limit requires a set of parameters which allows for sufficient formation of GeH_x radicals ($x = 1, 2, 3$) in the gas phase, leading to a high concentration of these radicals on the substrate surface. The SnCl_4 , being a much more stable molecule,

will arrive at the surface and react with the GeH_x radicals forming HCl and the GeSn crystal. The chemical reaction between the radicals and the SnCl_4 molecules is very exothermic; this energy is used to overcome kinetic barriers of the growth of GeSn [18]. Indeed activation energies (E_A) determining the growth rate (r) of GeSn, $r \sim E_A/kT$, as small as 0.3 eV have been determined. Compared to $E_A = 1.3$ eV for the growth of pure Ge using GeH_4 [19]. Conclusively, at temperatures below 630 K the growth rate of Ge decreases much faster with temperature than that of GeSn, leading to an increase of the Sn concentration while decreasing T. Thus the exothermic reaction on the surface warrants high growth rates and crystalline integrity of the GeSn film despite low growth temperatures (T) and high Sn concentrations, exceeding 14% [20].

Two common commercially available Ge precursors, namely germane (GeH_4) and digermane (Ge_2H_6), are the most commonly used in (Si)GeSn chemical vapour deposition. The increased reactivity of Ge_2H_6 at low growth temperatures and the resulting high growth rates makes it ideal for the epitaxy of thick relaxed layers [3, 20]. However, Ge_2H_6 is significantly more expensive than GeH_4 , has limited availability, and the epitaxy may be accompanied by the formation of defects [22–24]. The growth rates obtained by using GeH_4 as precursor are smaller, however, films with high structural perfection can be obtained as well [19]. However, for thin $\text{Ge}_{1-x}\text{Sn}_x$ layers the low growth rate accessible with the GeH_4 precursor is less crucial. The GeH_4 precursor narrows the process window of growth parameters such as reactor pressure, gas velocity and temperature [25, 26]. It is quite obvious, that these parameters (pressure, temperature, gas velocity) have strong impact on the gas phase reactions of molecules of different stability like GeH_4 and Ge_2H_6 . The preferred reaction partner for the stable SnCl_4 molecule on the substrate surface are GeH_x ($x = 1, 2, 3$) radicals. An additional parameter suitable to influence gas phase reactions is the composition of the carrier gas, i.e. mixtures of H_2 and N_2 . A high N_2 concentration is expected to increase the cracking rate of GeH_4 and Ge_2H_6 , whereas a high H_2 concentration will decrease the cracking rate and will increase the reaction rate for the back-reaction from GeH_x -radicals to GeH_4 molecules. However, it has to be kept in mind that the H_2 ambient supports the hydrogen passivation of the surface preventing Ge segregation [27] as well as surface oxidation [28]. Most importantly, the molecules prepared by gas phase reactions absorbing at the substrate surface are crucial for the subsequent surface kinetics guiding the CVD growth at low temperatures [29]. The cognizance that the amount of (physisorbed) GeH_x radicals on the surface is determined by gas phase reactions and governs the growth rate and the Sn concentration of the growing film leads to novel methods for simple switching processes of

to change the composition of the films in heterostructures, which will be discussed in the next chapter.

3 Growth of isothermal hetero- and quantum well structures

As stated before, a high Sn concentration is achieved at low T, typically around 540–570 K, with a strong dependence of the Sn concentration on T. High Sn concentrations are desired for layers exhibiting a strong “directness” ΔE of the bandstructure, here, ΔE reflects the energy difference of the Γ and L valley in the conduction band. A high ΔE is essential for a laser supposed to emit at room temperature and at low threshold currents [14] or in electronic devices taking advantage of the high carrier mobility in Sn rich layers. Typically these devices need cladding layers to provide optical or electronic confinement, thus layers with a larger bandgap, thus with lower Sn concentration and may be additional Si incorporation need to be deposited underneath and on the top of the high Sn concentration alloy. In conventional GeSn CVD growth, processes to fabricate such structures can be tried by changing the deposition temperature while interrupting the growth or changing the SnCl_4 partial pressure. However, in particular for the growth of low Sn containing layers on top of layers with high Sn concentration, an increase of T leads to Sn precipitation. Keeping the temperature constant and changing the SnCl_4 partial pressure results in a very limited range of Sn concentrations. As argued above, it seems to be appealing to use the other two parameter, the reactor pressure and the total gas flow of N_2 in the reactor. Here, we keep all other flows and the temperature constant, thus the GeH_4 to SnCl_4 ratio is constant as well. The growth is performed on strain relaxed Ge buffer layers. Both parameter, decreasing the total pressure or increasing the flow rate have similar effects. The partial pressures are proportionally decreased with the factor of pressure reduction or N_2 flow increase. The gas velocity increases, i.e. the retention time of the reactive precursors in the reactor decreases for both cases. Consequently, the amount of GeH_x radicals on the surface will decrease as well. Indeed keeping a temperature of 570 K and reducing the total pressure (p_{tot}) from 200 to 60 mbar leads to a Sn concentration of 10.5 and 8.5% and growth rates of 1.25 and 2.37 nm/min, respectively. An even stronger impact is found while changing the total flow of N_2 from 2000 l/min to 13,000 l/min at 570 K and $P_{\text{tot}} = 60$ mbar. At 2000 l/min a Sn concentration of 12% and at 13,000 l/min a Sn concentration of 6.7% was established, with $r = 2.55$ and 1.47 nm/min, respectively. For the growth of GeSn alloys at small N_2 fluxes 15% of Sn was determined from x-ray diffraction if the growth was performed on GeSn (12%) instead of growing on the strain relaxed Ge buffer. Further investigations are

necessary to clarify this effect. However, using this very simple process in switching the total gas flow of N_2 (Q_T), and keeping all other parameters (T , p_{tot} , GeH_4 and SnCl_4 fluxes) constant the desired structures, as demonstrated in Fig. 1, can be manufactured. Additional changes in the SnCl_4 - GeH_4 ratio increases the accessible range for Sn concentrations. Thus, we found an isothermal growth method to realize hetero- and quantum well structures of high perfection.

The proposed method was used in the fabrication of a quantum well structure. The design of the heterostructure is shown in Fig. 1b. Keeping a constant deposition temperature of 570 K, a 100 nm pseudomorphic $\text{Ge}_{0.93}\text{Sn}_{0.07}$ barrier was deposited under a Q_T of 13,000 l/min on the Ge pseudosubstrate. Subsequently, the N_2 flow was decreased, and a 25 nm well layer with a high Sn content of 11 at. % was deposited. Finally, the upper barrier of 15 nm was obtained with the same flux as the first layer. The layer thickness and stoichiometry of every layer were obtained by fitting the Rutherford backscattering spectra (RBS) random spectra shown in the inset in Fig. 1a. The crystal quality of the obtained heterostructure is reflected by the low minimum channelling yield (χ_{min}) of 3%. These results were confirmed by the symmetric X-ray diffraction (XRD) spectra with the presence of Laue oscillation around the

peaks corresponding to $\text{Ge}_{1-x}\text{Sn}_x$ while the reciprocal space mapping (RSM) shows that the layers are growing pseudomorphic (Fig. 1c). Secondary ion mass spectrometry (SIMS) show the same stoichiometry and also the uniformity of the elements along the heterostructure (Fig. 1d). The high-resolution transmission electron microscopy (HR-TEM) images of Fig. 1e show high crystallinity of the epitaxial stack with very sharp and well-defined interfaces. Finally, the temperature-dependent photoluminescence (PL) measurement is presented in Fig. 1f with a maximum intensity at 5 K. As the temperature increases, the PL peak position shifts towards lower energy as expected due to T dependence of the bandgap.

The above heterostructure proves the suitability of the proposed method for the design of high-quality isothermal heterostructures for device applications in electronics, quantum transport, or spintronic, where a high control in the thickness and the Sn concentration of the layers is required.

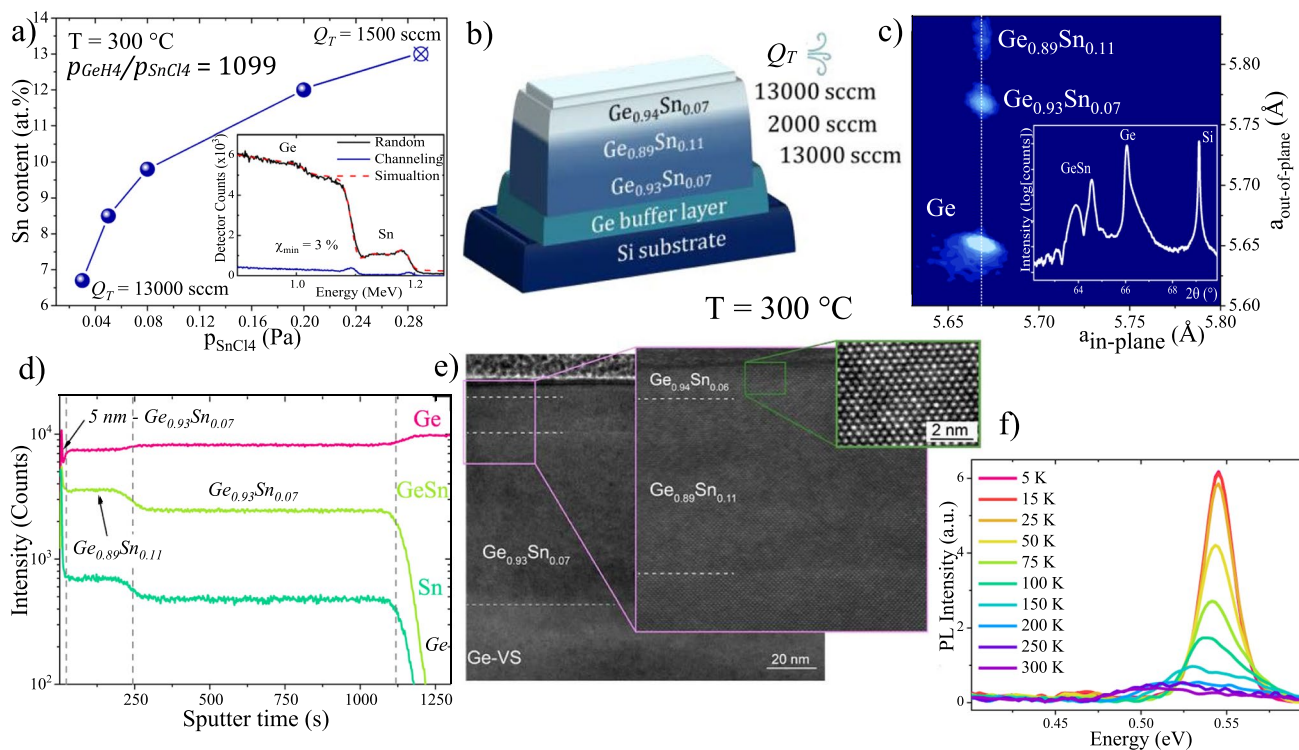


Fig. 1 **a** Different Sn content incorporation at 300 °C as a function of the partial pressure of SnCl_4 determined by the total carrier flow (Q_T) keeping $p_{\text{GeH}_4}/p_{\text{SnCl}_4}$ constant. Characterization of an isothermal quantum well heterostructure: Inset: RBS random and channeling spectra with a minimum channelling yield of 3%. **b** Sketch with

the matching total flow. **c** Asymmetric RSM showing pseudomorphic growth. Inset: symmetric 2θ - ω XRD spectra along the (004) plane. **d** SIMS profile, **e** cross-sectional high-resolution TEM micrographs, and **f** temperature-dependent PL spectra

4 Si-Ge-Sn applications

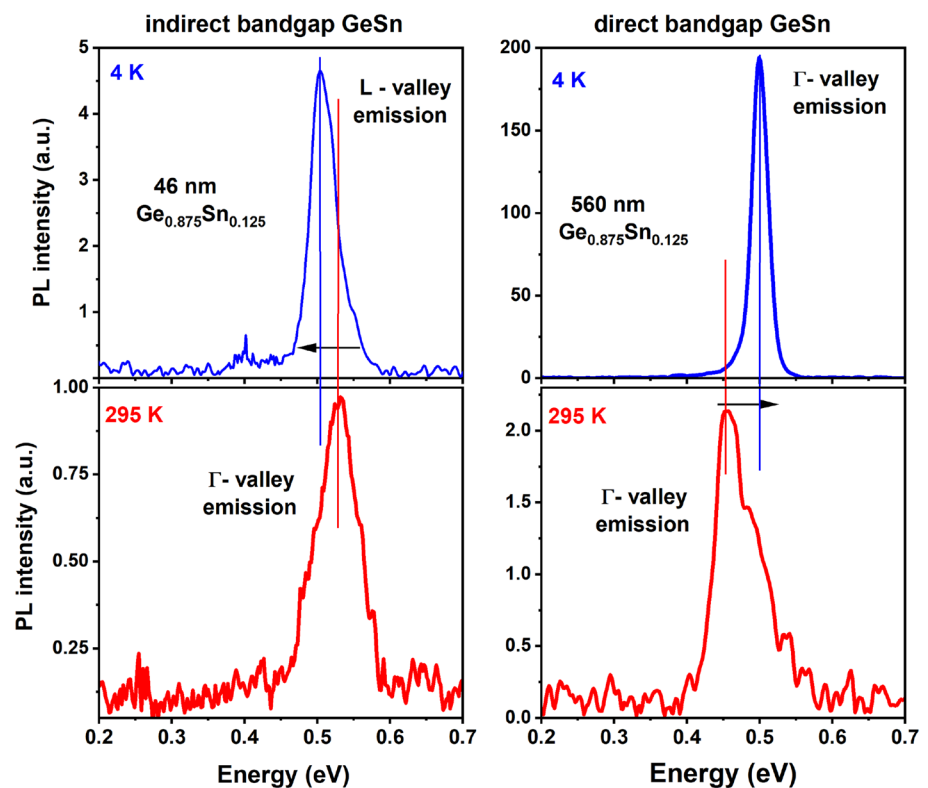
4.1 Photonics

Photonic applications take advantage from the unique property of the fundamental direct bandgap in the GeSn compared to the other Si group elements and alloys, which are indirect semiconductors. This property is obtained for Sn atomic composition above 8% in a cubic structure, as was mentioned before. However, their directness ΔE , the difference between the minimum energy, at the Γ -valley and the next close L-valley (indirect transition) is small, typically between $\Delta E = 0$ and 100 meV. This directness can be tuned by increasing the Sn content but also by strain engineering. The tensile strain increases the directness while compressive strain decreases it. As an example, Fig. 2 shows the difference between the same GeSn layer being indirect and direct depending on the strain in the layer. A 45 nm GeSn-12 at. % layer, pseudomorphically grown on Ge substrate as a compressive strain of about -1.65% that transforms the layer into an indirect semiconductor. At the same Sn content, a strain relaxed layer, here 560 nm, with a rest compressive strain of 0.3% it is a direct bandgap semiconductor. The difference between indirect and direct semiconductors can be easily observed by looking at the temperature-dependence PL. At room temperature, the PL emission in both cases is given by the

Γ -valley transitions. At low temperatures, the PL emission is given by the lowest conduction band energy which is the L-valley for the indirect 46 nm GeSn layer and the Γ -valley for the 560 nm GeSn layer [30]. So going from 300 to 5 K the PL will shift to lower energies for the indirect semiconductor and to higher energy for the direct bandgap semiconductor, for ex GaAs [31].

Evidently, direct bandgap semiconductors are the ideal candidates for the fabrication of detectors and light emitters, especially lasers. The lasing in GeSn alloys has been first observed in 2015 by Wirths et al. [3] and, in a time period of only 5 years, for a large range of Sn contents from 8 to 20 at.% Sn and different cavity configurations like microdisks [14, 32, 33], waveguides [34] Sn content between 8 and 14 at.% using a fabric Perot cavity configuration. Moreover, multiple QW lasers have been demonstrated which underline the enormous potential of GeSn/SiGeSn heterostructures as the optical active medium. The laser figures of merit like the threshold and the maximum lasing temperature have been constantly improved over the past few years reaching a threshold as low as 800 W/cm² in tensile strained layers and 395 K operation for larger Sn contents or in combination with strain (Fig. 3b). However, the understanding of physical mechanisms and material limitations behind the laser emission is still under debate. Different approaches are lately investigated: (i) increasing the Sn contents, e.g. above 17 at.% [35, 36] Sn; (ii) introduce tensile strain in the active layer [14]. These two approaches do not exclude one each other

Fig. 2 PL emission spectra shift with temperature for (left) a 45 nm indirect bandgap GeSn layer and (right) a 560 nm direct bandgap GeSn layer. The energy shift direction indicates if the layer is a direct or indirect semiconductor



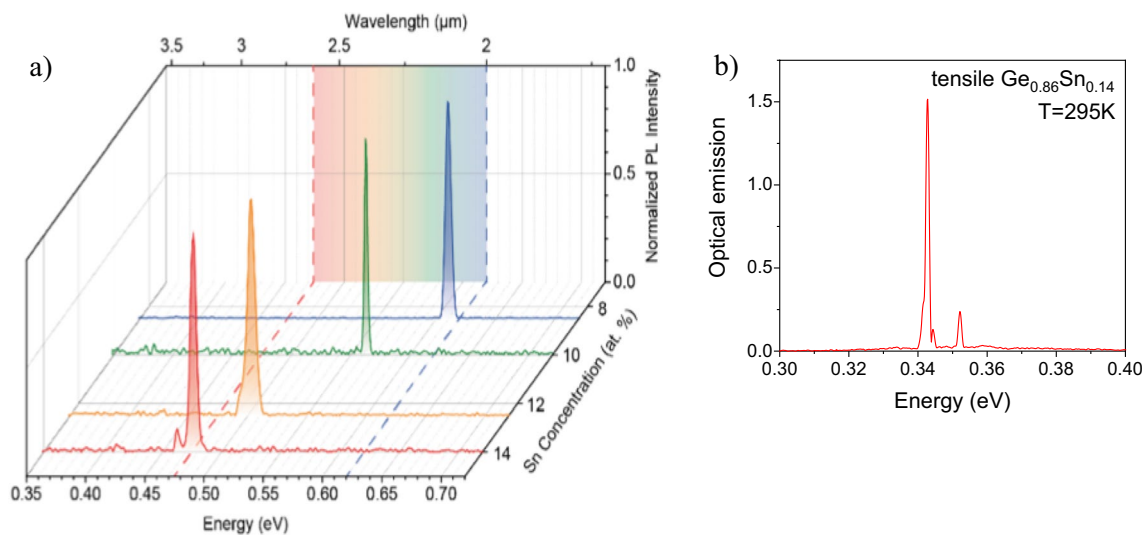


Fig. 3 **a** PL laser spectra at 10 K of GeSn layers with different Sn contents using a fabric Perot cavity configuration. **b** Optical emission at 295 K of a tensile GeSn with 14 at. % Sn

and may be unite by manipulating the material electronic band structures such that allow larger energy separation ΔE of the bands and even larger net gain via decreased emission re-absorption [37, 38].

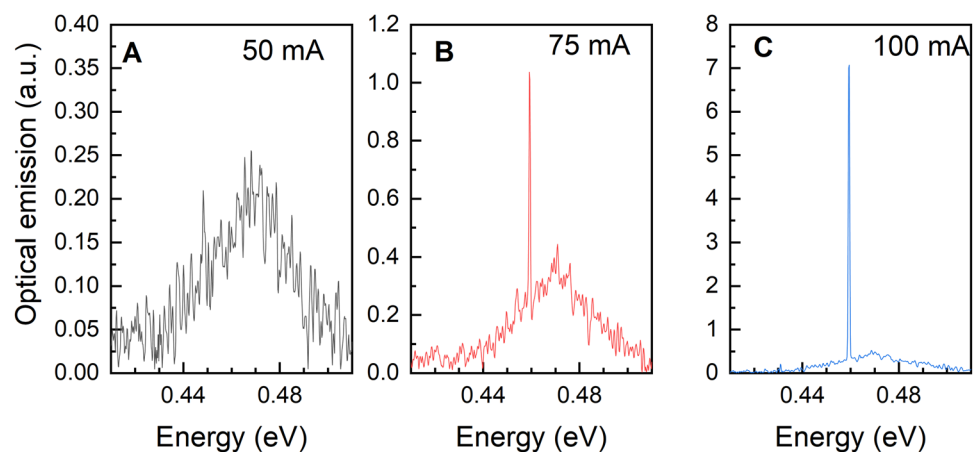
The main target of Si photonics is to realize an electrically injected GeSn layer monolithically integrated on Silicon. To this aim, the threshold for optically pumped lasers must be reduced. Our experiments showed that a 14 at. % Sn content alloy is a good choice that offers a reasonable large directness of ~ 100 meV with a high crystalline quality of the layer. Such GeSn layers offer a laser threshold of 20 kW/cm^2 at 10 K and a maximum laser temperature of 270 K using an under-etched microdisk configuration. If in addition $\sim 1\%$ tensile strain is induced in the GeSn lattice then the optical laser threshold further reduces to $< 10 \text{ kW/cm}^2$ and the maximum temperature for lasing reaches 300 K. These facts as well as the possibility to realize low contact resistance on

GeSn and SiGeSn alloys allow to successfully address electrical injection in GeSn-based laser structures. Using a double heterostructure Ge_{0.86}Sn_{0.14} layers and SiGeSn barriers as injection layers an electric microdisk laser structure has been fabricated. The emission spectrum change from the broad electroluminescence (EL) to the formation of whispering gallery modes and finally to laser emission is clearly shown in Fig. 4. The spectra were taken at 5 K for a microring laser diode with outer/inner diameters of $7/2 \mu\text{m}$, respectively.

4.2 Vertical gate all around (GAA) nanowire MOSFETs

The vertical design of MOSFETs allows us to improve the performance of both p-channel and n-channel FETs with different heterostructures. The devices will benefit from high quality single crystalline layer providing high mobility

Fig. 4 EL spectra of a Ge_{0.86}Sn_{0.14} microring diode indicating the transition from spontaneous emission to laser emission at different pumping currents



channels, defect-free interfaces, and *in-situ* doping for source/drain contacts. The gate-all-around (GAA) nanowire architecture further improves the short-channel effects.

For the fabrication of vertical GAA nanowire p-FETs, the $\text{Ge}_{0.92}\text{Sn}_{0.08}/\text{Ge}$ heterostructure depicted in Fig. 5a is grown. Here GeSn layer on top of the nanowire defines the source of the FET. The small bandgap of the GeSn improves the carrier injection and lowers the contact resistance. The device is fabricated with a top-down process, including nanowire formation by e-beam lithography and reactive ion etching and a subsequent $\text{Al}_2\text{O}_3/\text{TiN}$ gate stack deposition, NiGeSn formation for source and drain contacts and finally metalization. A detailed description of the fabrication process can be found in ref. [39]. Figure 5b shows the fabricated nanowires with a diameter from 65 nm down to 32 nm. A 9 nm thick Al_2O_3 and a 40 nm thick TiN layer form the gate stack which is wrapped around the nanowire (Fig. 5c) with a perfect interface to the Ge channel as indicated by the high-resolution TEM in Fig. 5d. A GeO_x interfacial layer is formed to passivate the Ge nanowire surface and reduce the density of interface states (D_{it}).

The comparison of the drain current I_D vs gate voltage V_{GS} (I_D - V_{GS}) transfer characteristics for the 32 nm (Fig. 5e) and 65 nm (Fig. 5f) devices indicates the scaling of the nanowire diameter can improve the device performance with a smaller subthreshold swing (SS), lower off-currents and a

larger on-current/off-current (I_{ON}/I_{OFF}) ratio. The drain current I_D shown in Fig. 5e is normalized with the perimeter of the nanowire. The on-current for smaller-diameter nanowires is lower because the contact resistance on a smaller-diameter nanowire is larger. Therefore, reducing the contact resistance on tiny nanowires is a challenge. The contact resistivity $\rho_c \propto \exp(\frac{\phi_b}{\sqrt{N}})$ depends on the Schottky barrier height ϕ_b and the doping concentration N . Thus using a low bandgap material on top of the nanowires providing also a reduced ϕ_b is expected to reduce the contact resistance. This is confirmed by the comparison of GeSn/Ge heterostructure and Ge homostructure p-FETs as shown in Fig. 5g. Using a $\text{Ge}_{0.92}\text{Sn}_{0.08}$ layer as the source on top of the nanowire can increase drain currents significantly. At $V_{DS} = -1.0$ V and a gate overdrive voltage $V_{ov} = V_{GS} - V_{TH} = -0.5$ V, where V_{TH} is the threshold voltage of the device, the on-current is improved by 32%.

Ge n-FETs face more challenges because of the low electron mobility. Thus we designed Ge/ $\text{Ge}_{0.95}\text{Sn}_{0.05}/\text{Ge}$ heterostructure for vertical nanowire GAA n-FETs as illustrated in Fig. 6a. Since $\text{Ge}_{0.95}\text{Sn}_{0.05}$ offers higher electron mobility compared to Ge, GeSn is thus used as the channel material. The larger bandgap of Ge at the source and drain area may reduce the gate-induced drain leakage (GIDL) which is caused by band-to-band tunnelling. The fabrication process

Fig. 5 **a** Schematic of a vertical GAA nanowire p-FET with $\text{Ge}_{0.92}\text{Sn}_{0.08}$ source and Ge channel. **b** Overlapped SEM images of GeSn/Ge NWs used for p-FETs. **c** Cross-sectional TEM image of a vertical $\text{Ge}_{0.92}\text{Sn}_{0.08}/\text{Ge}$ GAA NW p-FET. **d** HR-TEM image showing the sharp interface between the Ge channel and the $\text{GeO}_x/\text{Al}_2\text{O}_3$ interface. **e** I_D - V_{GS} transfer characteristics for a p-FET with NW diameters of 32 nm and **f** 65 nm. **g** Comparison of the I_D - V_{DS} output characteristics of a GeSn/Ge heterostructure nanowire p-FET with that of a reference Ge homojunction device. The nanowire diameter is 65 nm for both cases. The GeSn/Ge p-FET shows much larger currents than its Ge counterpart

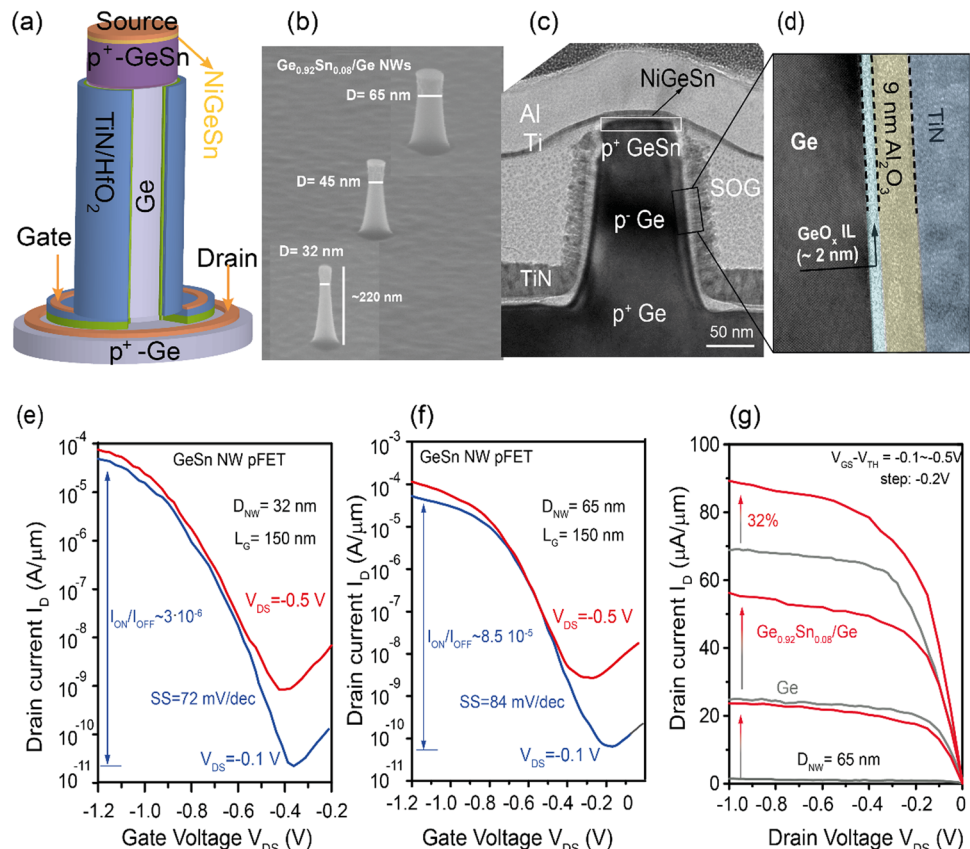
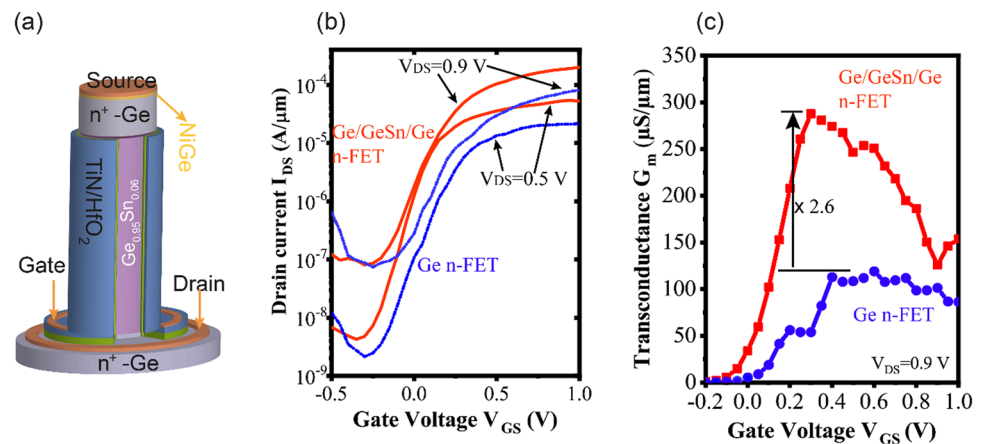


Fig. 6 **a** Schematic of a vertical GAA nanowire n-FET with $\text{Ge}_{0.95}\text{Sn}_{0.05}$ channel and Ge source/drain. **b** Comparison of the I_D - V_{GS} transfer characteristics for a Ge/ $\text{Ge}_{0.95}\text{Sn}_{0.05}$ /Ge n-FET with that of a Ge homojunction device, both with an NW diameter of 25 nm. **c** The GeSn channel n-FET shows 2.5 times higher transconductance G_m , compared to the Ge n-FET, demonstrating higher electron mobility of the GeSn layer



is the same as we developed for p-FETs. Figure 6b shows the I_D - V_{GS} transfer characteristics of a vertical Ge/ $\text{Ge}_{0.95}\text{Sn}_{0.05}$ /Ge nanowire GAA n-FET in comparison with a vertical all-Ge homojunction GAA nanowire device. Both devices have an NW diameter of 25 nm and a gate length of 100 nm. The homojunction Ge device shows a SS of 136 mV/dec and an I_{ON}/I_{OFF} ratio of $\sim 1 \times 10^4$ at $V_{DS}=0.5$ V. Using $\text{Ge}_{0.95}\text{Sn}_{0.05}$ channel improves the SS, which is reduced to 92 mV/dec and results in higher I_{ON}/I_{OFF} ratio ($\sim 1.3 \times 10^4$) and larger on-currents. The improvement of the transconductance (Fig. 6c) with $G_{max} \sim 290 \mu\text{S}/\mu\text{m}$ peak for GeSn which is 2.6 times larger than the 112 $\mu\text{S}/\mu\text{m}$ obtained for the Ge device demonstrates the mobility enhancement by using GeSn as a channel. Since the source/drain and the gate stack for both devices are the same, the transconductance increase is mainly caused by the higher electron mobility. We can estimate that the electron mobility in the $\text{Ge}_{0.95}\text{Sn}_{0.05}$ channel is 2.6 times higher than that in Ge. Employing GeSn layers with Sn concentrations above 5% as channel material will further increase the electron mobility. The performance of such devices is currently under investigation.

4.3 Thermoelectric

The large carrier mobility, leading to a high electrical conductivity, in combination with strong phonon scattering induced by the (Si)GeSn alloys immediately leads to the assumption that this material might be of interest for thermoelectric. The low thermal stability of the metastable GeSn alloy will limit thermoelectric applications to temperatures below the CVD deposition temperature (< 600 K). However, in particular in the low temperature regime low cost and efficient energy harvesting thermoelectric devices are missing. This field is becoming increasingly important, for example aiming grid independent, wearable/portable devices, putting pressure on material research for the development of new materials with improved thermoelectric properties as well as low cost, CMOS compatibility, and mechanical

flexibility. The most common thermoelectric materials, the IV-VI semiconductor alloys, like BiTe, PbTe, and PbSe are environmental harmful or contain rare earth elements. In view of applications, semiconductors based on group IV alloys are advantageous due to their easier monolithic integration with the CMOS technology and Si photonics. While Si and Ge have very large lattice thermal conductivity (160 and 60 W/K.m) and are consequently inefficient for thermoelectric application the SiGe random alloys offer a low lattice conductivity due to a strong phonon scattering. SiGe thermoelectric generators are already in use for over 50 years but for high-grade energy (above 1200 K). For low-grade heat harvesting, below 500 K, there are to date no bulk Si-compatible semiconductors. The Si-based thermoelectric research was mainly focused on SiGe/Si superlattices or reduced dimensionality by the use of Si nanowires. Sn-based alloys like GeSn and SiGeSn have the potential to become game changers in CMOS energy harvesting. The element, Sn, is a well-known component in TE materials like SnTe or SnSe that recently gained a lot of interest for medium-high grade energy conversion (> 700 K). Interestingly, Sn was not studied in alloys with its own group IV, like GeSn and SiGeSn that even makes the monolithic integration of electronics and photonics a real possibility.

To evaluate the possibility to use GeSn alloys for thermoelectric devices with the aim to power grid independent devices for application like the internet of things (IoT), the first property to address is the lattice thermal conductivity. Our recent studies showed that the thermal conductivity at room temperature strongly decreases by alloying Ge with Sn from 46 W/m.K for Ge to 4 W/m.K by increasing the Sn content to 14 at.% [13] (Fig. 7). This result, together with the high electric conductivity are critical material parameters for obtaining a high thermoelectric figure of merit Z_T . Based on the experimental determination of the lattice thermal conductivity (k) the Z_T value were calculated using the electrical conductivity and the Seebeck coefficient obtained from simulations. The calculation reveal Z_T values of > 0.8 for

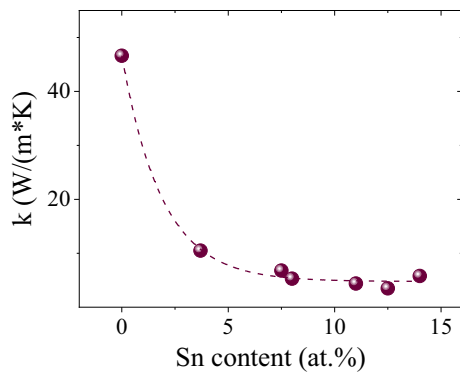


Fig. 7 Experimental thermal conductivity (k) of $\text{Ge}_{1-x}\text{Sn}_x$ layers, $0 \leq x \leq 14$

n-type and > 0.4 for p-type GeSn at 400 K, manifesting the high potential of GeSn for low temperature thermoelectric.

5 Conclusions

The growth of GeSn alloys by CVD with Sn concentrations far beyond the solubility limit is enabled by exothermic chain reactions of hydride radicals (GeH_x , $x = 1, 2, 3$) at the surface permitting to overcome the barriers kinetic surface reactions. This allows for low temperature growth with reasonably large growth rates and high crystalline perfection of the film. The formation of the radicals is governed by gas phase reactions, which will depend on the temperature, the total pressure and the retention time of the molecules in the gas phase. The latter allows for simple methodology to isothermally control the Sn content in Si-Ge-Sn alloys grown by changing the total carrier gas flow, while the pressure of the reactor and the flowrates of the precursors are kept constant. The precise Sn content obtained in high-quality epitaxial layers with sharp interfaces allows the design of different heterostructures. Optically pumped Sn-based lasers are obtained operating at room temperature as well as electrically injected at low temperatures. Vertical gate all around nanowires MOSFETs using GeSn as channel shows 2.5 times higher transconductance compared to the Ge n-FET, demonstrating higher electron mobility of the GeSn layers. The thermal conductivity of GeSn alloys with different Sn content was investigated showing promising values through their application in thermoelectric devices. There are still challenges to overcome but these group-IV materials pave novel paths towards the monolithic integration of multiple functionalities in the current Si semiconductor technology.

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Declarations

Conflict of interest The authors declare that they have no conflict of interest.

Informed consent The manuscript has not been published elsewhere.

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