On the importance of the SrTiO$_3$ template and the electronic contact layer for the integration of phase-pure low hysteretic Pb(Mg$_{0.33}$Nb$_{0.67}$)O$_3$-PbTiO$_3$ layers with Si

Shu Ni[1] · Evert Houwman[1] · Gertjan Koster[1] · Guus Rijnders[1]

Abstract

The rapid advent of the piezoelectric microelectromechanical systems (PiezoMEMS) field has created a tremendous demand for low hysteretic piezoelectric thin films on Si. In this work, we present the integration of epitaxial Pb(Mg$_{0.33}$Nb$_{0.67}$)O$_3$-PbTiO$_3$ (PMN-PT) thin films with Si to enable device fabrication using state of the art methods. With optimized buffer layers and electronic contacts, high-quality low hysteretic PMN-PT thin films are integrated with Si, which is a significant stride towards employing PMN-PT thin film for PiezoMEMS devices. It is found that the processing of the necessary SrTiO$_3$ buffer layer is crucial to achieve the growth of phase-pure perovskite PMN-PT layers on Si. Furthermore, we propose the engineering of the electronic contact for the PMN-PT-on-Si capacitors to obtain low hysteretic polarization and displacement responses.

Keywords Phase-pure · PMN-PT thin films · SrTiO$_3$ buffer layer · Perovskites oxides on Si

1 Introduction

Perovskite oxides display a vast range of functional properties. Among the significant properties are ferroelectricity, piezoelectricity, multiferroicity, colossal magnetoresistance, and high temperature superconductivity [1]. These functionalities present opportunities for numerous technological challenges, such as continuous device downscaling and reducing power consumption [2]. However, it has been a great challenge to implement perovskite oxide thin films in practical devices, as the properties of such films differ from their bulk single crystal properties, in terms of, for instance, strain and defect concentration. The defects in the thin films, such as dislocations and component intermixing, are frequently present at the interfaces between the oxide layers or the substrate/layer interface, which can greatly degrade the functional properties [3]. To tackle this problem, great progress has been made in the last decades to realize atomically controlled growth of perovskite oxide thin films with well-defined interfaces. This was achieved using different deposition technologies, such as Molecular Beam Epitaxy (MBE), Pulsed Laser Deposition (PLD) and Atomic Layer Deposition (ALD) [4]. The controlled growth usually relies on the use of single crystal substrates, such as SrTiO$_3$ (STO), LaAlO$_3$ (LAO), LaAlO$_3$-SrAl$_{0.5}$Ta$_{0.5}$O$_3$ (LSAT) and REScO$_3$ (RE = Dy, Gd, Sm and Nd) [1–4]. These substrates have different unit cell parameters, and one fruitful direction of research was the study of the effect of epitaxial strain on the quality and properties of deposited films. However, it became evident that the use of oxide substrates limits the use of these films in potential device applications because of their high cost, small sizes and their low compatibility with Si-based electronic circuitry and the existing processing tools, such as lithography and etching, which were developed for the semiconductor industry where Si is the standard platform [4]. As a result, different approaches have been investigated to integrate perovskite oxide thin films with Si substrates. It is known that a bare Si surface is highly reactive and an amorphous Si-oxide layer at the interface with the perovskite thin film is usually formed prior to the start of the deposition of the epitaxial perovskite oxide film [1–3]. This presents a challenge to the direct integration of epitaxial oxides with Si because of the loss of registry between the deposited layer and the substrate. To circumvent this

✉ Guus Rijnders
a.j.h.m.rijnders@utwente.nl

1 Inorganic Materials Science Group, MESA+ Institute, University of Twente, 7522 NB Enschede, The Netherlands

problem, various buffer layers have been explored to prevent the oxidation of the Si surface. Tatsuyama et al. first reported the use of SrO as the buffer layer for the overgrowth of an epitaxial $SrTiO_3$ film on Si [5]. A. McKee et al. reported that the exposure of a bare Si surface to an alkaline earth metal (for example Sr or Ba) resulted in an ordered silicide structure, enabling the growth of a $SrTiO_3$ layer in perfect registry with the Si [6]. This work was widely acknowledged as a technological breakthrough and was further optimized by several research groups. Norga et al. from IBM-Zurich utilized the Reflection High-Energy Electron Diffraction (RHEED) phase shift method to monitor the growth of (Ba, Sr)O on Si and thereby determined the impact of the Sr oxidation on the stability of the resulting barrier layer [7]. They confirmed that the deposition of additional metallic Sr at a reduced temperature is crucial to prevent the formation of a Sr terminated layer, which permits the growth of monolayers of (Ba, Sr)O with good crystal quality and largely reduced the number of interfacial Si–O bonds. They further studied the growth of a $SrTiO_3$ layer on top of the (Ba, Sr)O buffered Si and showed that the accurate control of the oxygen exposure and the subsequent annealing is pivotal to avoid undesired interfacial reactions which lead to the formation of SiO_2 and $TiSi_2$ [8]. In addition to $SrTiO_3$, many other template layers, such as yttria-stabilized zirconia/cerium oxide (YSZ/CeO_2), nanosheets and graphene oxide, have been used for the integration of perovskite oxide heterostructures with Si [2, 9]. For example, Chen et al. integrated $LaMnO_3/SrTiO_3$ superlattices with Si employing different buffer layers, including YSZ/CeO_2, $SrTiO_3$-coated $Ca_2Nb_3O_{10}$ nanosheets and reduced graphene oxide and compared their crystalline quality and magnetic properties [10]. Besides using buffer layers, another methodology for the integration is the epitaxial transfer of the perovskite layer grown on a perovskite substrate to a different type of substrate (such as Si) utilizing a sacrificial layer such as $La_{0.7}Sr_{0.3}MnO_3$, $Sr_3Al_2O_6$ and $SrVO_3$ [11–13].

Relaxor ferroelectric $Pb(Mg_{0.33}Nb_{0.67})O_3$-$PbTiO_3$ (PMN-PT) is a promising perovskite oxide for PiezoMEMS devices due to its giant electromechanical coupling and low hysteresis [14]. The excellent piezoelectric performance is associated with the existence of Polar-Nano-Regions (PNRs), which are thought to be highly dynamic and sensitive to external electrical stimulus [15]. However, it is of great challenge to fabricate phase-pure perovskite PMN-PT thin film. Because of the complex composition and the relatively low stability of the perovskite phase, secondary non-piezoelectric pyrochlore phases are often formed, which significantly deteriorate the piezoelectric response. In our previous work, we have achieved epitaxial growth of phase-pure perovskite PMN-PT layer on $SrTiO_3$ (STO) substrates using La-doped $BaSnO_3$ (LBSO) as the tensile mismatched buffered electrode [16]. Here we demonstrate the integration

of phase-pure perovskite PMN-PT thin films on $SrTiO_3$ buffered Si (STO/Si) substrates. The STO/Si substrates are provided by Lumiphase AG and have a 4 nm thick STO buffer layer that was epitaxially grown on the Si using MBE. A $BaSnO_3$ (BSO) layer was first deposited on the STO/Si substrate at 700 °C followed by the growth of the LBSO at 750 °C as the tensile mismatched electrode layer, on which phase-pure perovskite PMN-PT layers could be grown at a high temperature.

It is found that the 4 nm thick STO grown by MBE is critical to prevent the nucleation and growth of the pyrochlore phases in PMN-PT films deposited on Si. An additional STO layer, even as thin as 2 unit cells (u.c.) grown on the STO/Si substrate by PLD, was shown to change the lattice parameters of the subsequent LBSO/BSO layers at the growth temperature of PMN-PT, leading to the formation of pyrochlore phases. Phase-pure perovskite PMN-PT thin films were integrated with Si substrates using LBSO (20 nm)/BSO (20 nm)/STO (4 nm (MBE)) as the buffer layers. The functional properties of PMN-PT capacitors on STO substrates were studied and it was found that a well-engineered electronic contact is crucial to obtain the low hysteretic response of PMN-PT capacitors by avoiding the hysteretic charge exchange between the electrode and the nearby-electrode region in the PMN-PT [16]. Based on these findings, engineering of the electronic contact of the PMN-PT capacitors on Si was performed. The results show that an additional layer of 2 nm $SrRuO_3$ (SRO) between the LBSO and the PMN-PT greatly reduces the hysteresis of the polarization and displacement responses of the PMN-PT capacitors on Si, which agrees well with the results measured on the PMN-PT-on-STO capacitors.

2 Materials and methods

2.1 Sample fabrication

PMN-PT thin films were epitaxially grown on 4 nm STO (grown by MBE) buffered Si substrates (Lumiphase AG, Switzerland) using a double layer stack of BSO and LBSO as the buffer layer. The BSO is employed to reduce the lattice mismatch between the LBSO and the STO layer and the LBSO is utilized as the bottom electrode. All thin film depositions were done by PLD, employing a KrF Excimer laser operating at 248 nm. It was expected that a thicker template layer would possibly be beneficial for the integration of functional perovskite oxide layers with Si because a thicker STO layer is expected to be more stable at the high deposition temperature during subsequent depositions. Therefore, additional STO layers of respectively 2 unit cell (u.c) and 10 u.c (0.8 and 4 nm respectively) were grown on the STO/Si substrates using a commercial single

crystal STO as target. The laser fluence and repetition rate were 2 J/cm² and 2 Hz. The substrate temperature was 600 °C and the oxygen pressure was 0.02 mbar. Subsequently, a 20 nm thick BSO layer was deposited from a commercial ceramic $BaSnO_3$ target, using a laser fluence of 1.3 J/cm² and a repetition rate of 1 Hz. The growth temperature and oxygen pressure were 700 °C and 0.13 mbar. After the BSO deposition, a 20 nm thick LBSO layer was deposited as the bottom electrode for which a commercial $La_{0.07}Ba_{0.93}SnO_3$ ceramic target was used. The laser fluence and repetition rate were 1.3 J/cm² and 1 Hz, the deposition temperature was 750 °C and the oxygen pressure 0.13 mbar. For some samples a 2 nm thick SRO layer was deposited on top of the LBSO. 800 nm thick PMN-PT thin films were subsequently grown on the LBSO layer from a commercial $(Pb_{1.1}(Mg_{0.33}Nb_{0.67}))O_3)_{0.67}$-$(Pb_{1.1}TiO_3)_{0.33}$ target (hence with a 10% extra Pb-content to compensate for the Pb loss due to the volatile character of ablated Pb) at a fluence of 2.0 J/cm², a repetition rate of 20 Hz, at a growth temperature of 600 °C, in an oxygen pressure of 0.25 mbar. To be able to characterize the electrical responses of the PMN-PT films, a 50 nm thick top SRO electrode was deposited. All SRO layers were grown from a ceramic $SrRuO_3$ target using a laser fluence of 2.0 J/cm², a deposition rate of 4 Hz, in an oxygen background pressure of 0.25 mbar at a growth temperature of 600 °C. All oxide layers grown by PLD were deposited without breaking the vacuum. The top electrode was patterned by photolithography and Ar-ion beam etching to form parallel plate capacitor structures.

2.2 Sample characterization

The crystallographic properties of the thin films were characterized by X-ray diffraction (XRD, Panalytical MRD). The film surface was investigated by Atomic Force Microscopy (AFM, Bruker). The polarization responses were characterized with an aixACCT TF-2000 analyzer, combined with a Double Beam Laser interferometer (DBLI) for displacement measurements. In the electrical measurements a triangular bipolar excitation voltage wave with different amplitudes and a constant scan frequency of 1 kHz was used. In all electrical measurements the bottom electrode was grounded, and silver paste was applied at the side of the sample. The top electrode and the silver paste was contacted by metal probes. Before all polarization and displacement measurements the capacitors were pre-poled with a negative half voltage cycle, preparing the polarization in the top-to-bottom electrode direction. The amplitude and duration of the pre-poling pulse are identical to the values used for the voltage wave in the following polarization and displacement measurements.

3 Results and discussion

3.1 Crystallographic properties

Figure 1 shows the XRD 2θ–θ spectra of the PMN-PT layers grown on the different LBSO/BSO/STO/Si templates. A phase-pure perovskite PMN-PT layer is only obtained when the PMN-PT layer is grown on LBSO/BSO/STO(MBE)/Si. The presence of an additional STO layer, deposited by PLD, causes the formation of pyrochlore phases in the PMN-PT films. An ω scan was performed for the (002) reflection of the phase-pure perovskite PMN-PT film, shown in the inset of Fig. 1. The FWHM of the rocking curve is about 0.6°, which is close to the value obtained for high quality perovskite oxide films grown on single crystal perovskite substrates.

From our earlier study on the growth of PMN-PT on single crystal STO substrates, we found that a tensile mismatched template is crucial to stabilize the perovskite phase of the resulting PMN-PT thin films and to prevent the formation of pyrochlore phases [16]. Based on this finding, we performed Reciprocal Space Mapping (RSM) of the LBSO/BSO heterostructure at the growth temperature of PMN-PT (600 °C) to gain more insight into the lattice mismatch between the PMN-PT layer and the underlying template layers under growth conditions. The RSM was performed around the (103) reflection and the results are given in Fig. 2. Because of the low concentration of La, the bulk lattice parameters of LBSO and BSO are similar (4.11
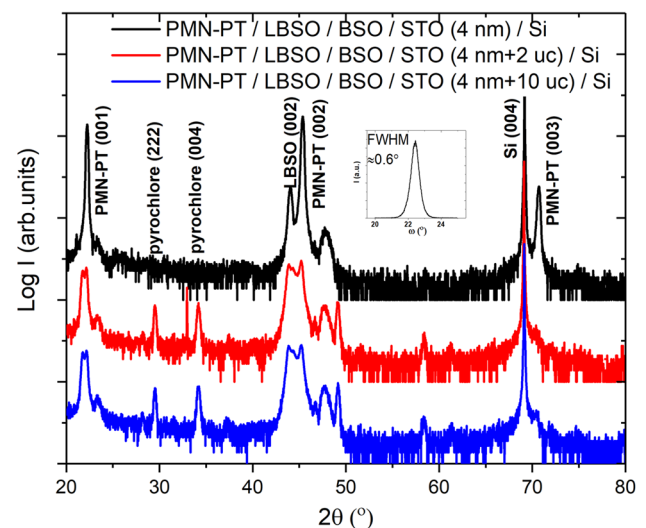
Fig. 1 XRD θ–2θ scans of PMN-PT films grown on SrTiO₃ (grown by MBE) buffered Si with different additional STO layers (grown by PLD); the inset shows the rocking curve around the (002) reflection of phase-pure perovskite PMN-PT grown on LBSO/BSO/STO(MBE)/Si
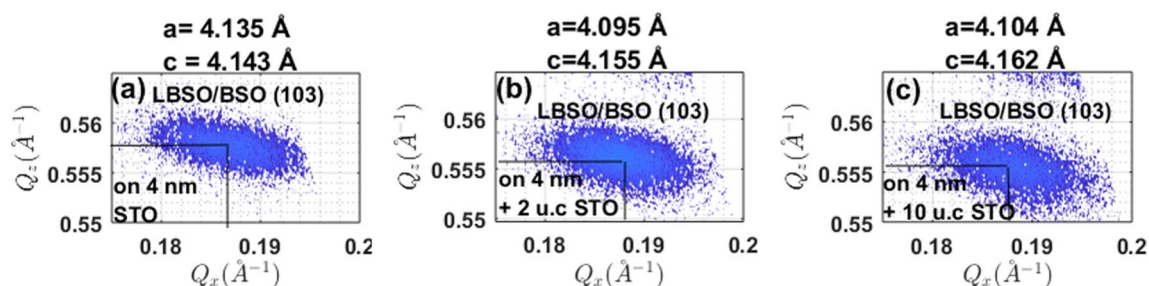
Fig. 2 Reciprocal space mapping (RSM) around (103) reflections of LBSO/BSO grown on **a** STO (4 nm, MBE)/Si. **b** STO (4 nm (MBE) + 2 u.c (PLD)). **c** STO (4 nm (MBE) + 10 u.c (PLD)), measured at the PMN-PT deposition temperature of 600 °C

and 4.10 Å, respectively [17]). As a result, the reflections of both layers in the RSM show up as a single peak as one may expect from the small differences between the lattice parameters. The in-plane and out-of-plane (average) lattice parameter values of the LBSO layer were obtained from the maximum intensity value of the RMS-peak and are given in Table 1.

From Fig. 2, we can see that the out-of-plane components of the (103) reflections of LBSO/BSO continuously shift to lower reflection angle, hence larger *c*-axis lattice parameter, when grown on a thicker STO layer, indicating the increasing tetragonality at this high temperature. The deduced tetragonality values are summarized in Table 1. It is known that perovskites generally start to grow cube on cube on a perovskite template layer at high temperature. In case of a large lattice mismatch this gives rise to large strain in the initial growth layer. As shown in Table 1, the additional STO layer grown PLD leads to a reduced tensile mismatch between LBSO/BSO and PMN-PT. We believe the reduced tensile mismatch at the growth temperature results in the formation of pyrochlore phases in the PMN-PT films.

3.2 Surface morphologies

Figure 3a–c depict the surface morphologies of the 4 nm STO grown by MBE directly on Si, and the 4 nm + 2 u.c and 4 nm + 10 u.c additional STO layers grown by PLD. All show smooth surfaces with peak-to-peak height differences less than 1 nm. The surface of the STO layers deposited by

PLD exhibit relatively lower height differences and noticeable smaller lateral grain sizes than the STO layer deposited by MBE, as can be seen from the line scans in the insets. Figure 3d–f give the surface morphologies of the LBSO films grown on these STO templates. The LBSO layers exhibit similar topological surface features: interconnected grains with particles. The peak-to-peak height differences of the LBSO/BSO film that was directly grown on the STO (4 nm MBE)/Si substrates (around 1 nm) are slightly lower than those with an additional PLD grown STO layer (around 1.5 nm). Figure 3g–i show the surface morphology of the resulting PMN-PT layers. The surface of the phase-pure perovskite PMN-PT layer grown on STO (4 nm, MBE)/Si (Fig. 3g) shows granular features, indicating island growth of PMN-PT. Clustered columns are observed for the PMN-PT layers grown on the substrates with additional PLD grown STO layers (Fig. 3h, i), which we attribute to pyrochlore phases.

3.3 Electrical properties

In our previous work on the electronic contact engineering of PMN-PT capacitors on STO substrates [16], we have shown that engineering the bottom electrode by adding a thin SRO layer on top of the LBSO is very important to obtain low hysteretic responses of the PMN-PT capacitors on STO. It was concluded that a defective, dielectric layer of low permittivity is present at the LBSO/PMN-PT interface that causes hysteretic charge exchange under high external

Table 1 Tetragonality (*a/c*), pseudocubic lattice parameters a_{pc} of LBSO/BSO heterostructure and the lattice mismatch between PMN-PT and LBSO/BSO at the growth temperature of PMN-PT deduced from Fig. 2

SrTiO$_3$ thicknesses	a_{pc} (LBSO/BSO) (Å)	a/c (LBSO/BSO)	Mismatch between PMN-PT and (LBSO/BSO) (%)
4 nm	4.137	1.002	+ 2.68
4 nm + 2 u.c	4.115	1.014	+ 2.13
4 nm + 10 u.c	4.123	1.014	+ 2.33

*a_{pc} (PMN-PT) = 4.029 Å at 600 °C (see SI1)

STO surface
## LBSO surface
PMN-PT surface
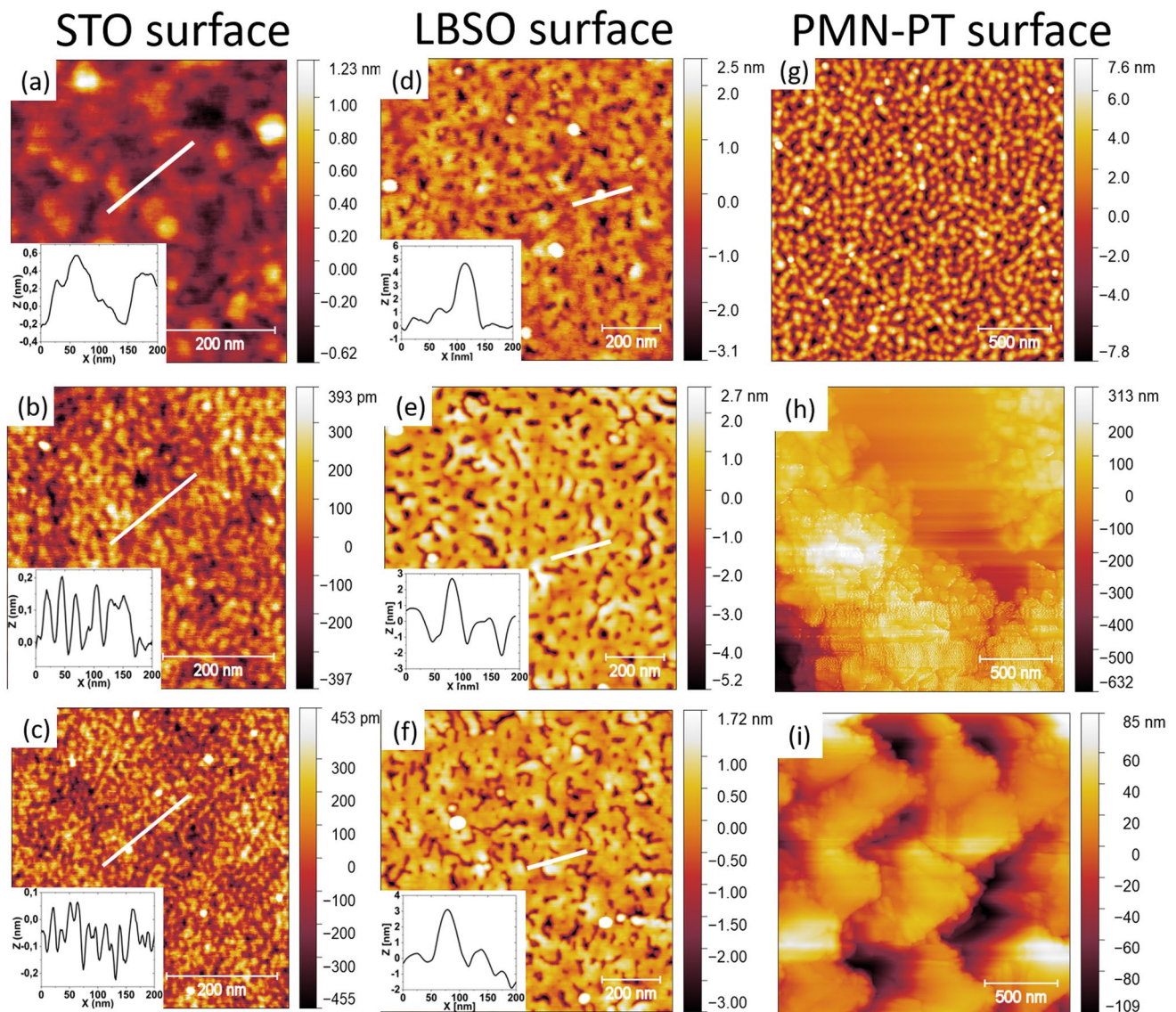
Fig. 3 AFM images of the surface morphology of subsequently grown STO, LBSO and PMN-PT layers on Si. **a–c** Surface morphology of 4 nm STO(MBE), 4 nm + 2.u.c STO (PLD) and 4 nm + 10 u.c STO (PLD). **d–f** idem for the LBSO (20 nm)/BSO (20 nm) layer. **g–i** idem for 800 nm PMN-PT layer grown on the LBSO/BSO/STO template multilayer on Si

electrical fields. By adding a 2 nm thick SRO layer, this effect can be strongly suppressed, and the resulting capacitors exhibit nearly ideal relaxor ferroelectric response with minimal hysteresis.

Based on this result, the bottom LBSO electrode of the present devices on Si was also complemented with an additional 2 nm thick SRO layer, before the growth of the PMN-PT layer. Figure 4a and b show the polarization responses of the SRO/PMN-PT/LBSO/BSO/STO(MBE)/Si and the SRO/PMN-PT/SRO/LBSO/BSO/STO(MBE)/Si capacitors. It is seen that the polarization responses of PMN-PT-on-Si capacitors exhibit similar electrode dependence as the equivalent devices on STO substrates

(see Fig. 4.3 in Ref. [16]). A significant polarization hysteresis is observed for the capacitors in which the PMN-PT layer is in direct contact with the LBSO bottom electrode (Fig. 4a); the coercive fields, remanent polarizations and maximum polarizations increase with increasing maximum applied field, and the P-E loops exhibit the non-saturated feature (opening at the tip) at the maximum applied fields. By insertion of the 2 nm thick SRO layer between the LBSO and the PMN-PT, the hysteresis of the polarization and the coercive fields are strongly reduced. The piezoelectric responses are given in Fig. 4c and d. The piezoelectric performance was characterized by the
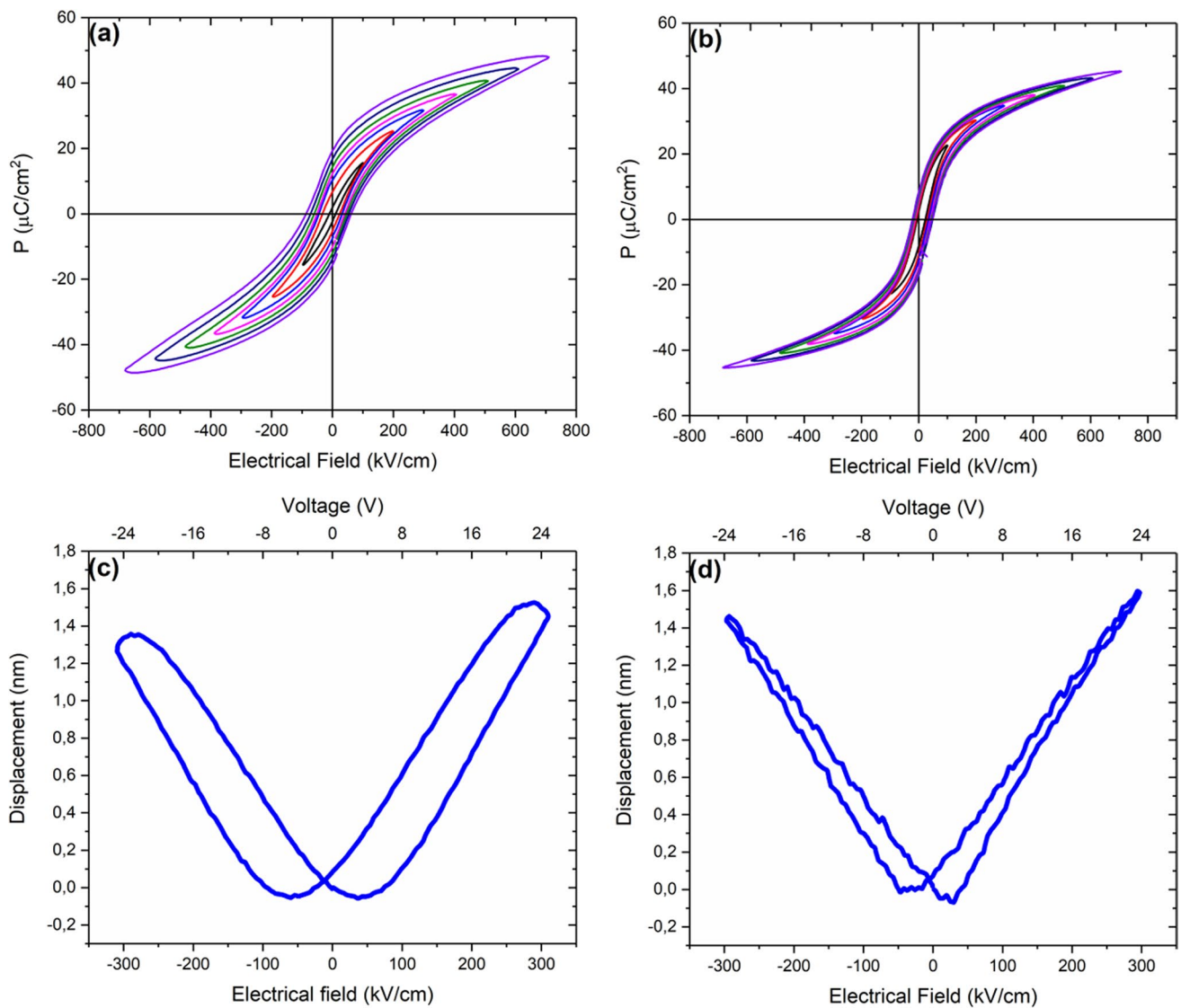
Fig. 4 Polarization-Electrical field (P-E) and Displacement-Electrical field (D-E) loops of PMN-PT capacitor on Si. **a, b** P-E loops of SRO/ PMN-PT/LBSO/BSO/STO(MBE)/Si and SRO/PMN-PT/SRO/LBSO/ BSO/STO(MBE)/Si capacitors. **c, d** idem for Displacement-Electrical field loops

large signal coefficient (D_{max}/V_{max}), which is calculated to be 62.5 pm/V for both SRO/PMN-PT/LBSO/BSO/ STO(MBE)/Si and SRO/PMN-PT/SRO/LBSO/BSO/ STO(MBE)/Si capacitors, where D_{max} is the maximum measured displacement and V_{max} the maximum applied voltage. Although there is no significant difference in the piezoelectric coefficient, the PMN-PT-on-LBSO capacitors (Fig. 4c) show much stronger displacement hysteresis than the PMN-PT-on-SRO capacitors (Fig. 4d). These results further demonstrate the importance of the well-engineered electronic contact for obtaining low hysteretic responses of PMN-PT capacitors on both STO and

Si substrates by suppressing hysteretic charge injection processes.

4 Conclusions

In this work, we have shown that phase-pure perovskite PMN-PT thin films can be integrated with Si substrates for potential device applications. It is found that the STO template plays a crucial role in the integration: the STO layer influences the lattice constants of the LBSO/BSO heterostructures at the growth temperature of PMN-PT. This is possibly associated with the different surface morphology

of the STO layer and therefore varied nucleation densities during the following growth of LBSO/BSO. The lattice constants of the LBSO/BSO determine whether the formation of pyrochlore impurities in the PMN-PT layer occurs or not.

Secondly, engineering of the electronic contact was performed by adding an additional 2 nm thick SRO layer between LBSO and PMN-PT. The results show that the capacitors on Si exhibit more hysteresis but similar dependence on the electronic contact compared with these capacitors on a bulk STO substrate: an extra 2 nm SRO layer between the PMN-PT and the LBSO greatly reduces the hysteresis. The larger hysteresis of PMN-PT on Si can possibly be attributed to the strain induced by the thermal mismatch between Si and perovskite oxides.

Data availability Data available on request from the authors.

Declarations

Conflict of interests The authors declare no conflict of interest.

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