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Research paper

A fully integrated CMOS 60-GHz transceiver for IEEE802.11ad applications

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Abstract: A fully integrated 60-GHz transceiver for 802.11ad applications with superior performance in a 90-nm CMOS process versus prior arts is proposed and real based on a field-circuit co-design methodology. The reported transceiver monolithically integrates a receiver, transmitter, PLL(Phase-Locked Loop) synthesizer, and LO (Local Oscillator) path based on a sliding-IF architecture. The transceiver supports up to a 16QAM modulation scheme and a data rate of 6 Gbit/s per channel, with an EVM (Error Vector Magnitude) of lower than −20 dB. The receiver path achieves a configurable conversion gain of 36~64 dB and a noise figure of 7.1 dB over 57~64 GHz, while consuming only 177 mW of power. The transmitter achieves a conversion gain of roughly 26 dB, with an output P_{1dB} of 8 dBm and a saturated output power of over 10 dBm, consuming 252 mW of power from a 1.2-V supply. The LO path is composed of a 24-GHz PLL, doubler, and a divider chain, as well as an LO distribution network. In closed-loop operation mode, the PLL exhibits an integrated phase error of 3.3º rms (from 100 kHz to 100 MHz) over prescribed frequency bands, and a total power dissipation of only 26 mW. All measured results are rigorously loyal to the simulation.

Key words: 60 GHz, transceiver, CMOS, sliding IF, circuit/EM co-design, LNA, PA, PGA

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1 Introduction

High-speed wireless communication and data streaming have become increasingly attractive in both academia and industry over the past decade. Wireless transceivers working in the 7-GHz unlicensed ultrawide band around 60-GHz have drawn significant attention from scientists and engineers worldwide over the past five years[1-8]. Next-generation Wi-Fi in the IEEE802.11ad standard[9,10] and next-generation (5G) mobile communication are capable of supporting wireless applications such as real-time data synchronization, full-HD video streaming, and high-speed wireless links up to 10 Gbit/s with capacity boosting of 1 000 times and <1 ms of latency[11-14].

In addition to with the aggressive scaling of modern CMOS(Complimentary Metal-Oxide-Semiconductor) technology, the current gain cutoff frequency (f_T) and maximal oscillation frequency

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(f_{MAX}) are extended well over 200 GHz (e.g., in a 90/65-nm process node or beyond), which makes millimeter-wave (mm-wave) integrated circuits and transceivers feasible in CMOS technologies. This enables mass production, high integration, and cost reduction when compared with their compound and III-V counterparts[15].

Challenges of 60-GHz CMOS circuit design include the performance degradation of active components (e.g., MOSFETs) and the serious parasitic effects of passive components (e.g., substrate loss, fringe effects, the CRP (Current-Return-Path) of inductors[16], a degraded quality factor (Q), and coupling between components with large footprints at the mm-wave frequency band, which prevents the accurate prediction of performance in measurements at a presilicon stage)[17]. In addition, the design margin is tight at such a high frequency; therefore, the accurate prediction of circuit performance from simulations based on a novel design methodology before tapeout is highly anticipated.

In this paper, a fully integrated 60-GHz CMOS transceiver with sliding-IF architecture for multi-Gbit/s wireless communication applications is presented and implemented in a 90-nm CMOS technology that is based on a proposed field-circuit co-design paradigm. The 60-GHz receiver consists of a differential LNA(Low-Noise Amplifier) with neutralization and transformer/transmission line (T-line) interstage matching techniques, a double-balanced RF(Radio-Frequency) mixer with inductive series peaking, a double-balanced I/Q down-conversion IF(Intermediate-Frequency) mixer, and a wide-band low-power PGA(Programmable Gain Amplifier).

To attain the wide-band characteristics of the PGA, a modified Cherry-Hooper amplifier with a negative capacitive neutralization technique is employed, and a novel circuit technique for gain adjustment is adopted. The 60-GHz transmitter is designed with a differential PA(Power Amplifier) with two-way power combining, a double-balanced RF up-conversion mixer, and a double-balanced I/Q up-conversion IF mixer. A LO (Local Oscillator) path is implemented with a PLL (Phase Locked Loop) synthesizer, followed by a doubler and divider chain with T-line networks, for the generation of LO signals of RF and IF mixers in both receiver and transmitter paths.

In this work, well-designed mm-wave circuits based on T-lines and transformers minimize the necessity for layout-dependent parasitic extraction for inherent regular structures and well-defined current return paths. Meanwhile, optimized circuit and EM (Electromagnetic) co-design paradigms are also proposed and incorporated, improving the accuracy of circuit simulations at mm-wave frequencies. The proposed transceiver front end supports a 7-GHz ultrawide bandwidth of approximately 60 GHz with three 2.16-GHz channels based on the 802.11ad standard, supporting up to a 16QAM modulation scheme and a data rate of 6 Gbit/s per channel. The measurement results of the 60-GHz CMOS transceiver are rigorously loyal to the simulation, showing competitive performance in a 90-nm process compared with prior arts in advanced processes.

This paper is organized as follows. Section 2 introduces the proposed circuit and EM co-design paradigm for millimeter-wave circuits. Section 3 elaborates on the design of the proposed 60-GHz transceiver. Measurement results for the transceiver and a system demo of Gbit/s data streaming based on the proposed transceiver are discussed in Section 4. Finally, conclusions are presented in Section 5.

2 Circuit and EM co-design methodology for millimeter-wave integrated circuits

Conventional RF designs for <6-GHz applications typically adopt a classical IC design flow, in which

passive and active devices are described by equivalent circuits from modeling, while parasitics are incorporated from post-layout extractions. However, parasitic effects of passive components (e.g., substrate loss, fringe effects, and coupling) seriously degrade the accuracy of circuit models at millimeter-wave frequencies. Meanwhile, current-return-path and connection parasitics of active components also become pronounced, and are not well considered in conventional design paradigms, as shown in Fig.1.

In millimeter-wave IC designs, passive and active components with closed or well-defined EM structures and CRPs are preferred to improve the accuracy of design and simulation, which calls for the applications of T-lines and transformers. T-lines have an inherent closed EM structure, well-defined connection parasitics, and CRPs, and can be flexibly used for impedance matching and connections[18]. Transformers can also be easily designed with EM simulations and compactly laid out for matching and dc blocking purposes[19,20]. On the other hand, active components (e.g. MOSFETs) are locally with compact footprint, which can be well described by parasitic extraction methodologies. Furthermore, global connection parasitics must be considered with the assistance of EM simulations. Eventually, the above discussions result in an EM-circuit co-design methodology, as shown in Fig.1.

In the design paradigm shown in Fig.1, active devices (e.g., MOSFETs with well-defined local connection parasitics and CRP) are extracted at first, considering all resistive and capacitive parasitics. Passive devices such as T-lines and transformers for matching and global connection purposes are extracted by an EM simulation to include coupling and parasitic effects at millimeter-wave frequencies. Both parts are eventually merged in the final simulation with possible iterations to improve the convergence.

3 Circuit design of the 60-GHz transceiver

3.1 Transceiver architecture

The proposed transceiver adopts a super-heterodyne architecture[21] composed of a three-stage LNA, a three-stage PA with two-way power combining, double-balanced down-conversion and up-conversion RF mixers, double-balanced down-conversion and up-conversion I/Q IF mixers, a PGA, a PLL followed

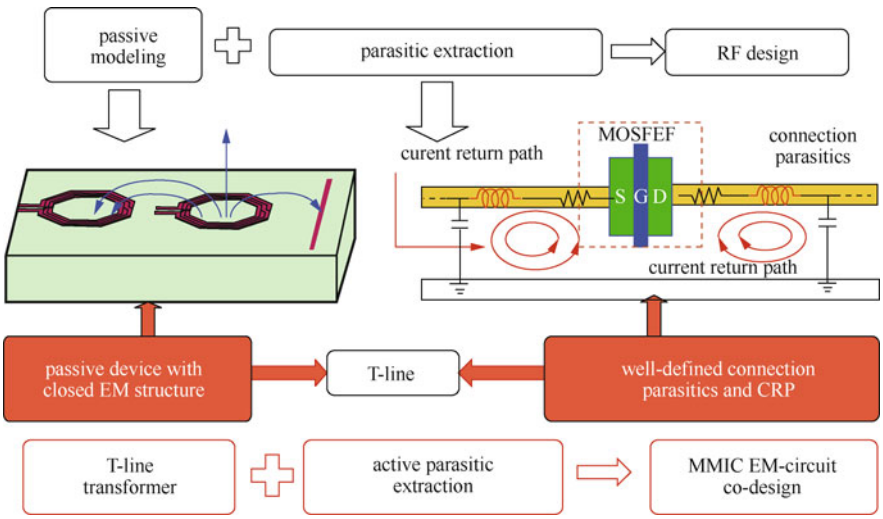

Figure 1 Proposed circuit and EM co-design methodology

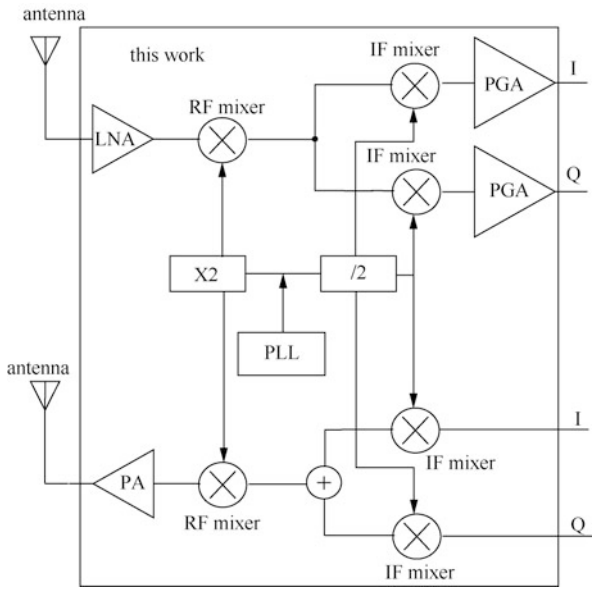

Figure 2 Block diagram of proposed 60-GHz super-heterodyne transceiver with sliding-IF architecture

by an LO doubler, and a CML(Current Mode Logic) divide-by-2 divider[22], as shown in Fig.2. An RF signal approximately 60 GHz from the antenna is first amplified by the LNA with single-to-differential conversion, subsequently mixed with an 48-GHz LO signal at the RF mixer, and down-converted to IF around the 12-GHz band.

The differential IF signal is further mixed with a 12-GHz LO at the I/Q IF mixer to eventually down-convert the received RF signal to analog baseband, where a PGA is incorporated for gain adjustment. In the transmitter path, baseband I/Q inputs are first up-converted to a 12-GHz carrier by IF mixers, and added together before being up-converted to the 60-GHz carrier by the RF mixer. The signal is further fed into a PA for amplification and power delivery to the antenna. The 48-GHz and 12-GHz LOs for the RF and IF mixers are generated from a 24-GHz PLL, followed by a doubler and a divider. Frequency planning following the 802.11ad standard comes up with three corresponding LO frequencies at 23.328 GHz, 24.192 GHz, and 25.056 GHz, respectively.

3.2 LNA

LNA is required with high gain and low noise figures to suppress the noises of the following stages in a receiver. A three-stage differential LNA with a transformer and T-line matching networks is proposed, as shown in Fig.3. The last stage is designed with conjugated matching, while the first two stages adopt optimal noise matching. Neutralization is used to improve the gain and stability of the differential pair, and the capacitance is

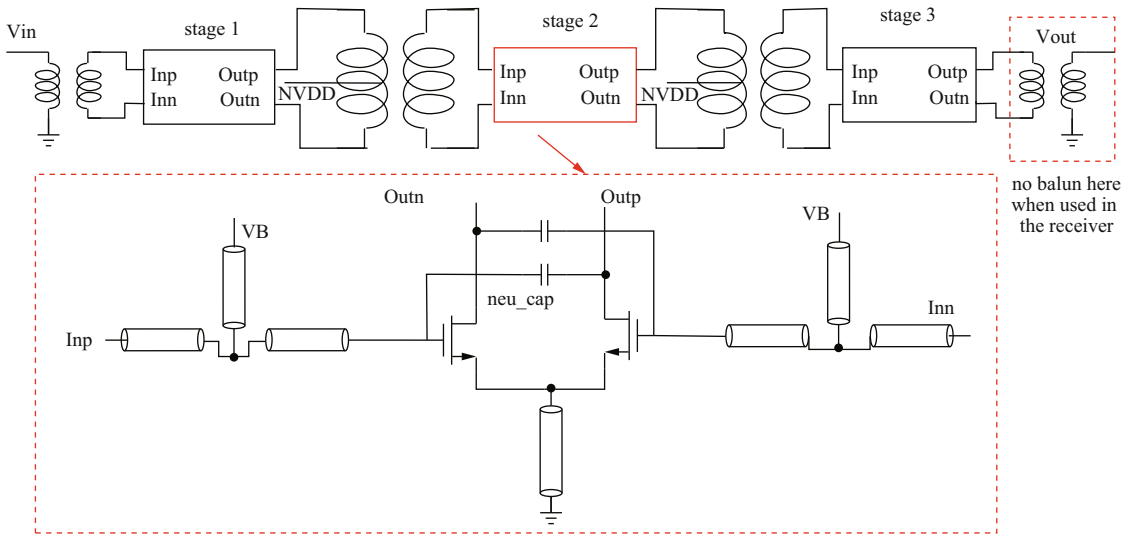

Figure 3 Topology of proposed LNA

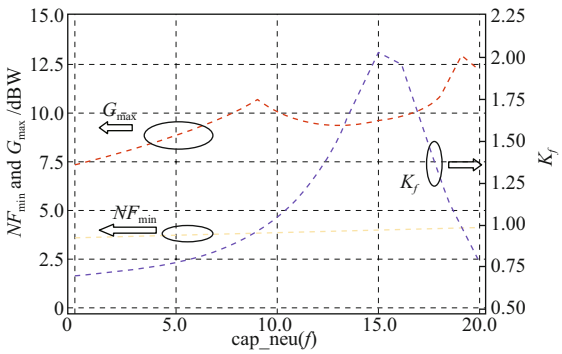

Figure 4 K_f, NF_{min}, and G_{max} vs. neutralization capacitance

chosen around 15 fF for a 2-dB enhancement on the gain and only a 0.1-dB degradation on the NF (Noise Figure), as shown in Fig.4. A T-line is incorporated in the common-source node of the differential pair to ensure common-mode stability. All MOSFETs are biased at a current density of 0.13 mA/μm to optimize their noise performance[23]. A transformer is used for interstage matching and dc blocking purposes with an insertion loss of less than 1 dB.

In the design, all the T-lines are optimized based on the scalable model extracted from an EM simulation[18], minimizing any exhausted iterations. Further, Calibre PEX is used for parasitic extractions around MOSFETs, while other passive devices, including connections are optimized by an EM simulation, following the proposed methodology in Section 2. The LNA shows a simulated maximal gain of 19.5 dB, a minimal noise figure of 6 dB, and an IIP3 of −6.9 dBm with a 3-dB bandwidth of over 9 GHz.

3.3 PA

PA is required with a high output power and linearity to deliver the signal power to the antenna with minimized compression. A three-stage differential PA with transformer-based two-way power combining and T-line matching networks is proposed, as shown in Fig.5. The last stage is designed with load-pull power matching, while the first two stages adopt optimal conjugated matching. Neutralization is also utilized to improve the gain and stability of the differential pair, following a similar design method as the LNA, with a T-line incorporated in the common-source node of the differential pair to ensure common-mode stability. All MOSFETs are biased at a current density of 0.25 mA/μm to optimize the gain and power performance[23]. A transformer is also used for interstage matching and dc blocking purposes with an insertion loss of less than 1 dB.

Following the design methodology in Section 2, the PA achieves a simulated maximal gain of 19.7 dB; output $P_{1\,dB}$ and P_{SAT} of 10.5 dBm and 14 dBm, respectively; and a PAE(Power-Added Efficiency) of 14%.

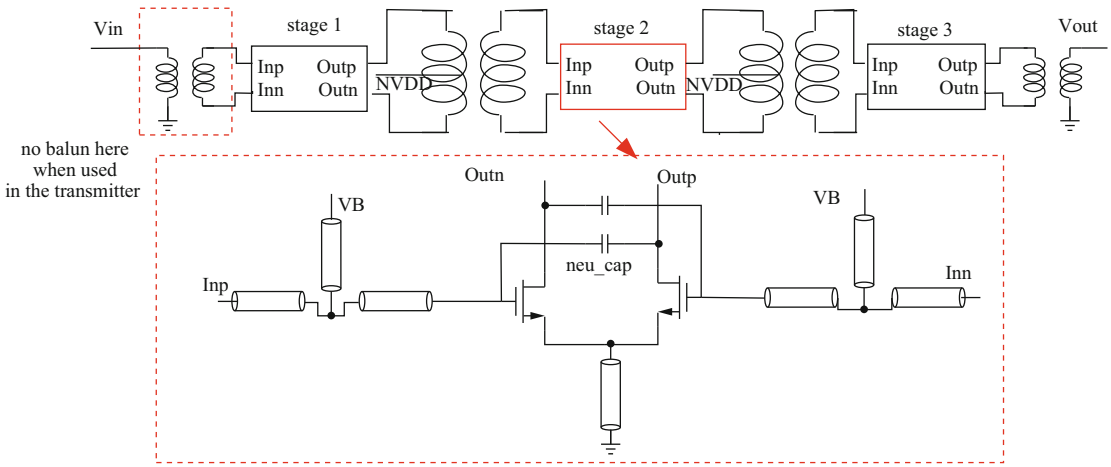

Figure 5 Topology of proposed PA

3.4 PLL

A 24-GHz PLL is designed with an integer-N topology for the purpose of simple tuning and superior phase noise, as shown in Fig.6. A VCO (Voltage-Controlled Oscillator) buffer, whose supply voltage can be tuned, is connected to the VCO. Three CML divide-by-2 dividers, serving as prescaling, are cascaded after the VCO buffer to bring the frequency below 4 GHz, which is readily divided by the MMD (Multimodulus Divider) before being fed into the PFD (Phase-Frequency Detector), CP (Charge Pump), and loop filter for comparison with the reference.

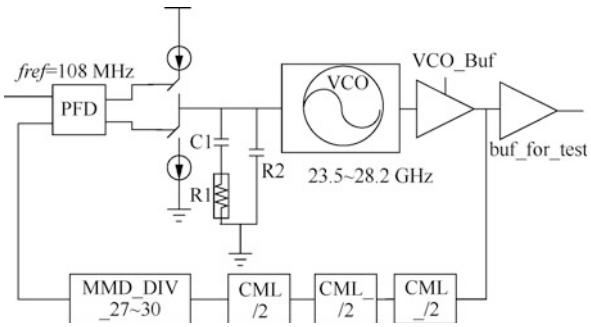

Figure 6 Proposed 24-GHz integer-N PLL with frequency planning

The VCO adopts an nMOS cross-coupling structure, as shown in Fig.7. In order to ensure sufficient swing to drive the CML divider, a common-source buffer is cascaded with the VCO, whose supply voltage is tunable for a compromise between the power and output swing. A 4-bit switched capacitor array is used for digital coarse tuning, and a varactor is used for fine tuning. Owing to the switching of fixed capacitors, K_{VCO} changes over frequency bands.

Owing to the PLL stability requirement over a wide band, e.g. 60-GHz applications, maintaining a constant LBW(Loop Bandwidth) is mandatory. This calls for a constant K_{VCO}[24-26]. In order to compensate for the K_{VCO} variation, a 2-bit switched varactor array is implemented together with the switched capacitor array. Simulation shows a K_{VCO} of 1.05 GHz/V with less than 13% of variation over frequency bands, as opposed to an over −40% variation without compensation, as shown in Fig.8. Furthermore, tail feedback is used to improve the phase noise by modulating the tail current, as shown in Fig.7. The average noise current over one period is reduced by modulating the ISF(Injection Sensitivity Function)[27]. The simulation in Fig.8 shows a 2-dB improvement

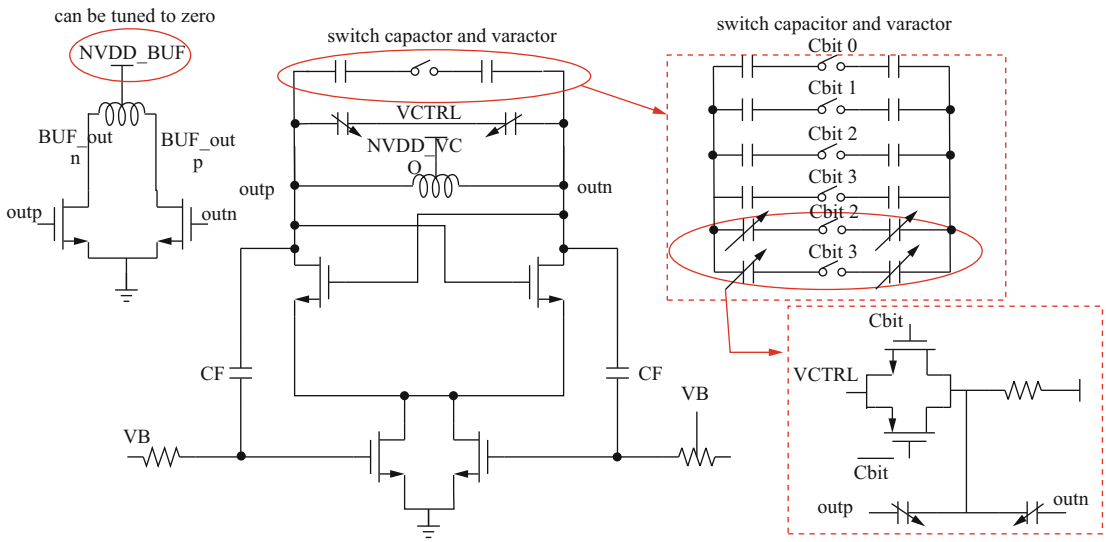

Figure 7 VCO with proposed switched capacitor and varactor arrays

in the phase noise. The phase noise at a 1-MHz offset is −103 dBc/Hz while consuming 11 mW of power without buffer.

A schematic of the charge pump is shown in Fig.9. A feedback amplifier is used to copy the current of the left branch to the right, minimizing the static current mismatch of the charge pump. MOSFETs M11 and M12 are used to reduce the clock feedthrough effect, while M9 and M10 give low resistance discharge paths when M5 and M8 are off, reducing the dynamic current mismatch. A simulation of the PLL in the locking state shows that the ripple on the control voltage is below 1 mV, as shown in Fig.8, resulting in a spur of lower than −60 dBc.

3.5 Doubler and divider

The doubler extracts the second-order harmonic of

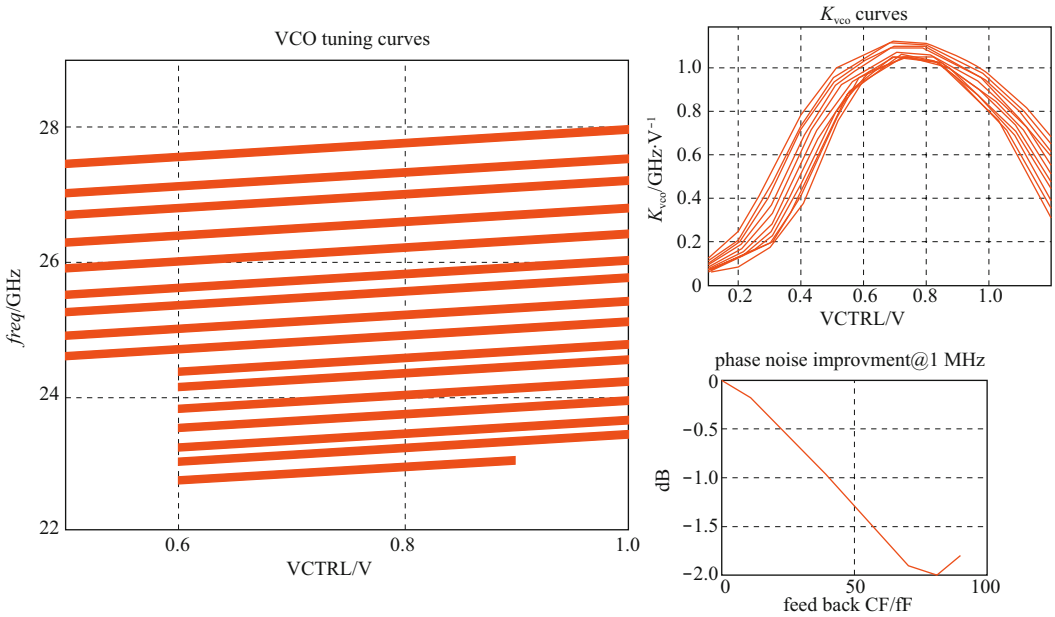

Figure 8 VCO tuning curves and phase noise improvement with tail-feedback technique

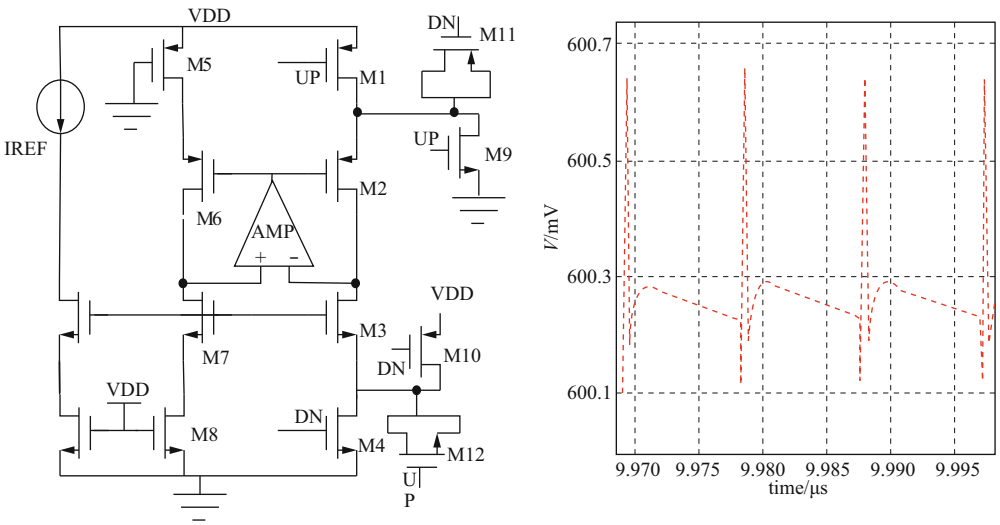

Figure 9 Charge pump structure and simulated output locking state

the LO and amplifies the signal to drive the RF mixer. The matching network in the doubler also utilizes a T-line similar to the LNA and PA. A CML divider with inductor peaking is implemented to generate second LO signals with sufficient swing to drive the IF mixers. A resistor is paralleled to de-Q the peaking inductor to trade the dividing range with an output swing, as shown in Fig.10.

3.6 Down-conversion mixers and PGA

Both down-conversion RF and IF mixers are designed with a double-balanced structure. To reduce the noise figure, two inductors are used at the drains of the tail MOSFETs in the RF mixer for series peaking, as shown in Fig.11.

The main challenges of the PGA are the wideband and high-gain requirements in the analog baseband. To attain wideband characteristics, a modified Cherry-Hooper amplifier with a negative capacitive neutralization technique is employed, and a novel circuit technique for gain adjustment is also adopted. In order to achieve gain control, each gm cell is partitioned into several unit cells, where digitally

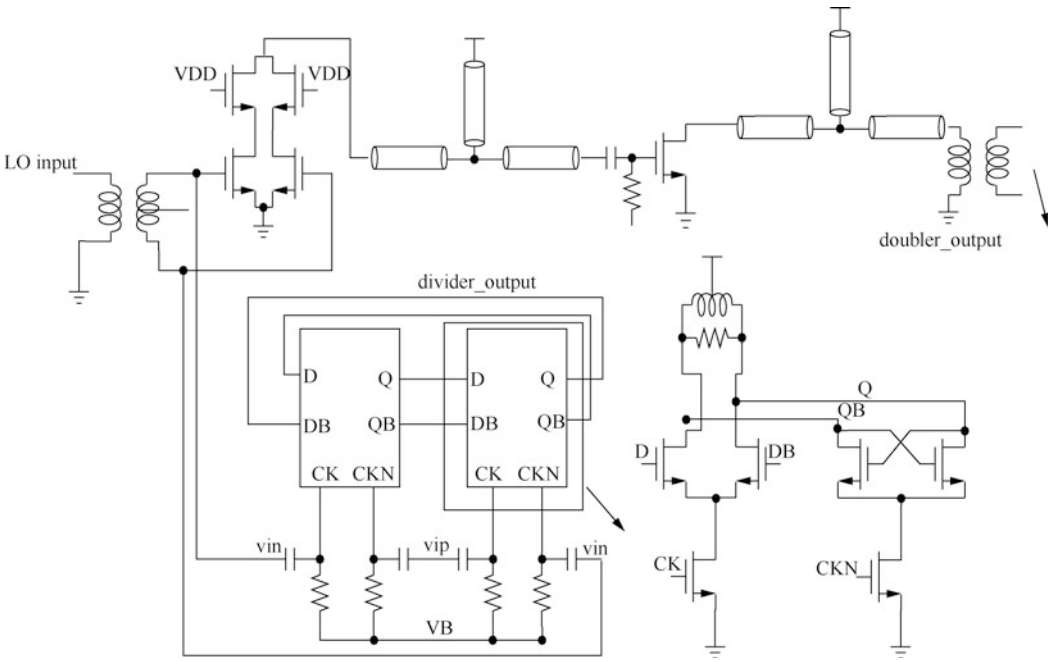

Figure 10 Schematic of LO path with doubler and divider

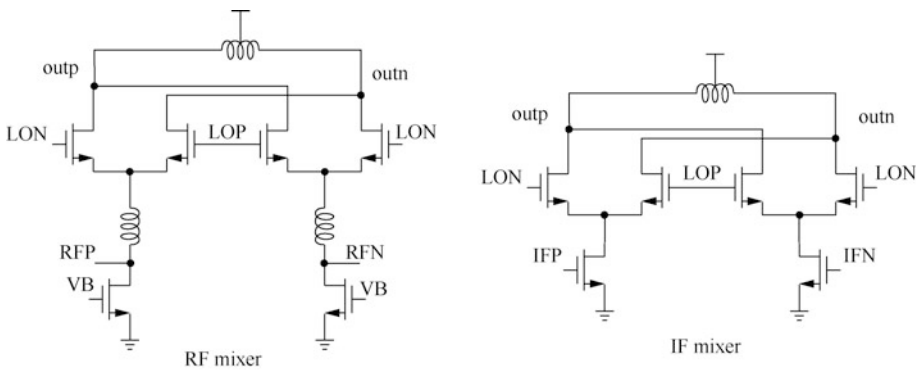

Figure 11 Circuit schematics of down-conversion RF and IF mixers

controlled shunting switches across the sources of the gm-cell devices turn each cell on/off in differential mode without affecting the common-mode bias. The structure of the PGA is shown in Fig.12.The simulation shows a maximal and minimal gain of 48 dB and 20 dB, respectively, with a 3-dB bandwidth above 3 GHz in all corners, as shown in Fig.13.

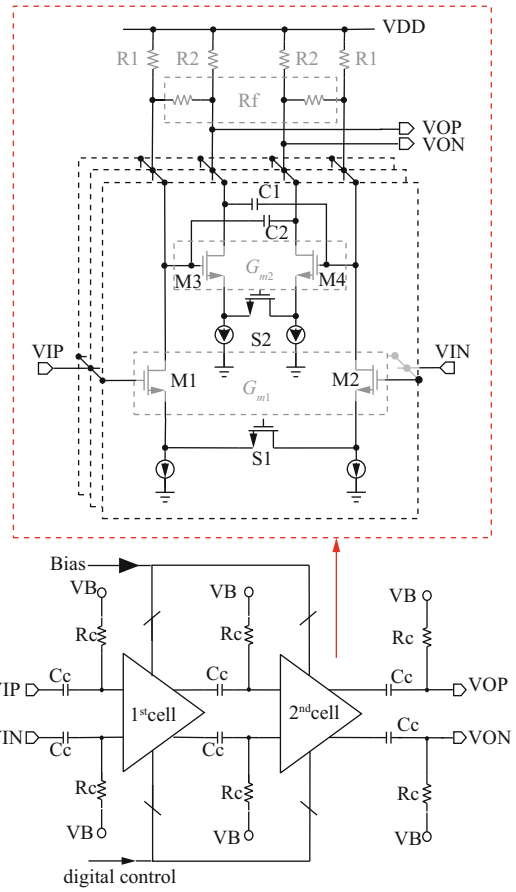

Figure 12 Schematic of proposed PGA

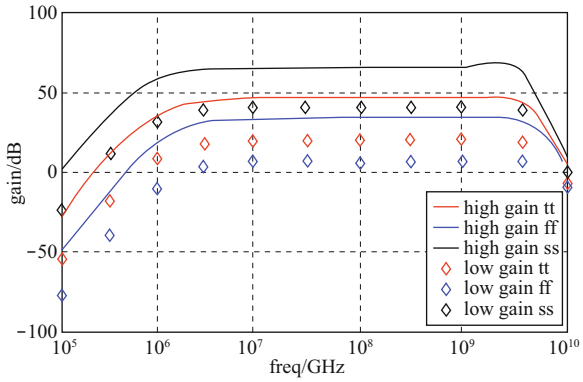

Figure 13 Simulated gain amd frequency curves over corners of the PGA

3.7 Up-conversion mixers

Both the up-conversion RF and IF mixers are designed with a double-balanced structure. The output summing of the IF mixers is implemented in current mode, as shown in Fig.14.

4 Measurement results

The entire transceiver and stand-alone LNA, PA, and PLL are designed and realized using a standard 90-nm CMOS process. A die microphotograph of the transceiver is shown in Fig.15.

4.1 LNA

Fig.16 shows the die microphotographs of the LNA.

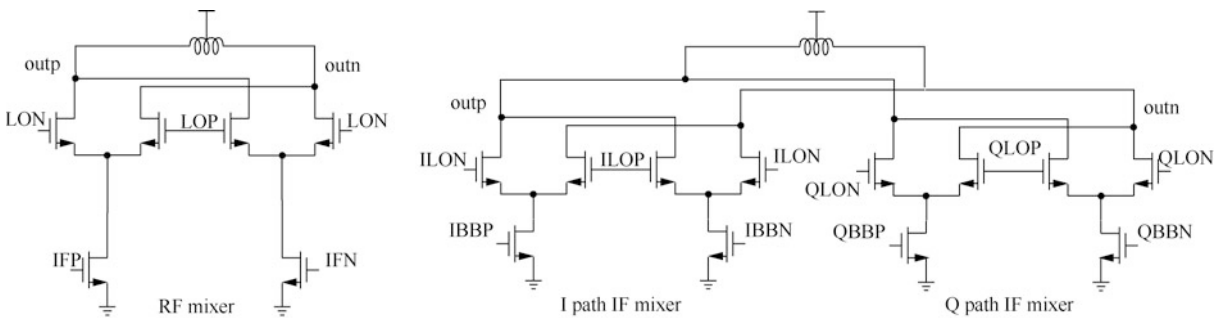

Figure 14 Schematics of up-conversion RF and IF mixers

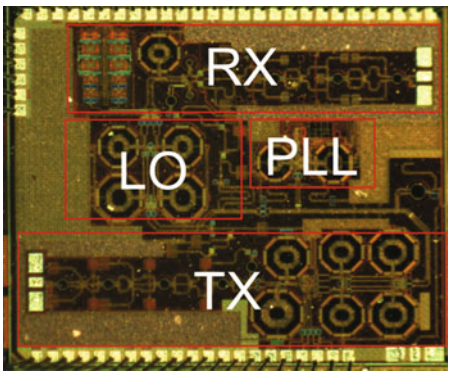

Figure 15 Die microphotograph of proposed transceiver

All measurements are performed in a COB(Chip-on-Board) package by directly probing mm-wave signals from GSG(Ground-Signal-Ground) pads with parasitic de-embedding[28], and bonding dc pads to PCB (Printed Circuit Boards). The measured S-parameters and NF versus frequency are shown in Fig.17. It can be seen that all measured results fit the simulations faithfully. The maximal gain of LNA is 23 dB @ 60.2 GHz, and the 3-dB bandwidth of S21 ranges from 58 GHz to 67 GHz.

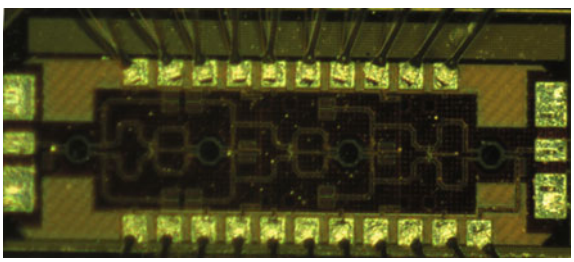

Figure16 Die microphotograph of LNA

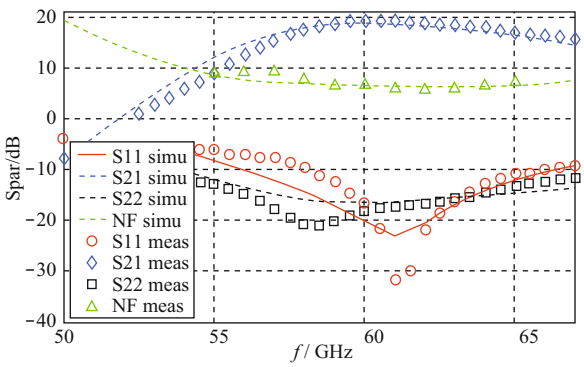

Figure 17 Measured S-parameter and NF of the LNA

The −10-dB bandwidth of S11 and S22 ranges from 58 GHz to 66 GHz. A measured minimal NF of 6 dB is achieved at 62 GHz, which is also well predicted by the simulation. The IIP3 measurement is shown in Fig.18. A measured IIP3 of −6.2 dBm is obtained versus its simulated counterpart of −6.9 dBm. The LNA consumes 23.5 mA from a supply voltage of 1.4 V.

4.2 PA

Fig.19 shows die microphotographs of the PA. The measured S-parameters versus frequency are shown in Fig.20. It can be seen that all measured results also fit the simulations faithfully. The maximal gain of the PA is 23 dB @ 60.2 GHz, and the 3-dB bandwidth of S21 is from 51 GHz to 65 GHz. Measured output P_{1dB}, P_{SAT}, and PAE are shown in Fig.21. The measured P_{1dB} and P_{SAT} of 10.4 dBm and 14 dBm, respectively, are obtained versus their simulated counterparts of 10.5 dBm and 14 dBm, with a PAE of 14%.

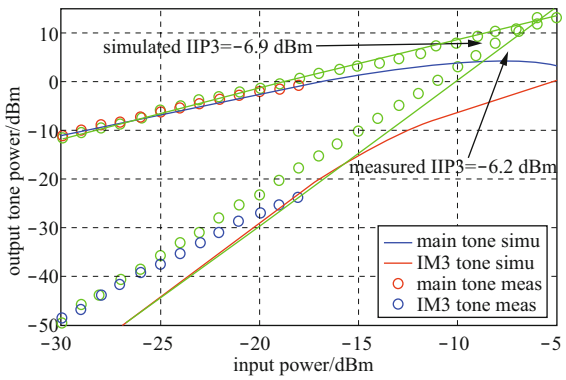

Figure 18 Measured IIP3 of the LNA

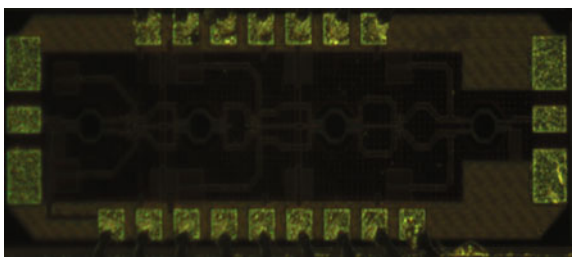

Figure 19 Die microphotograph of the PA

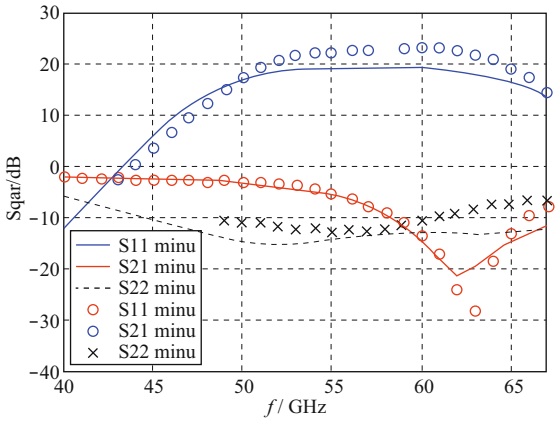

Figure 20 Measured S-parameter of the PA

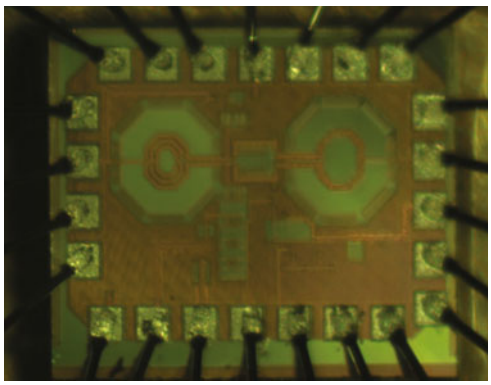

Figure 22 Die microphotograph of the PLL

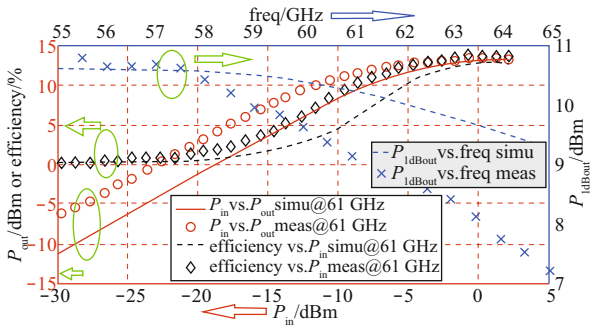

Figure 21 Measured output P_{1dB} and PAE of the PA

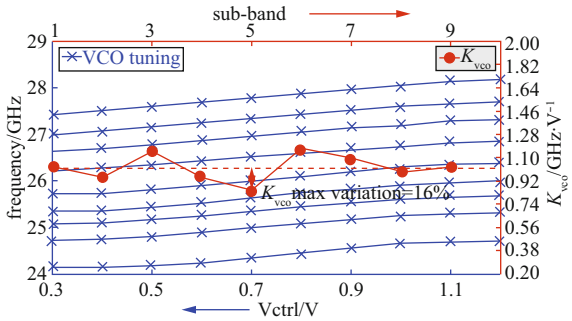

Figure 23 Measured VCO tuning range and K_{VCO} over different bands

4.3 PLL

The PLL occupies 0.8×0.62 mm^2 of the chip area, as shown in Fig.22. The VCO tuning curves in the concerned bands are shown in Fig.23, together with K_{VCO} versus different bands. Benefiting from the switched varactor array compensation, K_{VCO} maintains approximately 1 GHz/V over bands with only less than 15% of variation, while the tuning range is above 16%. The measured phase noise at a 1-MHz offset is below −101 dBc/Hz, as shown in Fig.24.

The PLL is kept with properly locking in the four channels of the IEEE802.11ad standard when turning off the VCO buffer, which substantially reduces the power of the PLL from 56 mW to 26 mW. The measured spur of the PLL is around −52 dBc, while the phase noise is −84 dBc/Hz @ 100 kHz (in-band) and −92 dBc/Hz @ 1 MHz (out-of-band), as shown in Fig.25. The integrated phase noise from 100 kHz to 100 MHz over the four channels ranges from 3.3º rms to 3.5º rms. A widely used FoM (Figure of Merit) of $f^2/(\Phi_{rms}\times Power)$ is adopted to evaluate the overall performance. Table 1 lists comparisons with state-of-the-art PLL synthesizers. This work shows a superior FoM over prior work with remarkably low power and low K_{VCO} variation, while with comparable phase noise and spur.

4.4 Transceiver

The transceiver is measured by an Agilent PNA-X network analyzer. The maximal conversion gains of the receiver over the three bands are measured as 62 dB, 63 dB, and 64 dB, which are <3 dB lower

R/S	phase noise				
	set tings		residual noise		spot noise[T1]
signal freq:	25.493 638 GHz		evaluation from 100 kHz to 100 MHz	100 kHz	−77.97 dBc/Hz
signal level:	−37.13 dBm	residual PM	4.191?	1 MHz	−101.28 dBc/Hz
signal freqΔ:	−112.85 kHz	residual PM	3.675 MHz	10 MHz	−107.37 dBc/Hz
signal levelΔ:	0.03 dBm	rMSlitter	0.456 6 ps	100 MHz	−106.37 dBc/Hz

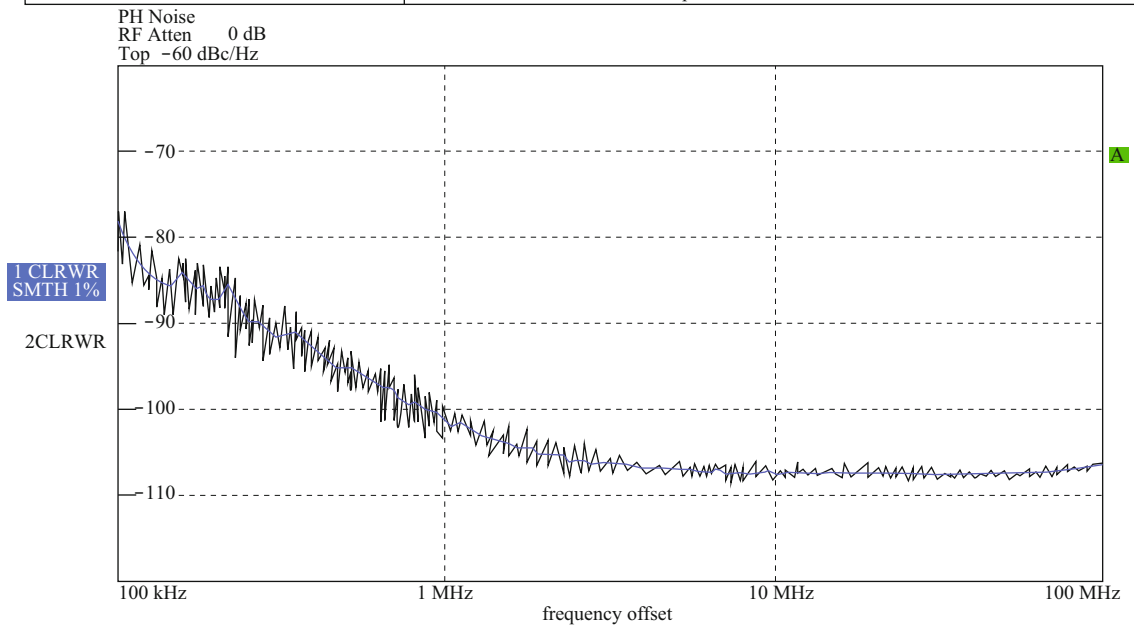

Figure 24 Measured VCO phase noise (open loop) and frequency offset

R/S	phase noise				
	set tings		residual noise		spot noise[T1]
signal freq:	25.056 003 GHz		evaluation from 1 kHz to 100 MHz	100 kHz	−84.05 dBc/Hz
signal level:	−33.72 dBm	Residual PM	5.282?	1 MHz	−92.18 dBc/Hz
signal freqΔ:	−31 Hz	Residual PM	2.688 MHz	10 MHz	−110.08 dBc/Hz
signal levelΔ:	0.13 dBm	RMSlitter	0.585 6 ps	100 MHz	−109.60 dBc/Hz

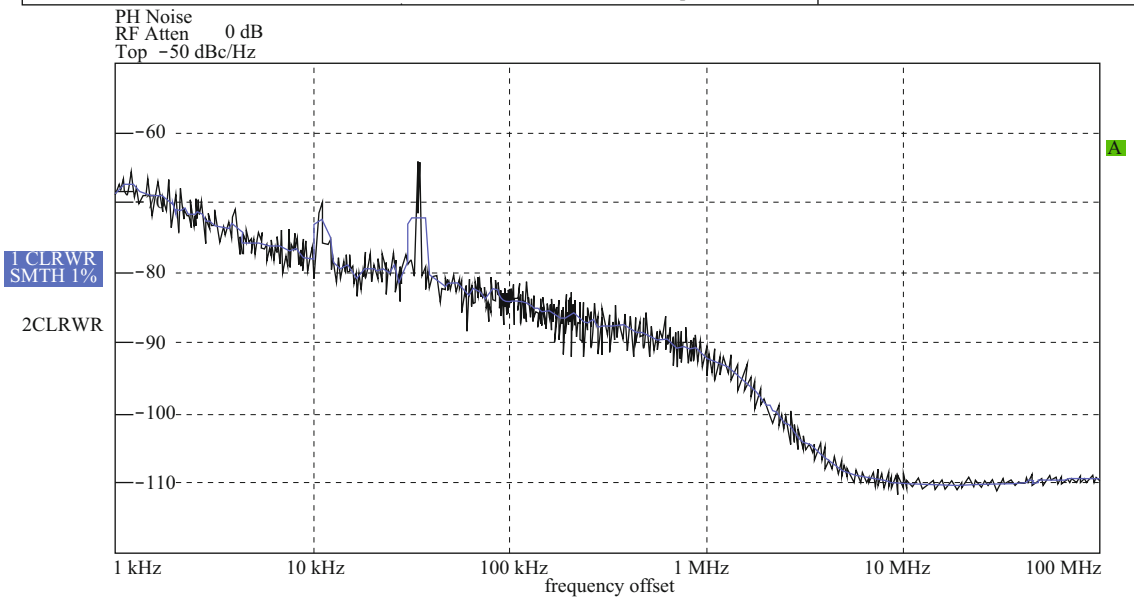

Figure 25 Measured PLL phase noise (close-loop) and frequency offset

Table 1 Comparison with prior work

references	this work	[29]	[30]	[31]
CMOS tech. nodes	90 nm	45 nm	65 nm	90 nm
supply voltage /V	1.4,1.2	0.9,1.1,1.8	1.2,1.8	1.2
freq. range /GHz	24.1~28.2	21.69~27.85	17.50~20.94	39.1~41.6
integr. phase noise	3.3°	2.57°	9.15°	18.2°
power /mW	26	40	80	64
spur /dBc	−52	−50	−50	−54
FoM (GHz^2/°rms×mW)	7.32	5.96	1.75	1.4

than the simulation, as shown in Fig.26. When multiplexing the control bits of the PGA, a tuning range of 28 dB is achieved during the measurement. A minimal noise figure of 7.1 dB is observed during the measurement. This is a deviation of less than 0.5 dB over the simulation. The difference is probably a result of the phase noise of the LO. In order to drive the 50-Ω impedance of the network analyzer for testing, a differential common-source buffer is employed. The measured 1-dB output compression power is −5.5 dBm at a 0.5 GHz baseband frequency, as shown in Fig.27, while the simulation gives −6 dBm at 1 GHz. All of the measurement results show excellent consistency with the simulations owing to the optimized T-line matching and proposed circuit design methodology. The entire receiver consumes 177 mW of power, excluding an output buffer for test purposes.

The maximal conversion gains of the transmitter are measured as 23 dB, which is <3 dB lower than the simulation. The saturated output power is 10 dBm, which is roughly 3 dB lower than simulation, as shown in Fig.28, consuming 252 mW of power.

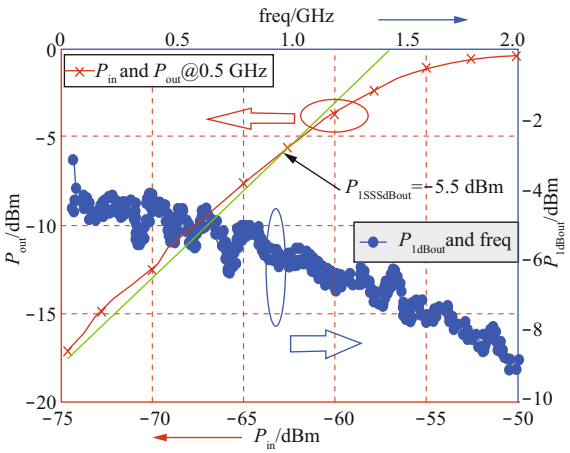

Figure 27 Measured output P_{1dB} of the receiver

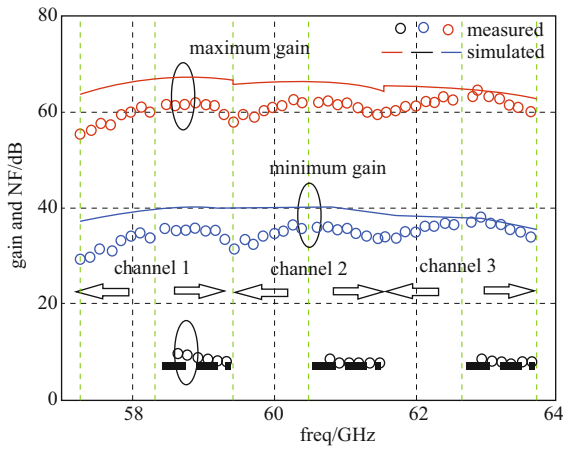

Figure 26 Measured gain and noise figure and frequency of the receiver

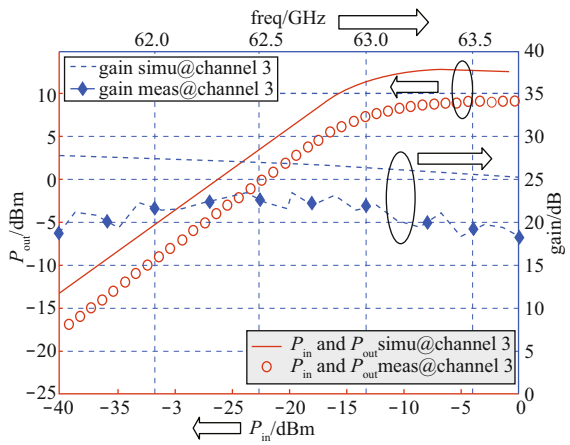

Figure 28 Measured conversion gain and output P_{1dB} of the transmitter

Table 2 Comparison with state-of-the-art

references	this work	[1]	[2]	[3]	[4]	[5]
gain/dB	36~64	30	60	30	0~60	56~70
BW/GHz	57~64	57~66	59~64	57~66	57~66	57~63
NF/dB	7.1	6.8	<10	5.5	7.1	6
OP_{1dB}/dBm	−5.5	–	–	−2	−6	–
supply/V	1.2, 1.4	1.2	1, 2.5	1.1	1.8, 2.5	1.25, 2.7
power/mW	177	155	178	112	274	540
tech/nm	90	65	65	40	90	SiGe

The discrepancies between the measured and simulated conversion gain and output power may be attributed to the reduction in the output swing of the 48-GHz LO driving the RF mixers, resulting in the degradation of conversion gains of both the receiver and transmitter. This can be fixed by inserting a buffer in the LO chain to achieve more abrupt switching in the RF mixers for performance improvements in the future.

Comparisons between this and prior work are listed in Table 2. Excellent performances with regard to conversion gain, bandwidth, noise figure, and nonlinearity are achieved over state-of-the-art technology and a commercial SiGe chip, with a reasonably low power.

4.5 System demo for Gbit/s data streaming

A demo system based on the proposed 60-GHz CMOS transceiver chip was established for Gbit/s data streaming and wireless communication, as shown in Fig.29.

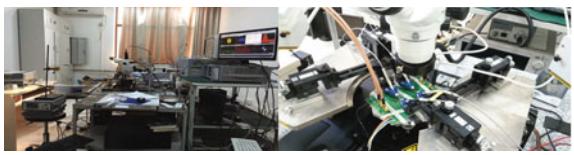

Figure 29 System demo for Gbit/s data streaming based on proposed transceiver chip

Measurements were performed in a COB package by directly probing mm-wave signals from GSG pads and bonding dc pads to a PCB, which was attached to the probe station. Baseband I/Q signals were sent to the transceiver through SMA cables from an arbitrary waveform generator, and the RF output was sent to a horn antenna with 22-dBi gain by a 1.85-mm coaxial cable. On the receiving end, the RF signal was first received from a horn antenna, and subsequently fed

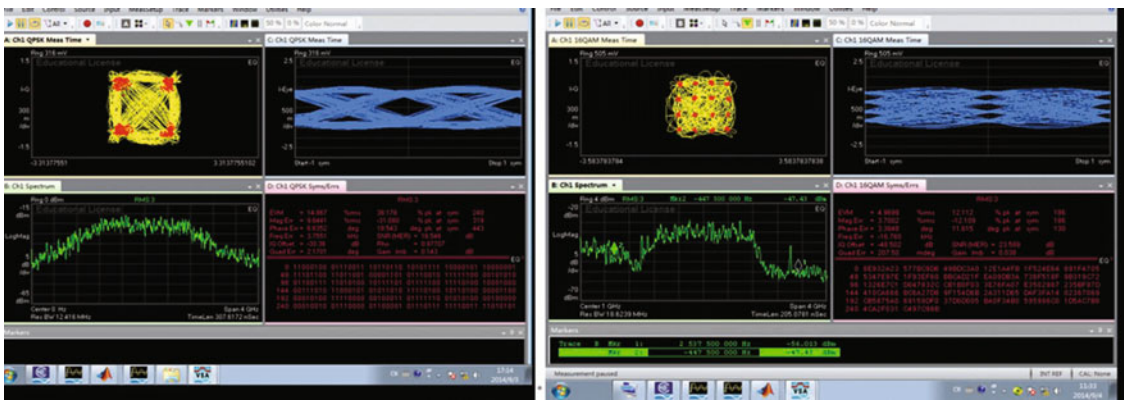

Figure 30 Measured signal constellation and eye diagram of system demo with (left) 2-GSps symbol rate and QPSK modulation scheme, and (right) 1.5-GSps symbol rate and 16-QAM modulation scheme

into the transceiver by a 1.85-mm coaxial cable for attenuation. It was then down-converted to baseband I/Q outputs, which were finally sent through SMA cables to an oscilloscope for analysis and evaluations.

A measured signal constellation and eye diagram of the system demo are shown in Fig.30. Channel 3 was utilized for data streaming verification. It can been seen that a maximal symbol rate of 2 GSps with a QPSK(Quadrature-Phase-Shift-Keying) modulation scheme is achieved with clear eye opening and an EVM(Error Vector Magnitude) of <−17 dB at a distance of 6 m considering the attenuation. The maximal symbol rate with a 16QAM modulation scheme is measured as 1.5 GSps with an EVM of less than −20 dB at a distance of 1.5 m, implying a maximal data rate of 6 Gbit/s per 2.16-GHz channel.

5 Conclusion

A fully integrated 60-GHz transceiver for 802.11ad applications in a 90-nm CMOS process is proposed and realized, based on a novel circuit and EM co-design methodology for millimeter-wave IC design. The reported transceiver monolithically integrates a receiver, transmitter, PLL synthesizer, and LO path. It is based on a sliding-IF architecture that supports up to a 16QAM modulation scheme and a data rate of 6 Gbit/s per channel, with an EVM of lower than −20 dB. All measured results are rigorously loyal to the simulation.

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References

[1] OKADA K, MINAMI R, TSUKUI Y, et al.A 64-QAM 60 GHz CMOS transceiverwith 4-channel bonding[J]. IEEE ISSCC dig. tech. papers,20142,2: 346-347.

[2] EMAMI S, WISERRF, ALI E, et al.A 60GHz CMOS phased-array transceiver pair formulti-Gb/s wireless communications[J].IEEE ISSCC dig. tech. papers, 2011, 2: 164-165.

[3] VIDOJKOVIC V, MANGRAVITI G, KHALAF K, et al.A low-power 57-to-66 GHz transceiver in 40 nm LPCMOS with-17 dB EVM at 7 Gbit/s[J]. IEEE ISSCC dig. tech. papers, 2012, 2: 268-269.

[4] TSUKIZAWA T, SHIRAKATA N, MORITA T, et al.A fully integrated 60 GHz CMOS transceiver chipset based on WiGig/IEEE802.11ad with built-in self-calibration for mobile applications[J]. IEEE ISSCC dig. tech. papers, 2013, 2: 230-231.

[5] A 60 GHz commercial receiver module for IEEE 802.11ad high speed wireless communications[Z].

[6] KONG L, SEO D, ALON E, et al.A 50 mW-TX 65 mW-RX 60 GHz 4-element phased-array transceiver with integrated antennas in 65 nm CMOS[J]. IEEE ISSCC dig. tech. papers, 2013, 2: 234-235.

[7] MITOMO T, TSUTSUMI Y, HOSHINO H, et al.A 2 Gbit/s-throughput CMOS transceiver chipset with in-package antenna for 60 GHz short-range wireless communication[J]. IEEE ISSCC dig. tech. papers, 2013, 2: 266-268.

[8] ZHAO D, KULKARNI S, REYNAERT P.A 60 GHz out phasing transmitter in 40 nm CMOS with 15.6 dBm output power[J]. IEEE ISSCC dig. tech. papers, 2013, 2: 170-172.

[9] PERAHIA E, GONG M X. Gigabit wireless LANs: an overview of IEEE 802.11ac and 802.11ad[J]. ACM SIGMOBILE mobile computing and communications review, 2011, 15(3): 23-331.

[10] ZAAIMIA M Z, TOUHAMI R, HAMZA A,et al. Design and performance evaluation of 802.11 ad phys in 60 GHz multipath fading channel[C]// Proc. IEEE Int. Workshop Systems, Signal Proc. their Applications (WoSSPA), 2013.

[11] KIM T, PARK J, SEOL J Y, et al. Tens of Gbps support with mmWavebeamforming systems for next generation communications[C]// Proc. IEEE GLOBECOM, 2013: 3790-3795.

[12] BLEICHER A.The 5G phone future: Samsung's millimeter-wave transceiver technology could enable ultrafast mobile broadband by 2020[J]. IEEE spectrum, 2013, 50(7): 11-12.

[13] RAPPAPORT T, SUN S, MAYZUS R,et al.Millimeter wave mobile communications for 5G cellular: it will work![J]. IEEE access, 2013, 1(5): 335-349.

[14] KHAN F, PI Z. mmWave mobile broadband (MMB): unleashing the 3~300 GHz spectrum[C]// Proc. IEEE Sarnoff Symp., 2011.

[15] ASSN S I.International technology roadmap for semiconductor[J]. Computer, 1999, 35(1): 42-53.

[16] WANG H, ZHANG L, YANG D, et al. Modeling of current-return-path effect on single-ended inductor in millimeter-wave regime[J]. IEEE electron device lett.,2011, 32(6):737-739.

[17] RAZAVI B. Design of millimeter-wave CMOS radios: a tutorial[[J]. IEEE trans. circuits syst. i: reg. papers,2009, 56(1): 4-16.

[18] LUO J, ZHANG L, WANG Y.A unified model and direct

extraction methodologies of various CPWs for CMOS mm-Wave applications[C]// Proc. IEEE Custom Integr. Circuits Conf., 2012: 1-4.
[19] TANG Y, YE Z, WANG Y. Broadband compact model for on-chip mm-wave transformers and baluns with emphasis on capacitive coupling effects[C]// Proc. IEEE Custom Integr. Circuits Conf.,2011: 1-4.
[20] YAO J, YE Z, WANG Y.An automatic parameter extraction and scalable modeling method for transformers in RF circuit[C]//Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC), 2013: 1-4.
[21] ZHANG L, ZHOU C, WANG H, et al. A Fully integrated 60 GHz four channel CMOS receiver with 7 GHz ultra-wide bandwidth for IEEE 802.11ad standard[J].China commun., 2014, 11(6): 1-6.
[22] ZHOU C, ZHANG L, ZHANG L, et al. Injection-locking based power and speed optimization of CML dividers[J].IEEE trans. circuits syst. II: exp. briefs,2011, 58(9): 565-569.
[23] DICKSON T O, YAU K H K, CHALVATZIS T, et al.The invariance of characteristic current densities in nanoscale MOSFETs and its impact on algorithmic design methodologies and design porting of Si(Ge) (Bi)CMOS high-speed building blocks[J]. IEEE J. solid-state circuits, 2006, 41(8): 1830-1845.
[24] LIN T Y. A low-noise VCO with a constant KVCO for GSM/GPRS/EDGE applications[C]//Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC), 2009: 387-390.
[25] HARA S, OKADA K, MATSUZAWA A.A 9.3 MHz to 5.7 GHz tunable LC-based VCO using a divide-by-N injection-locked frequency divider[C]//Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC),2009: 81-84.
[26] KIM D, KIM J, CHO C.A 94 GHz locking hysteresis-assisted and tunable CML static divider in 65nm SOI CMOS[C]//IEEE ISSCC Dig. Tech. Papers, 2008: 461-462, 628.
[27] HAJIMIRI A, LEE T H. A general theory of phase noise in electrical oscillators[J].IEEE J. solid-state circuits, 1998, 33(2): 179-194.
[28] LUO J, ZHANG L, WANG Y.A distributed de-embedding solution for CMOS mm-wave on-wafer measurements based-on double open-short technique[J]. IEEE microw. wirelesscompon. lett.,2013, 23(12): 686-688.
[29] OSORIO J F, VAUCHER C S, HUFF B, et al. A 21.7-to-27.8GHz 2.6-degrees-rms 40Mw frequency synthesizer in 45nm CMOS for mm-Wave communication applications[C]//IEEE ISSCC Dig. Tech. Papers, 2011: 278-280.
[30] RICHARD O, SILIGARIS A, BADETS F, et al. A 17.5-to-20.94 GHz and 35-to-41.88 GHz PLL in 65 nm CMOS for wireless HD applications[C]//IEEE ISSCC Dig. Tech. Papers, 2010: 252-253.
[31] PELLERANO S, MUKHOPADHYAY R, RAVI A, et al.A 39.1-to-41.6 GHz ΣΔ fractional-n frequency synthesizer in 90 nm CMOS[C]// IEEE ISSCC Dig.Tech. Papers, 2008: 484-630.

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