The path to 5G: mmWave aspects

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Abstract: The wide spectrum and propagation characteristics over the air give mmWave communication unique advantages as well as design challenges for 5G applications. To increase the system speed, capacity, and coverage, there is a need for innovation in the RF system architecture, circuit, antenna, and package in terms of implementation opportunities and constraints. The discuss mmWave spectrum characteristics, circuits, RF system architecture, and their implementation issues are discussed. Moreover, the transmitter key components, i.e., the receiver, antenna, and packaging are reviewed.

Key words: mmWave, 60 GHz, MIMO, beamforming, transmitter, receiver, antenna, packaging

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1 Introduction

Driven by the ever-increasing consumer experience requirements, wireless communication undergoes a 10-year cycle for every generation of cellular advancement. To date, 3G and 4G wireless communication networks are widely deployed. However, rapidly expanding multimedia communication (such as large file transfer, home entertainment, gaming technology, and smart hardware) increase the burden on 3G/4G systems, particularly in terms of communication capacity and speed.

Considering the above facts, there has been much interest in 5G research from both academia and industry. It is expected that 5G wireless communication will be realized by 2020 or beyond. Compared to 4G systems, it is anticipated that 5G

will achieve mobile traffic growth of 1 000X, 100 billion connected devices, etc. To achieve the above targets, several key technologies (e.g., massive MIMO(Multiple-InputMultiple-Output), ultra-dense networks, and all-spectrum access) will be used. To be more specific, 5G should meet the following specifications: 0.1~1 Gbit/s user experience data rate, tens Gbit/s peak data rate, ms-level end-to-end latency, and improvements of 100 times in terms of energy-efficiency and cost reduction per bit, etc.

Because of the wide bandwidth characteristics, mmWave systems have advantages of high data rates and communication capacity, which benefit fixed access and cellular applications^[1-4]. To date, several mmWave communication prototype systems have been demonstrated. Together with NTT DOCOMO, Nokia reported an experimental E-band

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communication system for 5G cellular applications. Together with an antenna with a 28 dB gain and 3° half-power beamwidth, the system is operating at 73.5 GHz with a 1 GHz bandwidth^[5]. Samsung reported a 28 GHz phased-array system whose field measurements demonstrate an error vector magnitude (EVM) of -24 dB for a 16QAM OFDM signal with a 500 MHz bandwidth^[6]. However, the high operating frequency and high path loss introduces strong challenges to the 5G mmWave system design. In particular, implementation issues become very important. To meet 5G key performance indexes, innovations in mmWave system architecture, circuit, antenna, and package levels are required.

In this paper, we discuss the mmWave spectrum characteristics, circuit, and system implementation issues, highlighting the advanced RF system architecture and implementation issues. Moreover, we review some RF blocks and systems for 60 GHz communication from Southeast University, including the transmitter key components, receiver, antenna, and packages.

2 mmWave communication system architecture and implementation issues

As opposed to sub-6 GHz, mmWave communication has unique characteristics. Accordingly, the main challenge for mmWave systems is the air interface design, particularly the RF front-end and antenna array. To achieve high data rate, high capacity, and

large coverage, it is very important to first understand the characteristics of the mmWave spectrum, and then the implementation issues. In addition, we will discuss the mmWave system architecture.

2.1 mmWave spectrum

As shown in Fig.1, a list of 5G candidate high-frequency bands ranging from 24 GHz to 86 GHz was selected at the WRC-15 conference (including 24.25~27.5, 31.8~33.4, 37~43.5, 45.5~50.2, 50.4~52.6, 66~76, and 81~86 GHz bands). To speed up 5G research in the US, the FCC recently announced several licensed and unlicensed mmWave spectra, i.e., 28 GHz (27.5~28.35 GHz), 38 GHz (37~40 GHz), and 64~71 GHz^[7]. It should be noted that with the existing 57~64 GHz unlicensed band, the US creates a 14 GHz contiguous spectrum at the 60 GHz band, i.e., the 57~71 GHz band. In this way, a myriad of new applications for consumer, business, industrial, and government use can be guaranteed. Compared with the traditional sub-6 GHz spectrum, the mmWave spectrum has several characteristics.

1) The mmWave spectrum is abundant, and it can easily achieve high data rates of the order of several Gbps even with low-order modulation.

2) As the free-space path loss is proportional to the square of the link distance and carrier frequency, the mmWave spectrum has a very large propagation loss. In addition, the mmWave wavelength is very short, making it very susceptible to obstructions. To increase the coverage, considering the typical LOS (Line-of-Sight) and NLOS (Non-LOS) communication

Figure 1 Available spectrum for wireless communication

scenarios, the characterization of mmWave indoor and outdoor channels has been emerging as an important research topic^[2]. From a system link budget perspective, the coverage can be extended by improving the system air interface performance, such as the transmitted power, receiver sensitivity, and antenna gain. However, these parameters depend largely on the implementation technology, which is to be discussed in Section 2.2.

3) Although the mmWave spectrum is very wide, its channel numbers are limited due to its wide bandwidth nature (500 MHz~2 GHz). In other words, the in-channel interference will become important, and interference control and mitigation techniques are needed.

2.2 Implementation issues

Considering the future mass consumer market requirements, it is very critical to realize the mmWave system in a cost-effective and energy-efficient way, particularly in terms of the RF front-end chip, antenna, and packaging implementation aspects.

In the past, the mmWave RF front-end chip is realized in Section 3~Section 5 compound process, with the penalty of high cost, high power, and low integration level. Guided by the ITRS (International Technology Roadmap for Semiconductors), the transistor feature size is reduced by Moore law scaling, and the CMOS transistor speed and integration level are significantly improved^[8]. Accordingly, the CMOS process is used to realize the mmWave RF front-end chip. Attracted by a potentially low cost, high integration level, and enhanced functionality, many academic and industrial groups are involved in CMOS mmWave circuit and system research and development for mmWave communication as well as for critical radar applications^[9-14].

Despite the advantage of increased CMOS transistor

speed due to size scaling, both the supply voltage and the ratio of the supply voltage to the transistor threshold voltage are also reduced. From the perspective of the mmWave circuit, this typically translates into a low signal swing and low signal dynamic range. On the other hand, the insertion loss of passive devices increases at mmWave frequencies, which further decreases the power gain of the active devices. Accordingly, it will result in a low output power and high phase noise for the power amplifier and oscillator, respectively^[9]. These issues can be solved from a 5G system large-array architecture perspective, which is to be discussed shortly in Section 2.3.

As the interface between the RF chip and the air, the antenna and packaging plays an important role in terms of radiation pattern, efficiency, insertion loss, etc. Nowadays, because of the short wavelength at mmWave frequencies, antenna designs are shifting from conventional discrete designs to AoC (Antenna-on-Chip) and AiP (Antenna-in-Package) solutions. Compared with the AoC solution, AiP solutions offer a high gain, broad bandwidth, and cost-effective approach by incorporating multilayer substrate materials and chip-integration techniques. Moreover, the insertion loss between the antenna and chip can be minimized by providing a shorter interconnect. Two kinds of interconnect techniques are available in the mainstream packaging industry: wire-bond and flip-chip techniques. The wire-bond technique, which is well established in consumer electronics, remains a very attractive solution because it is robust and inexpensive. However, if not carefully designed, the discontinuity introduced by the bond wire can significantly affect the performance of the interconnect. The flip-chip interconnect has a better performance than that of the wire bonding because of its less parasitic inductance; however, it is more expensive and complex.

2.3 System architecture

Considering the unique characteristics of the mmWave frequency, an advanced RF transceiver architecture is needed to improve the system speed, energy efficiency, and spectral efficiency. With the high integration level in the chip and very compact antenna array, it is suitable to realize a mmWave system using MIMO and beamforming techniques^[15-18].

As shown in Fig.2 and Fig.3, for mmWave communication, there are two typical transceiver architectures, namely direct conversion and dual-conversion^[9,19,20]; both of these have their advantages and disadvantages. Direct conversion, which is popular in GHz RF radio, can achieve compact and low power implementation, as well as operation flexibilities. However, for mmWave applications, its high-frequency quadrature modulation/demodulation typically gives rise to severe distortion, such as I/Q imbalance and LO (Low Oscillator) feedthrough. Moreover, the indispensable quadrature PLL (Phase-Locked Loop) has introduced several implementation issues. These are the trade-off between the phase noise, tuning range, and phase error, as well as the frequency pulling/pushing caused by the power amplifier^[20].

Figure 2 Direct-conversion architecture

Figure 3 Dual-conversion architecture

To overcome the above-mentioned design issues and improve the SNR, an alternative solution is to use the dual-conversion architecture (also referred to as sliding-IF), as shown in Fig.3. In this architecture, the quadrature modulation and demodulation working frequency is significantly reduced. Moreover, the tuning range and operating frequency of the LO are reduced, simplifying the system design. Therefore, the sliding-IF architecture is very popular in mmWave systems^[19, 21-23].

Combined with the beamforming technique, based on the above transceiver architecture, we can realize the phased-array system, thus achieving beam-scanning capability, which is good for LOS and NLOS communication scenarios. With the above features, mmWave wireless access and wireless backhaul can be simultaneously supported, increasing the system flexibility^[2-4]. Moreover, with a large-scale antenna array, we can realize a large antenna array gain, compensating the large path loss associated with high frequency and increasing the coverage. Accordingly, we can establish a stable wireless link.

To be more specific, from an implementation perspective, mmWave can achieve a high directivity using a large array antenna, and the actual power that is required to deliver a certain EIRP (Equivalent Isotropic Radiated Power) is significantly reduced. Accordingly, the requirements on each RF front-end component, such as the antenna gain and PA output power, can be relaxed, thereby increasing the system energy efficiency. On the other hand, we can achieve a small beam, increasing the signal spatial isolation and simultaneously accommodating many co-channel users. In other words, a kind of spatial filtering on the co-channel signal is achieved, and the spectrum efficiency can be improved. Combined with the mmWave large path loss feature, the interference can be relaxed and the frequency can be reused by using small-cell techniques, as well as increasing the spectrum efficiency and communication capacity.

These characteristics make mmWave communication very attractive for ultra-dense networks with a range of 10~200 m. It should be noted that because of the small beam, large-array systems are very sensitive to channel amplitude and phase mismatch in terms of aging, environment variation, and fabrication tolerance. To maintain a stable wireless link, macro assistant small cells, beam tracking, and channel calibration techniques are essential.

Based on the phase shifting and amplitude control mechanism, beamforming can be realized with RF-path, LO-path, baseband, and digital beamforming^[19, 21-23]. The advantage of LO-path and baseband beamforming is that the phase shifter is not in the signal path or in the low-frequency signal path. In this way, the challenges of the mmWave circuit design can be reduced. However, more mixers are needed, and the LO routing becomes complex, potentially increasing

the coupling between each RF channel, insertion loss, and phase noise. This will typically worsen the large-array system performance and increase the power consumption. In contrast, with the RF-path beamforming, more RF components can be shared, resulting in a very compact structure. In addition, the linearity performance is improved because of the spatial filtering. However, as the phase shifter is in the signal path and working at high frequency, special attention should be paid to improving its bandwidth and insertion loss.

In 4G LTE (Long-Term Evolution) MIMO systems, each antenna has its own transmitter and receiver chain. Doing so in mmWave systems will cause the power consumption to be too large as the number of antennas exceeds 100. To deal with these issues, the hybrid beamforming architecture can be used, as shown in Fig.4. In this architecture, based on

Figure 4 Hybrid RF/baseband MIMO architecture

the design trade-off mentioned above, RF-path beamforming is selected. It should be noted that with respect to the MIMO and beamforming operation, TDD (Time-Division Duplexing) is a good alternative to FDD (Frequency-Division Duplexing) because of the ability to leverage uplink/downlink reciprocity.

Among the system components, the transmitter/receiver chain (RF, IF, analog front-end), PLL, ADC (Analog-to-Digital Converter), and DAC (Digital-to-Analog Converter), and baseband parts are typically the most important power-consuming parts, and their performance is the system bottleneck. Moreover, the supporting circuit power overhead, which is independent of the radiated output power and array size, is also very important. To achieve a power-efficient system, an optimized, in terms of the number of antennas, transmitter/receiver chain, number of and resolution ADCs/DACs, baseband circuit, and system complexity. As an important part of the system, the waveform of mmWave 5G systems is also critical, and will affect the system performance in terms of parameters such as the SNR (Signal-to-Noise Ratio), power amplifier PAPR (Peak-to-Average Power Ratio), ADC/DAC resolution, and in-band flatness.

Considering 5G's cost-effective and high-performance requirements as well as high-frequency design challenges, the co-design of chip-package-systems becomes very important. To reflect this trend, ITRS has not been updated since 2015, and the IEEE and SEMI organizations propose to start a new roadmap called the IEEE IRDS (International Roadmap for Devices and Systems). In May 2016, its first meeting was held in Leuven, Belgium. Instead of focusing only on device scaling, IRDS covers other devices, modules, systems, architectures, and software mission is to set a new future direction of the semiconductor, communications, IoE, and computer industries for the next few decades.

3 Transmitter

As the up-conversion mixer and PA (Power Amplifier) working frequency is high, they typically limit parameters such as the transmitter power efficiency and bandwidth. In the following sections, we focus on 60 GHz applications, and we discuss design considerations and show test results for these key components.

3.1 Up-conversion mixer

The performance of the 60 GHz up-conversion mixer is crucial for the transmitter. In particular, to achieve good EVM performance for the 60 GHz wideband and transmitter large signal operation, the mixer should achieve good in-band gain flatness and high linearity performance. In addition, to drive the power amplifier, the mixer should provide a high gain and a high output power.

Fig.5 shows the implemented up-converter mixer^[24]. It consists of a Gilbert cell, an LO, and an RF buffer. Here, the LO frequency is set to 48 GHz in order to realize the sliding-IF architecture^[23]. We used the RF buffer to boost the mixer output power. In this design, we used the transformer-based impedance-matching network to realize the inter-stage matching between the Gilbert cell, the RF buffer, and the LO buffer. Compared with traditional T-type or LC-type networks, the transformer-based matching network can typically achieve a more compact layout and lower insertion loss, and it can provide the biasing flexibility, good common-mode stability, and broadband impedance matching. In the RF and LO buffer, we adopted the capacitive neutralization technique to further increase the reverse isolation and the power gain.

We implemented the up-conversion mixer using a 65 nm CMOS process. Fig.6 shows the chip micrograph. Including all pads, the mixer occupies an area of $0.725 \times 0.595 \text{ mm}^2$. Fig.7 illustrates the measured

Figure 5 Schematic diagram of the proposed 60 GHz CMOS up-conversion mixer

conversion gain versus frequency and channels. The conversion gain is over 13 dB across the 57~66 GHz band, and the gain variation in each channel is about 1 dB. Moreover, driven by an -11.5 dBm LO power, the mixer output power 1 dB compression point is as high as 2.5 dBm.

Figure 6 Chip micrograph of the 60 GHz up-conversion mixer

Figure 7 Measured conversion gain and frequency and channels

Tab.1 summarizes the performance of state-of-the-art 60 GHz CMOS up-conversion mixers. Compared to the previous work, only the proposed mixer can cover the IEEE 802.15.3c standard four-channels. Further, in-band the gain variation is less than 1.5 dB. To the author's best knowledge, both the gain and output power of this broadband 60 GHz mixer are the highest achieved.

3.2 PA

The PA plays an important role as the key component of the 60 GHz transmitter, especially in terms of the output power, power gain, power efficiency, and linearity. Basically, the PA output power should be high enough to realize large coverage. Considering the large PAPR of the high-order modulation signal, the PA linearity and efficiency should be improved. On the other hand, in order to reduce the driving requirement of the up-conversion mixer buffer, the PA needs to provide sufficient power gain.

The schematic of the proposed PA is shown in Fig.8, which consists of three pseudo-differential stages. As in the case of the up-conversion mixer, the capacitive neutralization is also used for the reverse isolation and $G_{\max}$, improving the stability and the PAE. In order to offer sufficient output power, we implemented a transformer-based 4-way power combiner. To reduce the loss, we fabricated the transformer using thick metal layers. To reduce the insertion loss, we propose a new inter-stage matching network

network, as shown in Fig.9. Fig.9 (a) shows the inter-stage matching network between the second stage and the third stage, and Fig.9 (b) shows its equivalent circuit, which consists of a transformer, transmission lines, and a shunt inductor. Simulations indicate that

Figure 9 Inter-stage matching network and its equivalent circuit

Table 1 State-of-the-art 60 GHz CMOS up-conversion mixers

references	this work	[25]	[26]	[27]	[28]
technology	65 nm	130 nm	65 nm	90 nm	130 nm
RF freq/GHz	57~66	58~66	58.3~62.5	57.1~63.3	59~65
IF freq/GHz	10~14	4	0~3	0.1	0.1
CG/dB	14	5	-4.1	4.5	4
RF BW/GHz	>9	8	6	6.2	6
PDC/mW	32	92.2	23	15.1	24
OP1dB/dBm	2.5	-5	-13.5	-11.8	-5.6

Figure 8 Schematic of the three-stage power amplifier with 4-way power-combining

compared to the case without the shunt inductor, the insertion loss of the inter-stage matching network is improved by more than 1.5 dB.

Fig.10 shows a photo of the PA chip, which is realized using a 65 nm process. Including all DC and RF pads, the PA occupies an area of 0.83 mm×0.88 mm, while the core area is only 0.68 mm×0.88 mm. The measured and simulated S-parameters across 50~70 GHz are shown in Fig.11. Because of the proposed inter-stage matching network and the capacitive neutralization technique, the measured S_{21} is greater than 20 dB from 54 GHz to 65 GHz, and the peak power gain is about 24 dB at 61 GHz. As illustrated in Fig.12, with a 1.2 V supply, at 61 GHz, the PA achieves a P_{sat} as high as 19 dBm, a P_{1dB} of 15.1 dBm, and a peak PAE of 15.1%. With a 1-5 supply, P_{sat} , P_{1dB} , and PAE are 18 dBm, 14.8 dBm, and 13.2%, respectively.

Figure 10 Micrograph of the PA

Figure 11 Measured S-parameter from 50~70 GHz

Figure 12 Measured Pout and PAE and input power @ 61 GHz

Tab.2 summarizes the comparison of the state-of-the-art 60 GHz CMOS PAs. Compared with other works, the proposed PA achieves the highest power

Table 2 Summary of 60 GHz power amplifiers

references	[29] ISSCC2010	[30] ISSCC2011	[31] ISSCC2010	[32] ISSCC2010	[33] RFIC2011	[34] JSSC2010	[35] JSSC2010	[36] APMC2011	this work	
technology	65 nm	65 nm	90 nm	65 nm	65 nm	65 nm	65 nm SOI	65 nm	65 nm	65 nm
freq/GHz	60	60	60	60	60	60	60	60	60	60
Vsupply/V	1	1	1.2	1.2	1.2	1	1.2	1.2	1	1.2
gain/dB	19.2	20.3	20.6	14.3	18.2	16	14	21	24	24.5
P_{1dB} /dBm	15.1	15	18.2	11	—	—	7.5	—	14.8	15.4
P_{sat} /dBm	17.1	18.6	19.9	16.6	9.6	11.5	10.5	13	18	19
PAE/%	11.1	15.1	14.2	4.9	13.6	15.2	22.3	36	13.2	12.8
Area	0.83 ^[*1]	0.28 ^[*1]	1.76	0.462	0.32	0.696	0.573	0.16	0.74	0.6 ^[*1]
3 dB BW	10	9	8	15	12.5	8.5	—	—	11	11

[*1] Core area excluding DC bias pads

gain, P_{sat} , P_{1dB} , PAE, and the bandwidth performance are also very good.

4 Receiver

For mmWave communication applications, the receiver has several requirements. First, to increase the data rate, we may employ high-order SC (Single-Carrier) modulations (such as 16QAM) that are sensitive to in-band amplitude variations. Secondly, to achieve both sensitivity and linearity performance, the receiver needs to have a low NF (Noise Figure) and large gain tuning range. Third, as the I/Q mismatch degrades the IRR (Image-Rejection Ratio) and corrupts the baseband output, I/Q balance performance should be improved. To meet future 5G high data rate requirements, higher-order modulation or channel bonding scheme may be used, imposing even more critical requirements on the mmWave receiver design.

Fig.13 shows the block diagram of the receiver, which is realized using the sliding-IF architecture for better I/Q mismatch performance^[37]. The receiver consists of a 4-stage 60 GHz LNA (Low-

Noise Amplifier), a 48 GHz RF mixer, a 12 GHz I/Q demodulator, and I/Q baseband VGAs (Variable Gain Amplifiers). The 48 GHz LO signal is provided from an external source, and is divided into two paths, driving the RF mixer and the divide-by-4 static frequency divider, respectively. The LNA and VGA gain control are realized using digital programmable gain bits. Moreover, the I/Q mismatch calibration is achieved through the I and Q VGA gain control and the digitally controlled phase delay at the output of the frequency divider^[38].

Fig.14 shows the proposed LNA structure, which consists of a 4-stage common source amplifier. Here, we used the capacitive neutralization technique and transformer-based matching network. Different from previous works, we used low-k transformer-based matching networks to improve the in-band flatness. In Ref.[8], the author demonstrated a very wide 3 dB bandwidth that extends to frequencies well below the 60 GHz band. However, from the perspective of the 60 GHz standard, this bandwidth extension may result in a desensitization problem, particularly when an out-of-band blocker is present.

As opposed to a stand-alone LNA, the LNA in the

Figure 13 GHz broadband receiver

Figure 14 Schematic of LNA

receiver needs to drive the mixer, and we require a combined design involving an LNA and RF mixer. As shown in Fig.15, we also used a low-k transformer-based matching network between the LNA and the mixer. In the RF mixer, we inserted a pair of inductors between the mixer input transconductance (GM) stage and the switching quads. At the RF mixer output, we employed two compact capacitive-bridged inductive shunt peaking loads. In this way, together with the low-k transformer-based impedance-matching network, we can realize a broadband bandwidth. To suppress noise contribution from the subsequent stages, the LNA gain should be more than 20 dB. Here, we used the LNA to drive the Gilbert double-balanced mixer, which has benefits in terms of the clock feedthrough. As the Gilbert mixer typically has high input impedance, the LNA output node is the receiver linearity bottleneck. For the 60 GHz application, the signal received by the antenna

has a large dynamic range, and the LNA should have a large gain-tuning capability with well-defined gain steps. Typically, using the cascade topology and varying biasing points of the common-source transistor, the amplifier gain can be tuned, albeit with the penalty being a worse linearity and noise performance^[39-40]. In this design, as shown in Fig.14, by controlling the current ratio of the amplifiers with switches, we can achieve a well-defined gain step that is not sensitive to PVT corners. Fig.16 shows the simulated LNA performance in three-gain modes. It is clear that because of the above-mentioned low-k transformer-based impedance matching and co-design of the LNA and RF mixer, the 1 dB bandwidth covers the full RF frequency band, and the out-of-band gain

Figure 16 Simulated LNA gain performance in three gain modes

Figure 15 Schematic of the RF mixer and the I/Q demodulators

has fast roll-off characteristics. Moreover, simulations indicate that the LNA linearity and noise performance are maintained, as the LNA gain is tuned in the last three stages.

In the demodulator, we used the double-balanced Gilbert-cell mixer is typically used, which has the trade-off between high linearity and low noise. In this design, the biasing point of the gm stage and the switching quads are set separately for linearity and low noise. In addition, as the IF frequency is reduced to 12 GHz because of the inverter-based GM cell. Compared with the typical common-source topology, simulations prove that the inverter-based GM cell has a higher linearity and twice the transconductance efficiency.

We used the VGA to maximize the dynamic range of the overall system and to maintain an SNR that is sufficient for a reliable wireless link. Fig.17 shows the proposed VGA topology, which consists of an input HPF (High-Pass Filter), a four-stage VGA core, a DCOC (Dc Offset Cancellation) unit and an output buffer. We used the HPF to eliminate the input dc offset generated by the receiver front-end. By introducing the digitally-controlled resistors and capacitor-array network, the VGA gain and bandwidth can be precisely controlled, eliminating the need for

DACs. With four gain cells (VGA1~4), considering the gain and bandwidth trade-off, the VGA core can achieve a total gain-control range of 69 dB for single-channel applications. For the single-channel applications, the VGA1 and VGA2 gain-control range is 24 dB with a 21 dB maximum gain and 6 dB steps for coarse tuning. The VGA3 gain-control range is 15 dB with 3 dB steps, while the VGA4 gain-control range is from 1 to 12 dB with 1 dB steps for fine tuning.

Considering the advantage in the bandwidth, we employed a modified Cherry-Hooper amplifier for the gain cell, as shown in Fig.18. The structure consists of an input transconductance (GM) stage and a TI (Trans-Impedance) stage. Further, the two dominant poles are located at the output of the GM and TI stages, respectively. Assuming that $R_f \ll R_3 // r_{o6}$, the impedances of dominant poles Z_A and Z_B can be given by $Z_A \approx Z_B \approx 1/g_{m3}$, which are much lower than the load resistance, resulting in higher frequency poles and a wider bandwidth.

Fig.19 shows the microphotograph of the receiver fabricated using a 65 nm CMOS process. It occupies a total chip area of 1.9×0.7 mm, including all the dc and RF pads. The maximum dc power consumption is 102.4 mW.

Figure 17 Proposed VGA topology

Figure 20 The measured conversion gain in high-gain, typical-gain, and low-gain modes in four channels

We also obtained the linearity and noise measurements. In the high-gain mode, the receiver input IP1dB is about -72 dBm, whereas in the low-gain mode, the receiver input IP1dB is about -30 dBm. The measured noise figure is about 5 dB.

The antenna and package design depends greatly on

references	[20]	[40]	[41]	[42]	this work
process	65	65	65	90	65
gain/dB	9~23	0.1~19.6	36	19.2~40	20~75
gain range	14	19.5	—	20.8	55
3 dB BW/GHz	2.16 ^[*2]	0.915	7.5	4 ^[*1]	8.5
NF/dB	<4.9	N/A	<11	4	5
IP1dB/dBm	N/A	N/A	−18	−32	−30
area/mm ²	2 ^[*1]	1.1	1.1	1.5 ^[*1]	1.4
power/mW	223 ^[*3]	48	30~42	35.3	28

[*3] including PLL and buffer

the fabrication material and fabrication technology in terms of the antenna gain, radiation efficiency, bandwidth, etc. In addition to the electrical performance, the antenna and package design should consider the cost and the yield for future large-volume applications.

As the working frequency is somewhat high, the material selection is critical considering its permittivity, loss property, and the ease with which it can be manufactured. Because of the superior electrical characteristics, low water absorption, and good mechanical properties, advanced antenna materials such as LTCC (Low-Temperature Co-fired Ceramics), LCPs (Liquid Crystal Polymers), and high-end hydrocarbon ceramic PCBs (Printed Circuit Boards) are promising solutions for mmWave antennas. The LTCC exhibits low-loss dielectrics and conductors, good thermal conductivity, and a high degree of integration. However, it has limitations that are due to its higher process temperatures, large feature sizes, etc. These considerations often make LTCC-based solutions too bulky and cost prohibitive. In recent years, LCPs have attracted attention because of their PTFE-like properties and availability in flexible films as thin as 25 μm . Because of its near-hermetic and low moisture-absorption properties, LCP can be used as a near hermetic packaging

material or as a capping material. Moreover, it is compatible with PCB processes offering a multilayer packaging solution. However, the high melting temperature (290°C) and relatively high CTE (Coefficient of Thermal Expansion) in the vertical direction increases the fabrication difficulty and reduces the manufacturing yield.

In this work, to satisfy the above requirements, based on the low-cost PCB process, we proposed an AiP multilayer integrated antenna with a rectangular ring^[43]. Fig.21 illustrates the cross-section of the AiP prototype, which is realized using the traditional low-cost PCB process to reduce the cost effectively. The proposed AiP solution consists of four laminates (RO3003 and TLY-5) and three bond-ply layers. As shown in Fig.22, the radiation elements are designed on the top two metals, and the feeding network in metal 4 are apertures coupled to the antenna. The ground metal 3 layers between the radiation and feeding layers act as a shielding layer, minimizing the influence of the feeding line on the radiation. The reflector layer in metal 5 is used to improve the antenna's front-to-back-ratio. Metal 7 is used to realize the low-speed trace and the power plane.

We designed a 16-element phased-array antenna, as shown in Fig.23. In order to reduce the SLL(Side Lobe Level) and to increase the maximum scan angle,

Figure 21 Cross section of proposed phased-array antenna packaging stack-up

the distance between each antenna is set as 3 mm (0.6 wavelength). Here, we modified the rectangular ring dimensions to resemble a rectangular 4-element ring, sacrificing a little antenna gain. Compared with the circular antenna array, the rectangular array has a broader main lobe beamwidth and lower side lobe level when scanning.

Figure 22 Simulated and measured S11 of the antenna array

Figure 23 Layout of the fabricated 16-element phased-array antenna

The 16-element phased-array antenna differential feed lines with identical length are designed with a 200 μm width and 150 μm space that exhibits a 100 Ω differential characteristic impedance. The feeding network simulation results show a maximum loss of 0.8 dB and a maximum phase deviation of 3°.

As shown in Fig.22, the antenna array is aligned in a staggered structure to distribute the balun and feeding line. Simulations confirm that this alignment has little difference on the synthesis array radiation pattern from the 16-element rectangular array. In this design, to investigate the phased antenna array beam steering performance, we fabricated and measured two beam fixed antenna arrays (0° and 30°). Fig.23 illustrates the simulated and measured S11 of the antenna array, which shows a relatively good agreement. The measured 10 dB bandwidth of this antenna array is 15 GHz. The measured radiation pattern of these two phased array antennas is shown in Fig.24. We compared the broadside (0°) antenna array fixed beam with the 30° E-plane fixed beam, and the measured peak gain changes from 16.6 dBi

Figure 24 Radiation pattern of beam-fixed 16-element phased array antenna at 60 GHz: (a) 0° E-plane; (b) 30° E-plane

(simulation 16.2 dBi) to 13.9 dBi (13.6 simulated) at 60 GHz, while the SLL increases from -13 dB to 8 dB. In both cases, we obtained a good agreement between the measurements and simulations. To evaluate the actual 16-element phased-array antenna performance in a package, we also fabricated and measured the feed network. The measured insertion loss of this feed network is 6.5 dB, which is about 4.5 dB higher than the actual differential feed network shown in Fig.3. Thus, the actual 16-element phased antenna array is expected to achieve a gain of more than 20 dB.

It should be noted that to achieve compact terminal size, multiple-antenna systems require that the distance between adjacent antenna elements should be small. However, this will typically result in high mutual coupling, which affects the antenna performance characteristics, such as the bandwidth, gain, and efficiency^[44]. In addition, the system performance will also be affected^[45]. To solve this problem, we can use EBG (Electromagnetic Band-Gap) structures and (WG-MTMs Waveguide Metamaterials) to suppress the mutual coupling between radiating elements. Many groups have focused on adjusting the mutual coupling to control the array antenna performance.

In the design and fabrication phase, the antenna and package parameters should be optimized by performing intense electromagnetic simulations. Moreover, along with the electrical performance, the thermal and mechanical issues should also be considered for future commercial applications.

6 Conclusion

In this paper, we discuss the transmitter key components, receiver, antenna, and packaging design considerations, and we present test results, paving the way for future 5G communication systems. To meet the 5G requirements, we require innovation

in terms of advanced RF transceivers, and from the perspectives of architecture and implementation. With advances in the CMOS process, antenna, and packaging technology, there will be scope to increase the 5G mmWave multi-antenna system performance, improving the energy efficiency and spectrum efficiency.

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