AN INTRODUCTION TO GOLD GETTERING IN SILICON

and a Discussion of Intrinsic Gettering

Thomas A. Baginski

Electrical Engineering Department, Auburn University, Auburn, AL 36849, U.S.A.

Metals, and particularly gold, introduce electrical states into silicon which act as traps for charge carriers. While this is desirable in some devices, in others it degrades performance and must be removed by gettering. This paper discusses the problem, and presents experimental studies on the mechanism of intrinsic gettering of gold.

Over the past two to three decades, semiconductor device structures have evolved from simple discrete components for the replacement of vacuum tubes to complex integrated circuits. The stringent performance criteria of modern integrated circuits have required the production of extremely pure fabrication materials with a minimum of electrical and structural defects.

Production facilities of integrated circuits must be kept clean to prevent material contamination. This is done by the use of specially filtered areas called 'clean rooms', in which typical air contamination is kept to less than 100 particles of size $0.5\ \mu\text{m}$ in diameter, or less, per cubic foot of air. Operators, technicians, and other personnel in such areas, wear protective clothing to reduce the amount of contamination arising from the human body.

The chemicals and gases used in processing are of special high purity electronic grades, thus reducing contamination to processing materials. In an effort to keep the wafers clean, furnace liners, diffusion tubes, carrying trays and a diverse assortment of other articles found in the processing area, are all made of high purity materials.

Temperature and time of thermal treatments, such as diffusions and oxidations, are both carefully controlled to produce the least amount of damage in the wafer.

Despite all these and other precautions taken to ensure a clean processing environment, contaminants and material damage are introduced into the wafer during processing. The contaminants usually, but not necessarily, take the

form of heavy metal impurities such as gold, copper, iron, chromium, nickel, etc. The material damage done to the wafer includes stacking faults and dislocations.

Metals, particularly gold, introduce electrical states in the material which are known as traps. These traps act as centres into which negative charge (electrons) or positive charge (holes) can migrate. Once either an electron or hole falls into a trap it can quickly recombine with a charge of opposite sign, an event referred to as recombination. Charge which has recombined is no longer influenced by an electric field in a semiconductor, and also is no longer available as a charge carrier.

The length of time a charge carrier exists is known as the carrier lifetime. In some cases, very short carrier lifetime is desired; in others, the opposite is true. Power devices, which typically require a very short lifetime, are primarily meant to move a large amount of charge during device switching. The traps aid this process by providing an electrical path within the material for charge to recombine. Thus, when the device is switched, charge can move from a point via the traps, in addition to the paths available due to the circuit elements to which the device is connected.

Other device technologies, such as memory elements, store charge in a cell. The cell's contents can then be read. A cell with charge is read as a 1. A cell without charge is read as 0. It is critical that these trap sites be removed for reliable operation of a device. Thus, in some cases, the addition of gold as a trap improves the electrical performance

of a device; in other cases, the addition of gold degrades the performance. The following discussion will be concerned with the latter.

A significant amount of effort has gone into the removal of heavy metals from the active device area of the silicon wafer. Schmidt and Pearce have performed a study to determine the sources of these various transition metals (1).

Various crucibles, holders, susceptors, slurries and other materials, along with a 3-inch-diameter boron-doped silicon wafer, were irradiated in a neutron flux. The gamma-ray spectra for various contaminants were then analysed to determine impurity concentration. By examining the interaction between silicon and material at each processing step, the introduction of contaminants was monitored.

High temperature oxidation was the processing step which gave rise to the largest quantities of detrimental impurities. The source of the impurities was the quartz tube used in the furnace. A substantial reduction of impurities at this step can be achieved by using either high purity SiC or polysilicon furnace tubes, passing HCl down the tube during oxidation, and passing a gas between the furnace tube and liner. The latter step is meant to provide a reactive gas buffer that prevents impurity passage from liner to quartz tube and from quartz tube to silicon.

The metal parts in a crystal grower can also provide significant contamination if allowed to get hot. Dirty lapping and polishing compounds can also be sources of undesirable contamination.

Since the presence of contaminants in the silicon can result in a degradation of its electrical performance, the semiconductor industry has therefore had to search for techniques to remove metallic impurities and crystalline defects from those areas of a wafer where devices are built.

The removal of impurities or defects is termed *gettering*, and any technique which effects such removal is described as a gettering technique.

Two major areas of gold gettering in silicon are intrinsic and backside gettering. Intrinsic gettering refers to the use of oxygen in the bulk of the silicon to form a sink for metallic impurities (2-12). The silicon ingot, from which the wafer is sawn, has oxygen added to it during the growth stage to produce a constant concentration of oxygen in the wafer, as shown in Figure 1 ('control') (13, 14). The wafer is then subjected to a thermal treatment. The treatment supposedly redistributes the oxygen profile to that as shown in Figure 1 ('denuded'). The high concentration of oxygen in the bulk is thought to form gettering sinks for the formation of metal-oxygen precipitates. Thus, if metals such as gold are introduced into the silicon, they are thought to migrate to the bulk of the wafer, away from the surface where devices are fabricated.

Backside gettering refers to inducing sites on the back-

Fig.1 Theoretical oxygen profiles for an oxygen-doped wafer. 'Control' is initial profile before any thermal treatment; 'Denuded' is profile after high temperature anneal

side of a wafer, which act as gettering sites. These gettering sites are formed by damaging the silicon. The damage is produced using a variety of techniques such as a laser, abrasion, phosphorus diffusion, etc. During subsequent thermal anneals, the damaged areas on the backside act as sinks which are thought to cause the migration of metals from the bulk and surface of the wafer to the backside (15-30).

As can be seen from the foregoing discussion, gettering involves a wide variety of techniques. The remainder of this paper will discuss intrinsic gettering of gold in silicon. A second paper will discuss backside gettering techniques.

Intrinsic Gettering Techniques for Silicon

Intrinsic gettering involves extracting metallic impurities such as gold from the surface of a silicon wafer, and trapping them in the body of the wafer. Since devices are usually built within a distance of several microns from the surface of the wafer, the reduction of surface impurities should directly improve device performance.

The gettering process involves the precipitation of oxygen in the bulk of the silicon. The precipitates strain the silicon lattice, thereby generating dislocations. It has been demonstrated that metals tend to accumulate on or near these dislocations. Since metals are fast-diffusing elements, it has been theorized that during a thermal anneal, metals would migrate from the surface of the silicon wafer to regions of these dislocations. It is therefore of utmost importance to leave the surface free of defects induced by oxygen precipitates, so that metals will be extracted from this area. An oxygen-free 'denuded zone' is formed near the surface by means of a high temperature anneal which permits the out-diffusion of oxygen. This thermal anneal is further followed by treatment to enhance nucleation and

growth of oxygen precipitates in the bulk (13, 14). A typical thermal cycle which produces the desired oxygen profile for intrinsic gettering is shown in Figure 2. The first step is a high temperature (1100°C) treatment to establish a denuded zone near the surface of the wafer. In Figure 1, the denuded profile shows an oxygen concentration profile of a wafer that was subjected to a 2-hour steam oxidation at 1100°C.

The second step in the thermal cycle of Figure 2 is a low temperature (600-800°C) anneal to enhance nucleation sites for oxygen precipitation. At normal device processing temperatures, oxygen occupies an interstitial position in silicon. For precipitates to form and grow, a stable nucleation site is needed. The nucleation site may be a defect, such as a dislocation, or a small oxygen precipitate that formed and remained stable throughout the crystal growth process. The rate of precipitation depends on the size and number of these nucleation sites. The number of nucleation sites can be increased by annealing the wafers at temperatures between 600°C and 800°C. The nucleation rate is strongly dependent on temperature, and is proportional to the square of the oxygen concentration. Annealing temperatures greater than 900°C cause the nucleation sites to dissolve.

The third step of the thermal treatment involves another thermal anneal. The temperature is raised to somewhere around 1000°C to allow for sites nucleated in the second stage to grow.

Wafers which have received the prescribed thermal treatment have seen improvement in both leakage-limited yield and in minority carrier lifetime. These improvements have been theorized to result from the movement of metallic impurities away from the surface due to the gettering sinks formed in the bulk.

Fig. 2 Typical thermal cycle to produce oxygen profile for intrinsic gettering (9, 10)

Experimental Procedure

Silicon wafers used as samples were of high (20-25 ppm atomic) oxygen concentrations. All wafers were (100) oriented, 2-7 ohm-cm, *p*-type, 3-inch-diameter and approximately 400 μm thick. The wafers were cleaved to form quarters. Quarter 1 of each wafer received no thermal treatment. Quarter 2 received no denuding treatment, a nucleation step at 750°C and a 24-hour, 1000°C growth treatment. Quarter 3 received a 1-hour, 1100°C denuding treatment, followed by a 750°C nucleation step and a 1000°C growth anneal. Quarter 4 received a 2-hour, 1100°C denuding treatment, followed by nucleation and growth anneals identical to quarters 2 and 3.

The time of the 750°C nucleation step was varied for wafers of both medium and high oxygen concentration in order to form a variety of oxygen precipitate concentrations.

A spin-on source was used for gold contaminations. The source consisted of silicon dioxide plus gold in an alcohol suspension. Following the application of the source, the quarters were placed in a nitrogen ambient for 20 minutes to evaporate the alcohol. The residue consisted of a glass layer saturated with gold.

The quarters were then annealed at 900°C for 30 minutes. The time and temperature of this diffusion were chosen to ensure that the wafer was saturated with gold. The diffusion length of gold, at this time and temperature, was calculated to be 950 μm . Following the diffusion of gold, the samples were dipped in hydrofluoric acid for 5 seconds to remove the remaining contamination film. The quarters were then replaced in the furnace for 30 minutes at 900°C to redistribute the gold.

For the determination of the concentration profiles of the gold, layers of silicon were sequentially removed by etching in an ultra-pure mixture of hydrofluoric and nitric acids. These solutions were then dried out, the residue redissolved in *aqua regia*, dried out again and this residue then dissolved in a 1 per cent mixture of nitric acid and de-ionized water. This solution was analysed using graphite-furnace atomic absorption spectroscopy. The etched layers were 5 μm thick. To ensure that only the front surface of the wafer was etched, the back side was protected with a wax inert to the etchant. In all cases, blanks were run to check that extraneous contamination levels were below 1 ppb (part per billion).

To begin the analysis, a quarter, having received an identical thermal treatment as one profiled for gold, was cleaved into approximately 30 pieces, each 0.5 cm x 0.5 cm square. The entire set for each quarter was simultaneously immersed in a chemical etch. (The outer half-centimetre of the quarter was disregarded to avoid any edge effects). The samples were then taken out at time intervals which allowed for approximately 1 μm of material to be removed.

The thickness of the wafer was periodically checked with a micrometer. The samples were then inspected, under both an optical microscope and an SEM, to count the number of defects present on the etched surface. In this manner, the defect density (defects/cm²) as a function of depth from the surface of the wafer was determined.

Results and Discussion

By superimposing the gold and defect profiles a direct correlation between the migration of gold and the position of defect sites can be made. It is assumed the density of defects is directly related to the density of precipitated oxygen in a sample.

High Oxygen-content Wafers

a). *Annealing Parameters: no thermal treatment (0 hours at 1100°C; 0 hours at 750°C; 0 hours at 1000°C).* Figure 3 illustrates a typical gold profile for a high oxygen-content control wafer which received no gettering treatment. The solid line represents actual sample points. The dotted lines represent assumed values. The gold profile shows a peak near the surface and drops rapidly as the distance from the surface increases. This is the characteristic U-shaped profile for gold in silicon. The profile shows the location to which gold migrates after a contamination diffusion. The normalized gold scale should be multiplied by 1.6×10^{16} atom/cm³ to yield atoms of gold per cm³ of silicon.

Fig. 3 Typical gold profile for a high oxygen-content wafer which received no gettering treatment

b). *Annealing Parameters: 0 hours at 1100°C; 6 hours at 750°C; 24 hours at 1000°C.* Figure 4 illustrates the profiles for a high oxygen-content wafer which received thermal anneals of 6 hours at 750°C and 24 hours at 1000°C. The left vertical axis shows the linear normalized gold profile; the right vertical axis is a logarithmic scale of defect count in terms of defects/cm².

The gold profile illustrates that most of the gold has migrated from the surface to a peak at a depth of 10-15 µm. The concentration then drops in the bulk and rises again

around 85 µm from the surface. The defect profile shows a low number near the surface rising gradually to a depth of 15 µm. At 17 µm from the surface the defect profile shows a dramatically sharp increase of about two orders of magnitude. This plane of defects is extremely narrow, being of the order of 1 µm wide. The concentration of defects drops again to a bulk value of around 10^4 /cm² and rises again around 85 µm. The two peaks (gold and defect) show a strong correlation. Thus, this graph shows that the gold migrates to a region of high defect density. In addition, an anomalous plane of defects has been observed in the denuded region.

Fig. 4 Gold and defect profiles for a high oxygen-content wafer which received thermal anneals of 6 hours at 750°C and 24 hours at 1000°C

Fig. 5 Gold and defect profiles for a high oxygen-content wafer which received thermal anneals of 1 hour at 1100°C, 6 hours at 750°C and 24 hours at 1000°C

c). *Annealing Parameters: 1 hour at 1100°C; 6 hours at 750°C; 24 hours at 1000°C.* Figure 5 shows profiles for the processing conditions of 1 hour at 1100°C, 6 hours at 750°C and 24 hours at 1000°C for a high oxygen-content wafer. The defect and gold profiles correlate well at a distance of approximately 15 μm with no corresponding peak in the defect profile. This anomaly is explained in terms of the physical dimensions of the plane of defects seen in Figure 4. The plane of defects is extremely narrow and of the order of 1 μm wide. It is postulated that the profiling procedure missed the plane of defects.

d). *Annealing Parameters: 2 hours at 1100°C; 6 hours at 750°C; 24 hours at 1000°C.* The processing scheme was now varied to include 2 hours at 1100°C, 6 hours at 750°C and 24 hours at 1000°C. The gold profile (Figure 6) exhibits two peaks, one occurring at 0-5 μm beneath the surface, the other at 15-20 μm . The defect profile also exhibits two peaks which correlate extremely well with the gold profile. The peak in defect density near the surface of the wafer is approximately 1 μm wide and shows up only 2 μm from the surface. This particular processing sequence results in a plane of defects very close to the surface of a wafer. It ap-

Fig. 6 Gold and defect profiles for a high oxygen-content wafer which received thermal anneals of 2 hours at 1100°C, 6 hours at 750°C and 24 hours at 1000°C

pears in the surface region where devices are built. The plan of defects is very narrow and does act as a gettering sink for the gold.

A second peak in the defect profile occurs at 15 μm and drops sharply again at 20 μm . It corresponds exactly with a peak in the gold profile. The concentration of defects again

rises in the bulk. The defect profile also rises dramatically in what should be the denuded region of the wafer.

From the previous experiments, a number of conclusions can be reached. In general, impurity atoms migrate to regions of high defect density. Thus, gold prefers to reside in areas of high defect (hence high-oxygen precipitate) density. It has also been shown that a thin plane of defects can form in the denuded region of a wafer. The formation of the plane of defects is critically dependent on processing conditions.

Summary of Experimental Results

Silicon wafer samples, doped to saturation point with gold, were given a variety of thermal treatments to produce a range of oxygen-precipitate profiles. Thereafter, the gold concentration profiles of the wafers were determined by etching away successive layers, each 5 μm in thickness, and analysing the etchant solution for gold at the end of each step. In a parallel series of experiments, wafers were cut from the same silicon slices and subjected to the same thermal treatments, but undoped with gold. The wafers then were immersed in an etchant and the defect concentrations in the surfaces exposed at successive depths, about 1 μm apart, were measured optically and by SEM.

It is shown that planes of high defect density (and hence high oxygen precipitation) in the undoped wafers correspond in position with planes of high gold concentration in the doped wafers. This supports the view that defects act as gettering sinks.

However, depending on the thermal treatments, the nucleation of the plane of defects can occur in the active region of a wafer. Thus, gettering sinks may be induced at the worst possible location near the wafer surface.

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