Erratum

In journal issue 2, number 4, the authors' photographs for the paper entitled "Wafer Scale Integration: A University Perspective" were inadvertently reversed. The correct photographs and biographies for D.C. Keezer and D.W. Whittaker appear below.

D.C. Keezer received the Ph.D. degree in electrical engineering from Carnegie Mellon University in 1983. He was previously the Test Technology Group Leader in the Government Systems Group at Harris Corporation, prior to joining the faculty at USF where he is an Associate Professor of Electrical Engineering. He is also currently the Coordinator of the Microelectronics Test Laboratory at the Center for Microelectronics Research.

His research interests include VLSI/WSI design and test, design for test, and high speed and mixed signal test.

D.W. Whittaker received the Bachelor of Science Degree in Electrical Engineering from TriState University in 1969. Until recently he was the manager of VLSI Design and Advanced Technology at the IBM VHSIC Operation in Manassas, VA. He was involved in advanced DRAM, SRAM, and circuit design at IBM for 19 years. Currently he is with the Center for Microelectronics Research at USF.