Signing Off Industrial Designs on Evolving Technologies

Sébastien Marchal

STMicroelectronics, France

Abstract. Many specific challenges need to be addressed in current SOC designs to offer a competitive product. Chip content become highly heterogeneous, performance has to be on the leading edge and robustness needs be guaranteed. Besides the technical merits, the "date of availability" of the product plays a key role in its overall competitiveness. Therefore, as schedule pressure is increasing, moving to new technology requires more parallelization of activities that used to be done serially. When the technology brick, which is the first link of the chain, moves through various maturity levels, the whole edesign process may be impacted. Traditionally, the impact of such evolutions were not anticipated. Layouts were updated as a consequence of design rules changes. "Brute force" timing margins were put in the models regardless of design specificities. Design For Variation techniques operate at design flow, SOC design and library/IP design levels to anticipate those variations. Different examples of Design Rules changes or Timing variations are discussed, and techniques to handle such changes are covered. Some aspects of Silicon process corners variations are also presented. Part of the talk covers clock network building techniques which are variation friendly. Impact of such techniques on final design analysis, also called SignOff, are demonstrated. How DFV can simplify SignOff is finally discussed.