Parallelism in Current and Future Processors – Challenges and Support for Designing Optimal Algorithms (Invited Talk)

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Abstract. Both explicit usable and implicit transparent parallelism is nothing really new in processor technology but has been restricted to high-end computer systems accessible to only a few developers. In recent years, however, parallelism on all levels has found its way into even the cheapest desktop and notebook system and thus every algorithm being developed today should reflect this change to optimally exploit these additional resources.

This session will outline the parallelism offered by current Intel processors and some new parallel enhancements of future architectures including the many-core approach implemented by Larrabee and the coming improvements for data-parallel (SIMD, SSE) execution. Some of these enhancements will introduce new challenges to the algorithm designer and developer. This includes the massive number of available hardware-threads, the increased size of vector operations, and non-uniform memory access. Intel actively looks for new parallel programming models to tackle these challenges including CT, Software Transactional Memory and Concurrent Collections for C++. While these models might make it into future program development environments, there are multiple developer tools for parallel program development as mature products available today – including compilers, libraries, thread checker/debugger, performance analysis tools using hardware performance counters etc. The talk will outline how some of these tools as offered by Intel and how they can facilitate the complete development cycle for parallel program development.