FPGA Design Productivity - A Discussion of the State of the Art and a Research Agenda

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Abstract. As we near 20 years of history with reconfigurable computing there is continued (and even increasing) interest in design productivity for RC. Configurable computing machines (CCMs) based on FPGAs are touted as re-usable, re-configurable platforms for accelerated computing, but the fact remains that FPGAs are simply not that easy to “program”, even after all this time. Why? The usual list of suspects is familiar to most, and includes challenges with timing closure, gate-level design, fixed-point arithmetic analysis, communication management, and clock cycle level control of design resources, to name a few.

To address these problems there continues to be much research in the community on higher-level languages, reusable core libraries, improved CAD tools, debug infrastructure, etc. While these research activities focus almost exclusively on CAD, there are other interesting and often overlooked pieces of the productivity puzzle. One such puzzle piece is circuit and architectural support for design productivity. Another puzzle piece poses the question: how is the RC landscape changing with the introduction of new devices (many/multi-core and coarse grain)? A final consideration is to look at the entire design productivity picture — if all the puzzle pieces were fit together into a comprehensive approach for improving productivity, is a 10× increase feasible? 20×? If so, at what cost?

This talk will focus on the above questions in the context of design productivity for FPGA application development, introducing the productivity problem, and identifying select issues which are key to providing radical design productivity improvements. It will then drill down on those key issues, showing the range of improvements possible using recently published and unpublished research results from a variety of venues.