On Parallel Models of Computation

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Abstract. The emerging trend on multi-core chips is changing the technology landscape of computing system in the scale that has not been witnessed since the Intel microprocessor chip commissioned in early 1970s. However, the implication of this technology revolution is profound: its success can only be ensured if we can successfully (productively) implement parallel computer architecture on a chip as well as its associated software technology.

Recently, a great deal has been said, studied, and written on the transaction memory model and its implementation as a promising solution for parallel programming/execution models and their architecture support – especially in the multi-core era. In this talk, we present a review on two types of memory events and their ordering in a parallel program - due to the data (or control) dependence and the mutual exclusion, respectively. We argue that the solutions based on the transaction memory model are intrinsically inefficient to support the fine-grain memory synchronization due to the data (or control) dependence in parallel programs in the scientific computation domain. We then comment on some fundamental work on parallel models of computation that goes back to 1960s and early 1970s that should be freshly reviewed and extended to resolve the new challenges in parallel architecture and software models presented by the multi-core chip technology.