Built-in test of analog non-linear circuits in a SOC environment

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Abstract This work describes a methodology for the built-in test of non-linear analog circuits, developed at the system level, by the use of digital non-linear adaptive filters. Non linear analog circuits are widely used on data transmission applications, such as wireless communication, radio and portable multimedia systems. Several non-linear circuits like mixer, automatic gain control amplifiers, peak-detectors and log-amplifiers were simulated, and some prototypes assembled, in order to allow fault injection in the circuit under test. The proposed built-in test methodology is very precise, has low cost when seen at the system level, and allows complete fault coverage with a very small testing time.

Key words: analog built-in testing, non linear circuits (mixer, agc, peak-detector, log-amplifier), non linear adaptive filters

1. INTRODUCTION

Although there has been a lot of work in the area of built-in test of linear analog circuits [1-6], the built-in test of non-linear analog circuits has been limited to AD and DA converters, and some experiments on PLLs. Other important circuits, used mainly in communication devices (like mixers, log-amplifiers and others presented here) are non-linear in nature. To the authors' knowledge, built-in test for mixers and other non-linear circuits has not been extensively addressed before. One of the reasons is that all the

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theory that can easily be applied to linear circuits (s and z transforms) is not adequate to deal with non-linear components. In [7-8] a discussion on where to insert test points in communication circuits using mixers and data converters has been presented. A built-in strategy to test the mixer itself was not considered. In [9], some design for testability issues were addressed to both reduce production test cost and improve test quality for automatic gain controllers.

In the era of Systems-on-Chip (SOC), a built-in test strategy that can benefit from other hardware already available in the system is likely to have lower area and performance penalties. Nowadays, almost all applications rely on some sort of digital processing of signals, from low level signal acquisition and filtering to complex multimedia applications like voice and video processing. A real-life example of such complex mixed signal devices is the Software Radio, a SOC by itself [10-12].

This way, aiming at extensive reuse of components and accurate and low cost built-in analog test, this work presents a built-in test methodology that uses common digital hardware found in most present-days SOC to test non-linear analog circuits, also present in the SOC. All testing is performed using non-linear adaptive filters developed in the digital domain. Adaptive Filtering has already been proved to be a powerful technique for linear systems testing and identification [13-14]. The main goal of this work is to use adaptive filters for identification and testing of non-linear systems.

The proposed test technique extracts the analog signature of the circuit under test and stores it as filter coefficients in the digital domain. Then, no precise knowledge of the circuit must be acquired. To the author's knowledge, this is the first proposed methodology targeting built-in test of different integrated non-linear analog circuits at the SOC level.

This paper is organized as follows: section 2 presents the proposed testing procedure, while section 3 presents the results achieved for this methodology, both in simulation and real life prototypes. Section 4 presents an analysis on the required resolution and frequency of the analog to digital converters used during testing. Finally, section 5 presents our conclusions and future work.

2. THE TESTING PROCEDURE

The theory regarding linear and non-linear system recognition using Digital Signal Processing techniques (DSP) is well developed [14] and is the basis of the work presented in [13]. The methodology of analog circuit recognition using adaptive filters is shown in figure 1. In the first phase (figure 1a), known as training phase, a fault-free system and the adaptive

filter are submitted to the same excitation and their outputs are compared. The error signal helps to calculate the filter coefficients to the next iteration in the training phase.

Figure 1. Adaptive Tester Topology

After the training phase, the filter coefficients have stabilized, and the filter can now reproduce the circuit behaviour under all situations for which it has been trained. Then, the fault-free system is replaced by the system to be tested and the error signal is used to detect system failures (figure 1b). This is called the testing phase. Both the circuit and the filter are submitted to the same input and their outputs are compared, generating an error signal. Hopefully, any fault in the system, either a hard, soft or catastrophic fault, will change the output of the tested system, which will be detected by the filter and compared to a tolerated error to indicate if the system is error free.

The error signal (figure 1b) indicates whether the system is fault free or not. It is important to notice that, although it is very close to zero, the error signal for the fault free system is not zero. However, the error signal for the faulty system is much larger than the fault free signal, thus indicating a failure in the tested system. A threshold value that indicates whether a system is faulty or not must be determined. Usually, this is done experimentally. A higher threshold implies that more systems will be classified as fault-free system, and then one can say that the tester is more tolerant or flexible.

As it is shown in figure 1, the proposed testing methodology requires the use of Analog to Digital converters. This is because the adaptive non-linear filter is developed in the digital domain, while the system under test works in the analog domain. However, in a mixed signal SOC like the Software Radio, for example, fast DA and AD converters are readily available [10-11, 22]. The use of a digital filter is favoured because of available design automation and construction robustness, not to mention its spread use on most present days SOCs. The influence of the resolution of the required analog to digital converters and some comments about their speed is studied in section 4.

2.1 Filter Algorithm and Topology

The most common topology for linear adaptive filters uses a Finite Impulse Response Digital Filter (FIR), mainly because of stability reasons. Although FIR filters are stable, an adaptive FIR filter can be unstable under some conditions [15]. On the other hand, for non-linear systems, many topologies have been studied, and probably the Volterra equations is the most common equation set for modelling these systems [15].

The topology proposed here is implemented with a non-linear FIR filter. The implemented filter can be represented by equation (1).

$$Y(n) = \sum_{m=0}^{N_1-1} (c_1(m)x_1(i-m) + c_2(m)x_2(i-m)) + \sum_{m=0}^{N_2-1} c_x(m)x_1(i-m)x_2(i-m) \quad (1)$$

$Y(n)$ is the output of the filter at discrete time n . N_1 and N_2 are the number of taps on the linear and non-linear components of the filter, respectively. The filter coefficients are $c_1(0...N_1-1)$ and $c_2(0...N_1-1)$, in the linear, and $c_x(0...N_2-1)$ in the non-linear components.

The filter adapts to any circuit, provided it has enough taps (pair coefficient-sample) to represent all poles and zeros of the original system. To decide which signal to use to train the filter and test the system, we should consider that the signal must last enough for the filter to converge and must be rich in frequency components, in order to provide excitation of the circuit under test at all frequencies of interest.

The main difference between our work and other non-linear filter topologies is that we develop a non-linear FIR filter with two inputs, instead of only one. This comes from the concept that, while in a linear system, the output can only present a sum of all inputs in a scaled and phase modified

version. In a non-linear system, frequencies that are not present at the input can be generated internally. Since $\cos(a) * \cos(b) = 1/2[\cos(a+b)+\cos(a-b)]$, it is clear that the multiplication of two cosines produces as a result two new frequencies, that were not present at the original inputs, but are a combination of both. If the difference between these two frequencies is large (say, 10 times, as it happens in heterodyne receivers [16-17]), it is very hard to obtain, with only one non-linear input, all the necessary frequencies to test the circuit in its entire frequency spectrum.

The algorithm for updating the filter coefficients during the training phase is the LMS, one of the simplest adaptive algorithms. Some experimentation is needed to determine the algorithm coefficients. Further details can be found in [18].

2.2 The input signal generation

In the testing case presented above, one relies on the accurate generation of an excitation signal. Again, considering the built-in test of the proposed analog non-linear circuits in a SOC environment, it is very likely that a DA converter might be available for a loopback test mode. This way, one can generate the excitation signal in the digital domain, and after use a DA converter to reach the desired analog circuits. For example, in the context of the Software radio or other application that requires bi-directional communication or interfacing with the real world, a pair AD/DA converter is most likely to be present.

The set of frequencies to be used as excitation for the circuit under test is another issue. Generally, white noise is the preferred choice, since it has enough frequency components spread trough all the spectrum of interest, and it is easily generated within the digital domain (with a LFSR, for example), considering the pass-band limitations of the circuits to be tested.

3. EXPERIMENTAL RESULTS

In order to check the coverage of the test procedure presented in this work, this section provides some test cases that were both simulated and prototyped in our laboratories. The simulation results were obtained using MatlabTM as the modelling and simulation tool. Also, an analog mixer was built by the authors with real life discrete components, so that it was possible to inject faults in the mixer and observe its output signal. This data was acquired with a digital oscilloscope and later used in MatlabTM, where the non-linear adaptive tester was implemented. All testing procedure was done off-line.

3.1 Analog Mixer

A prototype mixer [23] was assembled and is shown in figure 3. The input signals x_1 and x_2 are represented in the diagram by the AC sources vin_1 and vin_2 . The output signal is differential, measured between points V_1 and V_2 . With this experiment we are interest in making actual fault insertion to check the behaviour of the pair mixer-adaptive tester.

Figure 2. The prototyped mixer

3.1.1 Component Deviations

The first type of failure that was simulated in the mixer was a deviation in the nominal value of the components of the circuit. We simulated faulty resistors for components RC1, RC2, RE1 and RE2, and after open and short faults for all the transistors in the system. Table 1 and table 2 show the error signal ratio for the faulty system and the fault free system in some test cases. For a complete table, with all the component deviation that was simulated, please refer to [18]. A unitary ratio means that the fault was not detected by the proposed testing procedure. Observing the results, it is possible to verify that the procedure is able to detect component deviations as small as 1% very easily. Also, shorts and open faults in the transistors produce an error signal that is much higher than the error signal of the fault free mixer.

Table 1. Output error ratio – resistor faults

	0%	+1%	-1%	+10%	-10%
RC1	1.00	163.41	163.68	1.63e+03	1.64e+03
RC2	1.00	163.46	163.59	1.62e+03	1.64e+03
RE1	1.00	18.39	18.90	177.56	195.97
RE2	1.00	18.68	18.54	177.51	195.30

Table 2. Output error ratio – transistor faults

	open	Short
Q1	1.50e+04	1.52e+04
Q5	2.12e+03	3.93e+03

3.1.2 Third Harmonic Interference

This section addresses the third harmonic interference problem, an important design parameter for communication circuits. The results presented here were simulated in MatlabTM. A third harmonic component was inserted in the local oscillator (input signal x_2) and the error signal was analysed. Table 3 summarizes the results.

As one can see in table 3, a very small (1/1000) third harmonic component in the output signal produces an error signal that is much larger than an error free output, being easily detected.

Table 3. Output error ratio

Amplitude	Error Power Ratio
0	1.00
1/10	6.62e+03
1/100	6.62e+02
1/1000	66.11

3.1.3 Voice Signal Testing

In order to verify the fault detection of the proposed testing methodology at the presence of complex signals, the RF mixer was excited with a voice signal (like in an actual modulation procedure, for example). First, a fault free system was tested. Later on, a faulty mixer, with a 5% frequency deviation in the local oscillator, was tested. Figure 4 shows the output signal and figure 5 shows the error signal for both testing cases.

As it can be seen, both outputs are very similar, but the error signal power for the faulty system is larger. While the error signal in the fault free mixer has a mean power of 0.0088, the faulty mixer has a mean power of 0.0171, that is 93% larger.

Figure 3. The input voice signal

Figure 4. Error signal for the voice signal

3.2 Automatic Gain Controller

An automatic gain controller (AGC) was simulated using MatlabTM. The input is a sinusoidal signal attenuated by an exponential signal, $v_i = A \cos(\omega t) \cdot 0.9^k$. The desired output of the ACG is the sinusoidal input with no attenuation. In the adaptive filter, the input signal x_1 is the input signal of the AGC, while the gain signal of the AGC is the input signal x_2 .

It is possible to observe in table 4 that a catastrophic fault like a short capacitor is easily detected by the testing methodology. Some component deviations are also detected by the proposed testing methodology. If the AGC produces a gain signal that is 1% larger than expected, the error signal is almost 10% larger when compared to the fault free system.

Table 4. Output error ratio

Fault simulated	Error Power Ratio
Short capacitor	3.28
Gain stuck at 1	2.29
1% error in gain signal	1.09

3.3 Peak Detector

A peak detector was also simulated in the Matlab™ environment. As a peak detector has only one input, the inputs of the adaptive filter were short-circuited, so that $x_1 = x_2$. During simulations, we inserted faults so that the peak detector under test could not sustain the peak voltage for a long time. Table 5 shows the error signal ratio for the faulty and the fault free peak detector.

Table 5. Output error ratio

Voltage sustained (%)	Error Power Ratio
95	3.00e+04
99	1.19e+04
99.9	2.35e+03
99.99	351.42

3.4 Log-amplifier

A logarithmic amplifier was modelled and simulated in Matlab™. A log-amp is a one input circuit, like the peak detector, and then again the inputs of the adaptive filter were shortened. Equation 2 was used to model the log-amp in Matlab™.

$$V_{out}(i) = (R_2 / R_1 + 1)V_t \ln(i / i_{ref}) \quad (2)$$

Faulty resistors and sources were simulated and table 6 shows the error power ratio for the fault free system and the faulty system.

Table 6. Output error ratio

	R1	R2	I _{ref}
+10%	1.44	1.55	1.71
-10%	1.69	1.55	1.71
+20%	2.33	2.84	3.05
-20%	3.48	2.72	3.66

4. THE REQUIRED RESOLUTION AND SPEED OF A/D CONVERTERS

All the results presented up to now considered a 16 bit A/D converter, that is almost an ideal assumption. In real life systems, there are different precision A/D converters, from 6 to 16 bits.

To determine the sensitivity of the proposed testing methodology to different precision A/D converters, we simulated several converters, from 6 to 16 bits. Table 7 shows the mean error value for the fault free system. Note that the more resolution available in the converter, the better is the error value for a fault free system. This means that one can assume a smaller threshold value in determining whether the system under test is good or not, which leads to more precise testing results.

Table 7. Mean error value

	Mean error value (fault free system)
6	8.2e-03
8	2.8e-03
10	8.2e-04
12	1.9e-04
14	4.6e-05
16	1.2e-05

The third harmonic interference problem was also simulated with different A/D converters and table 8 reports the different error ratios. Observing table 8, it is possible to see that as the precision of the A/D converter increases, the testing procedure performs better. However, even with lower precision converters, the testing was also successful. Among all the third harmonic interference that were simulated, only one failure was not detected, when the third harmonic component had an amplitude 1/1000 and the system used an 8 bit A/D converter. With the same amplitude (1/1000) for the third harmonic, a system with a 10 bit A/D converter reported an error signal that is 37% higher than the error signal in the fault free mixer.

Table 8. Error power ratio

Amplitude	8-bit A/D	10-bit A/D	12-bit A/D
0	1.00	1.00	1.00
1/10	33.33	104.22	447.05
1/100	3.32	10.28	44.76
1/1000	1.00	1.37	4.28

One important point concerning the use of the proposed method is the speed of used AD and DA converters. It is true that although mathematically robust, for high-speed circuits the method presented in this paper depends heavily on the availability of high-speed analog to digital converters. Present day AD and DA converters have a limited sample ratio, when one thinks on actual communication frequencies requirements. For example, one can find commercial AD and DA converters reaching 1G samples/second, with 8 bits resolution [10,22]. However, the power consumption of such devices makes them inadequate for portable equipment.

For some RF frequencies, fast and low-power converters are available [19], but for Gigahertz applications they are still missing. Nevertheless, there

have been appearing ever more publications regarding the integration of $\Sigma\Delta$ converters directly on the RF signal path, as in [20]. Moreover, some of the present work into RF AD converters focus on the integration of the mixer and the converter in a single unit, like [21]. This way, it is possible that in a near future this same testing technique can be applied to online testing of non-linear analog circuits working at Gigahertz speeds.

5. CONCLUSIONS AND FUTURE WORK

This paper addressed the difficult topic of built-in testing of non-linear analog circuits like RF mixers, automatic gain controllers, peak-detectors, and log-amplifiers. The test methodology here presented allows the construction of a built-in self test mechanism that is precise, and can take benefit from other modules available at the system level. The proposed technique can be applied to RF communication systems and multimedia portable SOCs, like the Software Radio, for example.

Faulty mixers were both prototyped and simulated, and the testing procedure was able to detect component deviations as small as 1%, and third harmonic component interference as low as 1/1000. All other circuits were simulated in Spice and MatlabTM, and small component deviation faults were successfully detected. Also, the required AD and DA converters resolution and speed was addressed.

The area penalty of the proposed approach is minimal, since most of the hardware is already available in the SOC. Area penalty will come mainly from switches to maintain the loopback configuration during test.

As a future research topic, the authors intend to verify the possibility of using low-speed and hence low-power converters in the test path, so that together with extra analog hardware, one can reach GHz frequencies without power penalties. Also, it would be interesting to evaluate the power consumption of the proposed technique with a purely non-linear analog built-in technique, which has yet to be developed.

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