CMOS Mixed-signal Circuits Design on a Digital Array Using Minimum Transistors

Jung Hyun Choi and Sergio Bampi

Microelectronics Group (GME), Informatics Institute, Federal University of Rio Grande do Sul (UFRGS). Av. Bento Gonçalves, 9500 - Campus do Vale - Bloco IV. P.O. 15064 - 91501-970 - Porto Alegre - RS – Brazil. Phone/Fax: +55-51-33167036 / 33167308

Abstract: This paper presents an analog semi-custom design using association of minimum channel length transistors for mixed-signal system applications on pre-diffused digital arrays. The Trapezoidal Association of Transistors (TAT) mimics the behavior of a full-custom single transistor, which should have an arbitrary geometry, using only a composition of regularly and linearly placed digital-based transistors in an array like SOT (Sea-Of-Transistors) style. TAT transistor achieves an analog performance that is similar to the single device. Basic analog building blocks were fabricated and tested using both semi-custom and full-custom design methodologies. Simulation and experimental results are for technologies at CMOS 1.0 μ m and 0.5 μ m.

Key words: TAT transistor, Pre-Diffused SOT array, Analog and Mixed-Signal Design, Building Blocks

1. INTRODUCTION

To rapid ICs design, pre-diffused digital arrays are largely employed, which are good alternative to decrease the design turnaround and prototyping time. Silicon area and speed are often larger than the equivalent full-custom version. Advantages are that the design is at high level of abstraction and the remaining steps are automated (positioning&routing), use of pre-defined cells and IP (Intellectual Property) blocks from the libraries.

Available technologies are not well appropriate for analog applications and analog technologies are still costly alternative and mixing analog-digital circuits can be prohibitive. Therefore, several performance issues come up when implementing an analog circuit in an environment traditionally

The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: [10.1007/978-0-387-35597-9_40](https://doi.org/10.1007/978-0-387-35597-9_40)

M. Robert et al. (eds.), *SOC Design Methodologies*

© IFIP International Federation for Information Processing 2002

dedicated for digital applications. Noise, DC and AC performances of MOSFETs are poor compared to bipolar devices. Mixed-signal and analog-digital circuits placed side-by-side on same silicon chip causes cross-talks and increased noise levels. Even in the traditional design methodologies, analog design is not straightforward. The design difficulty increases in the digital technology environment. It demands better device modeling and new design techniques. Also it needs improvement on CAD tools that reflect more accurately the linear and non-linear behavior of the devices, counting RF behavior and effects.

Consequently, analog design is a difficult task, as the digital array and technology are designed to stress the performance requirements of the large digital blocks, that most likely comprise the overwhelming majority of the transistors effectively used in the array. The alternative to overcome and/or improve on these characteristics is applying a specific discipline for designing the analog blocks on fixed-size transistors, that is, the principle of TAT. Unit transistors on SOT array were designed in such a way to facilitate migration to down-scaled technologies taking into account solely the digital circuits demand for speed (only L_{min} transistors) and adequate average digital load drive for local routing. Comparisons between TAT and single versions are presented for common-source amplifier, comparator and folded-cascode OTA designed and fabricated in both methodologies.

2. THE TAT TRANSISTOR TECHNIQUE

The principle of TAT transistor was demonstrated earlier at the device level by Ricc [3], showing that enlarging the channel width at the drain end of the channel (trapezoidal shape – small source, large drain), shown in Fig. 1a, results in a substantial improvement on the output conductance in saturation region. Furthermore, Galup-Montoro [2] established that the series-parallel association of discrete transistors emulates an equivalent single transistor.

The TAT is a combination of the previous techniques, i.e., a trapezoidal series-parallel association of transistors, shown in Fig. 1b, using only minimum channel length transistors. The transistor variable sizes and geometry for electrically equivalent MOS channel lengths and widths required for analog design is achieved with appropriate association of the unitary transistors available on the SOT array. Details of this technique are better described in [1], [6].

Figure 1. (a) Trapezoidal MOSFET [3]. (b) TAT: series-parallel association of unitary transistors.

Figure 2. : TAT: simulated $V_x \times V_{DS}$. $ND=17$, $NS=4$, $L_{min}=0.5\text{mm}$.

Consider the series transistors, MD and MS at the drain and source ends, respectively shown in Fig. 1b. The equivalent conductance (linear region) is given by an equivalent aspect ratio of the association as [2]:

$$\left(\frac{W}{L}\right)_{Eq} = \frac{\left(\frac{W}{L}\right)_D \left(\frac{W}{L}\right)_S}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_S} \quad 2.1$$

where $(W/L)_D$ and $(W/L)_S$ are, respectively, the aspect ratios of the top parallel association MD and the bottom parallel association MS transistors. Equation 2.1 can be rewritten as follows:

$$\left(\frac{W}{L}\right)_{Eq} = \frac{m}{m+1} \left(\frac{W}{L}\right)_s \quad 2.2$$

with:

$$m = \frac{\left(\frac{W}{L}\right)_D}{\left(\frac{W}{L}\right)_s} \quad (m > 1) \quad 2.3$$

Taking into account the limit of the function in 2.2, from $m=1$ to $m \rightarrow \infty$, TAT aspect ratio will vary between a half of the MS aspect ratio and its physical individual value. Therefore, we must impose an aspect ratio to the MS greater than the required aspect ratio and smaller or equal than twice this value in order to get a trapezoidal association.

Regarding again Fig. 1b, to achieve improvement (decrease) on the output conductance [8], the channel width of MD must be larger than the width of the MS, as described in [2] and [3]. In fact, MD is obtained by having N_D unit transistors in parallel and similarly N_S unit transistors in parallel for MS, where N_S is smaller than N_D , in order to keep the principle of trapezoidal geometry. The association shown in Fig. 1b is the basic building block for analog design in a digital SOT array.

The intermediate node voltage V_x , Fig. 2, is clamped at a fraction of the pinch-off voltage of the MD source end terminal. This effectively limits the MS drain voltage to be the channel saturation voltage for a given V_G , which keeps MS in the linear region. MD and MS have the same gate voltage, then they have the same channel pinch-off voltage [9], [10], therefore, for both MD and MS in strong inversion, considering MD is saturated, V_x is given by:

$$V_x = \left[1 - \frac{1}{\sqrt{1 + N_D/N_S}} \right] V_P \quad 2.4$$

where V_P is TAT pinch-off voltage. Above expression shows clearly the advantage of the TAT to be trapezoidal, i. e., V_x approaches to V_P . Since the transconductance of TAT is roughly the MS transconductance (equation 2.6) and it is in the linear region (onset to saturation), the TAT transconductance is directly proportional to MS drain-to-source voltage or V_x .

The MD and MS are the equivalent transistors obtained by several unit transistors physically laid out in parallel. Therefore, the equivalent threshold voltage is in fact an averaging over many unit transistor threshold voltages. This averaging in fact compensates the higher spread of V_T for minimum

lengths. Offset voltages should improve by using such composite TAT devices in deep sub-micron circuits.

TAT is trapezoidal and channel lengths are the same for both MD and MS transistors (only the electrically equivalent L_{eq} of TAT is variable). Then, MD is always made wider than MS and its width is not the minimum and the threshold voltage of MS will not be larger than that of MD, given the presence of body effect. Additionally, TAT can be used in several analog low voltage applications because it works as an intrinsic self-cascode (a second gate bias for MD is required for a traditional cascode).

Improvement, i.e. reduction, on the effective output conductance is effectively achieved for a TAT (in relation to minimum channel-length unit transistors), because it is similar to the traditional cascaded MOS transistors. Then, the output conductance is given by traditional expression:

From 2.5, the output conductance of MD $g_{ds_{MD}}$ is represented by a large value, typical of the worst-case minimum channel length transistor, which is effectively reduced by the transconductance of MD. The effective transconductance of TAT transistor is given by:

$$g_{m_{TAT}} = \frac{g_{ds_{MS}}}{g_{m_{SD}}} \left[\frac{g_{m_{GS}} \cdot (g_{m_{SD}} + g_{s_{MD}})}{g_{ds_{MD}} + g_{m_{DS}}} + \frac{g_{m_{GD}} \cdot g_{m_{DS}}}{g_{m_{DS}} - (g_{m_{SD}} + g_{s_{MD}})} \right] \cong g_{m_{GS}} \quad 2.6$$

According to 2.6, TAT transconductance is determined mainly by MS transconductance. Hence, to improve overall TAT characteristics one needs to increase the MS transconductance and improvement on the effective output conductance one has to increase mainly the output impedance or the MD transconductance. Thus, MD mainly determines the output conductance and MS determines the TAT transconductance.

In Fig. 3 is the experimental output conductance for TAT with channel length $L=1.2\mu m$ and channel width $W=51\mu m$, compared to the equivalent single transistors. It shows clearly that the TAT output conductance is similar to the single transistor. At lower gate drive (1.5V) the short channel effects of V_T reduction and Drain Induced Barrier Lowering (DIBL) combine to give a larger g_{ds} both in conduction and saturation regions.

Figure 3. TAT: experimental output conductance at $V_G=1.5V$, $V_G=2V$ and $2.5V$. 0.5mm technology: $L=1.2mm$, $W=51mm$ ($N_D=10$, $N_S=10$, $W_u/L_u=5.4/0.6$).

The total equivalent noise power at the input present in the TAT transistor is given by:

$$V_{n_{TAT}}^2 \Big|_{in} = \left\{ \frac{N_D \cdot (g_{mG_{MD}}^2 \Big|_u)}{[N_S \cdot (g_{mG_{MS}} \Big|_u)]^2} + \frac{1}{N_S} \right\} \cdot V_{n_{rk}}^2 \Big|_u + \left\{ \frac{N_D + N_S}{[N_S \cdot (g_{mG_{MS}} \Big|_u)]^2} \right\} \cdot I_{n_{th}}^2 \Big|_u \quad 2.7$$

where $V_{n_{rk}}^2 \Big|_u$ and $I_{n_{th}}^2 \Big|_u$ are the flicker noise and thermal noise of each unit transistor. Comparing above expression to the equivalent single transistor, TAT is noisier. Electrical simulation and experimental results (for OTAs) demonstrated that thermal noise is similar, however flicker noise is larger for TAT. The $1/f$ noise can be minimized increasing the MS (or TAT) transconductance.

3. BASIC ANALOG BLOCKS USING TAT

Main parasitic capacitances in TAT are the gate-source capacitance from MD (in saturation) and from MS (in conduction) is the gate-source and gate-drain capacitance, shown in Fig. 4. The combination of parasitic capacitances is larger for the TAT than in its equivalent single transistor.

The presence of intermediate node in the TAT (pole) increases the total parasitic capacitance seen at the input. Nevertheless, due to the self-cascode effect the gain bandwidth is similar to the single transistor. Indeed, the product gain-bandwidth (GBW) is increased by this effect. In Fig. 5 it is shown clearly by electrical simulations for common-source amplifiers

(PMOS type current source). Channel lengths, widths and W/L ratios are exactly the same values for both TAT and single transistors for better comparison purposes, as indicated in the figure caption.

Figure 4. TAT: AC model with body effect.

Table 1. Track-and-Latch comparator: measured performance in 0.5mm CMOS technology.

	Full-custom	SOT array
V_{DD}	3V	3V
C_L	10pF	10pF
f_{max}	41.1MHz	30.5MHz
V_{os}	7.33mV	14.2mV
I_{tail}	$\sim 80\mu A$	$\sim 90\mu A$

Table 2. OTA: measured performance in 1.0mm digital CMOS technology.

	Full-custom	SOT array
A_V (db)	64.5	62.9
GBW(MHz)	0.186	0.514
@ C_L (pF)	82.4	53.5
GBW @ 50pF	0.307	0.550
V_{os} (mV)	+30	-15
SR (V/ μs)	0.42	1.10
@ C_L (pF)	82.4	53.5
PM ($^\circ$)	79.4	51.7
$V_{o_{max}}$ (V)	+1.1/-0.7	+0.9/-0.9

Fig. 6a shows the total equivalent noise power source at the input of common source amplifiers. It is clear that the flicker noise is almost 5 times larger in TAT transistor. In Table 1 is shown the simulated performance reached by the track-and-latch comparator. Maximum switching clock frequency for TAT version is approximately 25% lower and sensibility is twice larger. However, TAT has shown good performance.

Figure 5. Common-source amplifier: gain and phase margin. Electrical simulation using TAT (dotted) and single (solid) transistors. $(W/L)_{eq}=106/1.9$ in $0.5\mu\text{m}$.

Figure 6. Total equivalent noise power in TAT (solid) and single (dotted) transistors. (a) Simulated noise for common-source amplifiers. $(W/L)_{eq}=106/1.9$ in $0.5\mu\text{m}$. (b) Experimental noise for OTAs in $1.0\mu\text{m}$.

A single-ended folded-cascode OTA - Fig. 7b - in both SOT (using TAT transistors) and full-custom methodology [6], [7] were also implemented to allow better performance comparisons. In Table 2 the comparison of results for electrical simulations and experimental measurements are depicted for both SOT array and full-custom OTAs.

The load capacitances were estimated from electrical simulation of expected output current and measured slew-rate. It is worth noting that the SOT version of the OTA has similar (unit gain frequency $1.9\times$ times higher) gain-bandwidth. It is expected because the TAT is an intrinsic cascode (self-cascode pointed out previously).

Offset voltage in SOT version of the OTA is smaller than the full-custom version due to its better intrinsic layout configuration, that is, naturally the TAT devices are very similar to the interdigitated layout technique that is widely used in full-custom layouts.

Figure 7. (a) Track-and-Latch comparator. (b) Folded-cascode OTA.

Figure 8. Die photos: OTA on SOT array (a) and the same OTA in full-custom (b).

Total noise power spectral densities measured in both OTAs are shown in Fig. 6b. The flicker noise in both are large due to its dependence on the OTA input differential pair geometry (area WL) [4], [5]. Thermal noise in SOT version is almost similar (slightly higher) to the equivalent full-custom version, as predicted previously.

In Fig. 8 are shown the die photos of the folded-cascode and in Fig. 9 is shown the chip-test containing OTA, comparator and transistor structure in both SOT array (TAT devices) and full-custom.

Figure 9. Test-chip die photo: Transistor structure, Track-and-latch comparator and folded-cascode OTA. 0.5 μ m CMOS technology.

4. CONCLUSION

This paper demonstrated the TAT technique, which can be used in many analog applications without major penalties. One has to deal with the demonstrated noise figures. It is noisier than the single transistor counterpart. However, using a large number of minimum-size transistors in the TAT, the worse characteristics with respect to noise can be compensated, while keeping the same equivalent W/L . TAT transistors, as shown herein, are not restricted only for semi-custom arrays. It can be used advantageously even in full-custom analog integrated circuits, as shown by the sub-circuits implemented in SOT array using TAT.

Even though the total noise is large and some natural limitations exist, TAT transistors in SOT methodology presented good performance. It is a good trade-off for a given application between performance, cost and design time turn-around.

5. ACKNOWLEDGEMENTS

The support of CAPES and CNPq Brazilian R&D Agencies and of the Analog VLSI Laboratory at OSU, USA, is gratefully acknowledged.

6. REFERENCES

- [1] Aita, A.L.; Bampi, S. "Design of Mixed Digital-Analog Circuits on a Digital Sea-of-Transistors", In: *International Symposium on Circuits and Systems*, Hong Kong. *Proceedings...*, ISCAS, 1997, p.2028-2031.
- [2] Galup Montoro, C.; Schneider, M.C.; Loss, I.J.B. "Series-Parallel Association of FET's for High Gain and High Frequency Applications", *IEEE Journal of Solid-State Circuits*, v.29, n.9, Sept. 1994, p.1094-1101.
- [3] Ricc6, B. "Effects of Channel Geometries on FET Output Conductance in Saturation", *IEEE Electron Device Letters*, vol. EDL-5, Sept. 1984, p. 353-356.
- [4] Mikoshiba, H. $1/f$ Noise in n-Channel Silicon-Gate MOS transistors, *IEEE Transaction Electron Devices*, Vol. ED-29, June 1982, p.965-970.
- [5] Bertails, J. C. Low-Frequency Noise Considerations for MOS Amplifiers Design, *IEEE Journal of Solid-State Circuits*, Vol. SC-14, No. 4, Aug. 1979, p.773-776.
- [6] Choi, J. H.; Bampi S. Design of CMOS OTA Amplifiers and Oscillators in a Digital Sea-of-Transistors Array. In: *5th IEEE International Conference on Electronics, Circuits and Systems*, ICECS'98. Lisboa, Portugal, 9-10/Sept/1998, p.321-324.
- [7] Choi, J. H.; Bampi, S. "Trapezoidal Association of Transistors for Mixed Analog-Digital Circuits Design on a SOT Array". In: *IEEE International Workshop on Design of Mixed-Mode Circuits and Systems, III (Proceedings)*. Puerto Vallarta, July 1999, p.65-68.
- [8] Choi, J. H.; Bampi, S. "Conductances and Noise in Trapezoidal Association of Transistors for Analog Applications Using SOT Methodology". In: *Symposium on Integrated Circuits and Systems Design, SBCCI. Proceedings...* Natal, Brazil, Sept. 1999, p.22-25.
- [9] ENZ, C. High Precision Micropower Design, Ph.D. thesis, 1989, 198p.
- [10] ENZ, C. The EKV Model: a MOST Model Dedicated to Low-Current and Low-Voltage Analogue Circuit Design and Simulation, *Low-power HF microelectronics: a unified approach*, 1996, p.247-299.