High Current, Low Voltage Current Mirrors and Applications

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Abstract. An improved current mirror structure suitable for low voltage analog applications is proposed which has high output impedance (≈5 MΩ), high bandwidth (≈400 MHz), low input (<0.4 V) and output compliance voltages (<0.5 V) and high output current capability (≈500 μA). These properties enhance the utility of this type of current mirrors. Applications of these current mirrors in analog circuits are also presented to demonstrate their superiority over their conventional counterpart. PSpice simulations confirm the suitability of the mirror for low voltage analog applications.

Key words: Analog VLSI, current mode analog signal processing, current conveyors, transconductors, current mirrors.

1. INTRODUCTION

Low voltage CMOS analog circuit structures are well established now. The requirement for such circuits stems from the requirements of high circuit density required to incorporate both analog and digital systems on a single chip. Hence, for mixed mode and complex circuit structures, smaller size devices are necessary. The device sizes are shrinking at a fast rate [1] and the threshold voltage of the MOSFET devices cannot be reduced below a certain minimum value. This necessitates investigation into new circuits using high

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threshold voltage MOS devices, which can operate at low voltages without sacrificing the circuit performance.

In analog circuits, a current mirror (CM) is an essential subsystem block. The overall performance of the analog circuit is dependent on the characteristics of the CM. This has generated the need for design of low voltage (LV) CM with low input and output voltage operation. Almost all-high swing CMs, which have been reported [2-4] so far, suffers due to the requirements of high voltage at the input end. Some LVCMs have been reported, which require low input voltages [5-7] for their operation. However, these CM structures possess poor frequency response (<100MHz) along with lower input current range (<100 μA). The demerits of these CMs make them unsuitable for use in low voltage high frequency analog and mixed mode signal processing applications such as current conveyors, operational floating amplifiers etc.

In this paper, we propose a LVCM circuit structure based on popular tail current enhancement technique [8,9]. This circuit has capability to operate at lower input voltages (<0.5V). The proposed LVCM circuit has been obtained through suitable modifications incorporated in the circuit of [8,9] by using a level shifter [5,7] at their input port. It is possible to obtain composite current outputs (i.e., positive and negative current simultaneously) by suitable modifications in output structure of LVCM. LVCMs, with composite current outputs are normally used in current mode analog signals processing circuits. The operating current range of the modified circuit extends from 1 μA to 500 μA with low input (<0.4 V) and output (<0.5 V) compliance voltages. The proposed LVCMs can operate up to a frequency of 400 MHz for negative output currents. However, for the positive output current the frequency response is in the range of 200 MHz. The proposed LVCM has been used to obtain class A current conveyor (CC) and voltage to current (V-I) converters.

2. PROPOSED LV CURRENT MIRRORS

2.1 CM Structure

The proposed LVCM circuit structure is shown in Fig. 1. At the input port a PMOS transistor M9 is used to shift the level of gate bias voltage required to operate the input transistor M2 in linear (triode) region. Injection of the input current I_{in} into the drain of transistor M2 causes a voltage (v_{in}), at its drain which is known as the input compliance voltage. The voltage shifter transistor M9 is designed to operate in saturation region for which an

appropriate amount of the bias current is required to flow. The selection of this bias current depends over the compromise reached between the offset current and v_{in}. Input bias current is obtained from an inverted current mirror formed by M15, M16, and M17. To enhance the output impedance of the current source, a cascode structure of MOSFETs, is built using M1 and M5 at the output.

Though the cascode structure at the output port enhances the output impedance, it affects the available output signal (voltage) swing. The required gate bias for M5 is achieved through another voltage shifter PMOS (M8). A CM formed by M14, M16, and M17 provides biasing current for M8. In this configuration, the output impedance R_{out} of the transistor M1 is enhanced and is given as [8]

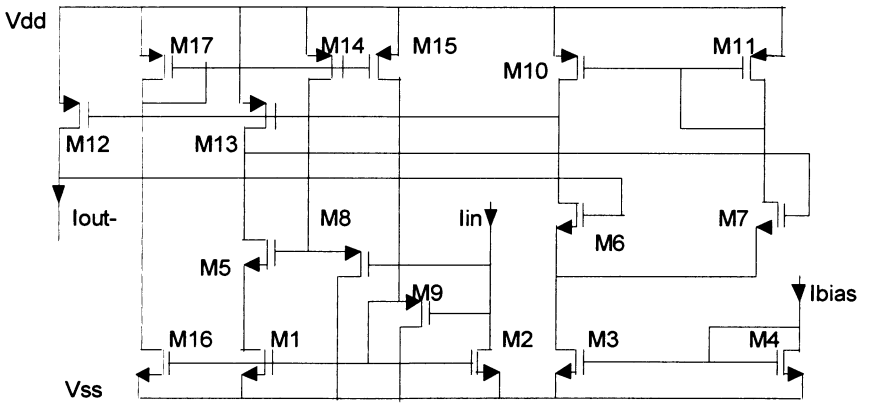

Figure 1. Proposed LV current mirror

$$R_{out} \approx - g_{m5}/g_{d1}\,g_{d5} \tag{1}$$

If g_{d1} and g_{m1} are the output conductance and trans-conductance of M2 respectively, the input impedance R_{in} and v_{in} will be given by

$$R_{in} \cup \frac{1}{g_{m1} + g_{d1}} \tag{2}$$

$$v_{in} \cup \Delta V_T + \sqrt{\Delta V_T^2 + \frac{2I_{in}}{\beta_{n2}}} \tag{3}$$

where $\Delta V_T = V_{TP} - V_{TN}$, V_{TP} and V_{TN} are the threshold voltages for M9 and M2.

Due to mismatch in the threshold voltages of the NMOS and PMOS transistors which are used in the input/output circuits and level shifter; there is an output current known as offset current (I_{offset}) for zero input current. The offset current for the circuit of Fig. 1 is given by

$$I_{offset} \cup \frac{\beta_{n2}}{2}\left[X + \Delta V_T^2 + 2\Delta V_T \sqrt{X}\right] \tag{4}$$

where,

$$X = \sqrt{\frac{2I_{bias1}}{\beta_{p9}}}$$

If $\Delta V_T^2 >> (X+2\Delta V_T\sqrt{X})$, I_{offset} can not be decreased below a certain minimum level ($\approx\beta_{n2}(\Delta V_T)^2/2$). The offset current is highly dependent on the mismatch ΔV_T between the threshold voltages of the input/output NMOS and level shifter PMOS. Smaller the mismatch, lower will be the offset current. However, if V_{TN} and V_{TP} can be matched, then I_{offset} can be reduced quite a bit. Thus, I_{offset} sets the lower limit of operating currents available from these current mirrors.

2.2 Composite Current Mirror

The composite current mirror (CCM) is required in many analog subsystem blocks where both positive and negative currents are needed. CCM can be derived from Fig. 1 by adding transistors M18 and M19 at the output ports as is shown in Fig. 2. M19, which is used in cascode mode, enhances the required output impedance for the positive current output. The gates of M18 and M19 are connected to the sources of transistor M9 and M8 respectively. Thus the additional transistors are not required to provide the required biases to M18 and M19. The input and output resistance remains same as that of LVCM. However, R_{out} for the positive current output is given as:

$$R_{out} \cup \frac{g_{m19}}{g_{d1}g_{d19}} \tag{5}$$

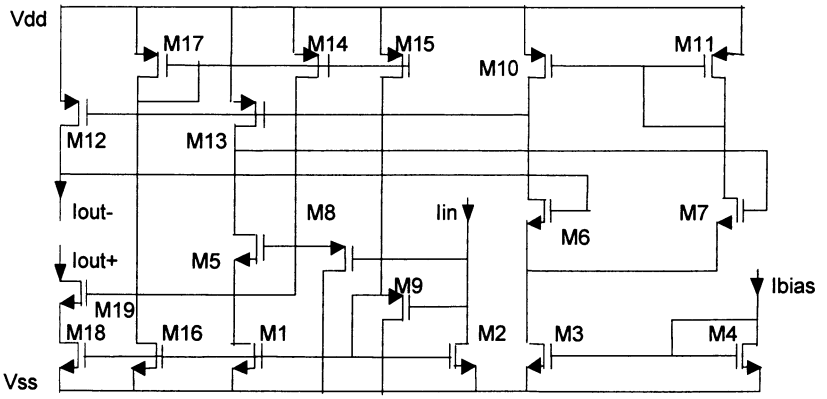

Figure 2. Proposed composite output current mirror

3. CIRCUIT ANALYSIS

3.1 CM Modeling

We have used hybrid (h) parameters to model the CM [10] and to analyse the circuit behaviour. Small signal analysis carried out for the circuit operation at low voltages gives the following expressions for the various low frequency hybrid parameters:

$$h_{11} \cup \frac{g_{dp9}}{g_{m2} + g_{dp9}} \tag{6}$$

$$h_{12} \cup 0.0 \tag{7}$$

$$h_{21} \cup \frac{g_{mn1}}{g_{m2}} \tag{8}$$

$$h_{22} \cup 0.0 \tag{9}$$

3.2 Frequency Response

Current transfer ratio from output to the input port is an important parameter for evaluation of the performance of LVCM. The frequency response characteristics in terms of output current I_{out} to I_{in} of the proposed CM is given as:

$$\frac{I_{out}(s)}{I_{in}(s)} \cup \frac{1+\dfrac{sC_{gdpo}}{g_{mpo}}}{1+\dfrac{s(2C_X+C_{gdpo})}{g_{mpo}}} H(s) \tag{10}$$

where C_{gdpo}, and g_{mpo}, represent the gate to drain capacitance and transconductance for M12 or M13 respectively. C_x and $H(s)$ are representing the stray capacitance associated at the gate of M7 and the current transfer function for the input circuit formed by M1, M2, M3, M8 and M9. Generally $H(s)$ is frequency independent and taking it to be unity, equation (10) reduces to:

$$\frac{I_{out}(s)}{I_{in}(s)} \cup \frac{1+\dfrac{sC_{gdpo}}{g_{mpo}}}{1+\dfrac{s(2C_X+C_{gdpo})}{g_{mpo}}} \tag{11}$$

As can be seen from the equation (11), the stray capacitance (C_x) severely degrades the high frequency response for the proposed LVCM.

3.3 Sensitivity Analysis

Sensitivity is one of the most important criteria used for comparing the circuit performance. We shall evaluate the sensitivity of the output current over the circuit parameters such as device dimensions and circuit structure. The sensitivity of the output current with respect to I_{bias1} and ΔV_T is given as:

$$S_{I_{bias1}}^{I_{OUT}} \cup \frac{\beta_{n1}}{2ST_{I_{bias1}}^{I_{OUT}}} \tag{12}$$

$$S_{\Delta V_T}^{I_{OUT}} \cup \frac{2\beta_{n1}\Delta V_T}{ST_{\Delta V_T}^{I_{OUT}}} \tag{13}$$

where the stability factors are represented as:

$$ST_{I_{bias}}^{I_{OUT}} \cup \frac{\beta_{n1}\overline{v_{in}+\sqrt{\dfrac{2I_{bias}}{\beta_{p5}}}+\Delta V_T}\sqrt{}}{\sqrt{2I_{bias}\beta_{P5}}} \tag{14}$$

and,

$$ST_{\Delta V_T}^{I_{OUT}} \cup \beta_{n1} \overline{v_{in}} + \sqrt{\frac{2I_{bias}}{\beta_{P5}}} + \Delta V_T \sqrt{} \quad (15)$$

As can be seen from the above expressions that the stability factors are quite high ($>10^3$) for the proposed circuit structures. This in turn results in low sensitivity ($<10^{-5}$) of the output current to the variations of the circuit (β_n and β_p) and device parameters (ΔV_T).

3.4 Simulation Results

The proposed LVCM circuits of Fig. 1 and Fig. 2 have been simulated using the PSPICE circuit simulator. The device parameters for 1.2 μm CMOS technology [11] have been assumed. The device dimensions taken for the simulation are given in Table 1.

We are primarily interested in R_{in}, R_{out}, v_{in}, and the frequency response of LVCM. For the proposed structure R_{in} is equal to 700 Ω (quite low value for any CMOS structure). R_{out} is calculated to be 5 MΩ for an input (output) current of 500 μA, which is sufficiently higher than that of a single transistor CM structure. Fig. 3 shows the I_{out} versus the voltage present at the drain of M12 characteristics for various values of I_{in} for the proposed LVCM.

Table 1. Device dimensions

Device	Device type	Aspect ratio (W/L)
M1, M2, M5, M16, M18, M19	NMOS	240 μm/2.4 μm
M3, M4, M6, M7	NMOS	60 μm/2.4 μm
M8, M9, M12, M13	PMOS	120 μm/1.2 μm
M10, M11	PMOS	240 μm/2.4 μm
M14, M17	PMOS	240 μm/1.2 μm
M15	PMOS	1.2 μm/120 μm

LVCM needs a voltage margin of less than 0.5 V at both ends of the power supply for an input current swing up to 500 μA. However, an input swing of 1.5 V for supply voltage of 2.0 V and for I_{in} < 250 μA can be achieved.

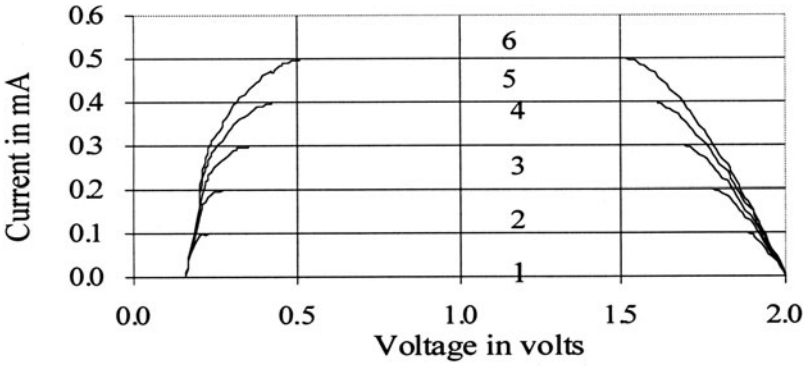

Figure 3. Output current versus the voltage present at the drain of M12 characteristics for various values of I_{in}
(1--0.0 mA, 2--0.1 mA, 3--0.2 mA, 4--0.3 mA, 5--0.4 mA, 6--0.5 mA)

The input voltage (v_{in}) characteristics are depicted in Fig. 4. The input voltage suddenly rises to a required voltage of 0.2 V as I_{in} is pumped in to the CM. Then it rises with the rise in the input current and still remains fairly low (<0.4 V) for the entire current range from 1 μA to 500 μA. The input compliance voltage for the conventional CM of [8] is also plotted in Fig. 4 for comparison. A clear gain of about 0.8 V in the input compliance voltage is visible.

Frequency response for the proposed LVCM and conventional CM of [8], are shown in Fig. 5. The proposed CM can operate up to 400 MHz while the conventional CM without the proposed modifications has a bandwidth of 270 MHz for same device parameters. The bandwidth enhancement due to the proposed modifications is explained in reference 12 and 13 in detail. The superiority of the proposed LVCM in terms of frequency response is evident from the figure. The peak present in the output is due to the pole shifting toward origin because of the stray capacitance C_x.

4. LVCM APPLICATIONS

The proposed LVCM can find use in low voltage analog signal processing circuits. We examine applications of LVCM in current conveyors and in linear trans-conductors.

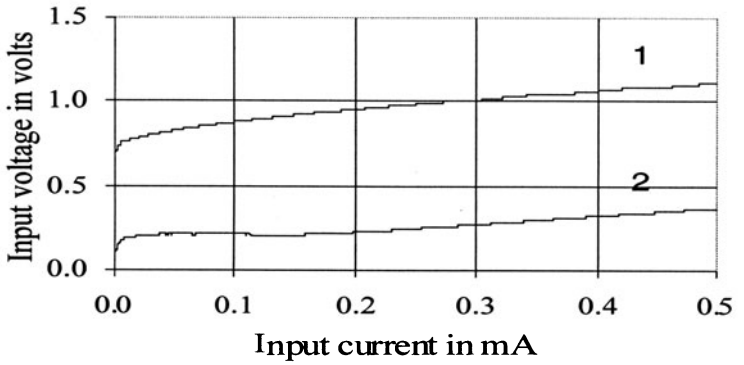

Figure 4. Input voltage characteristics
(1 - Conventional mirror [8] and 2 - Proposed LV CM)

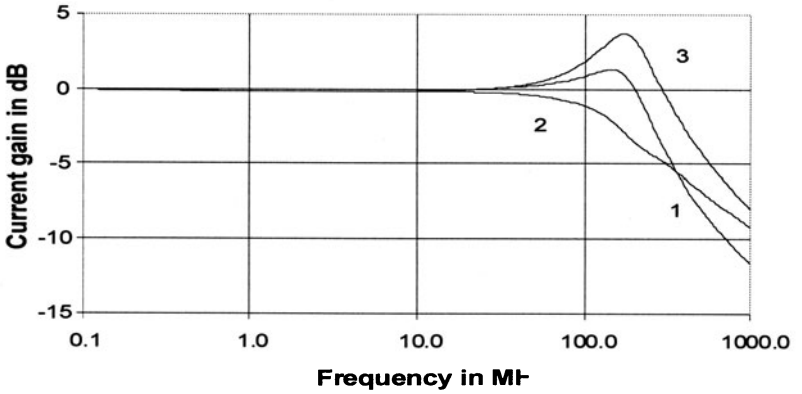

Figure 5. Simulated frequency response characteristics
(1—Conventional CM [8], 2—Proposed LVCM for positive current output and 3--- for negative current output).

4.1 Current Conveyor II

LVCM discussed in the previous section has been used for the design of a class A CMOS current conveyor III (CCIII) of the type discussed in [14, 15]. For rail to rail operation of this type of CCIIIs, low input voltage CMs are necessary.

4.1.1 Circuit Implementation

The circuit diagram of a proposed CCIII is shown in Fig. 6. The voltage transfer from port Y to port X takes place as the LVCM1 forces the equal current to flow through M1 and M2. When the aspect ratio (W/L) of the transistor are kept to ensure $\beta_{n1}=\beta_{p2}$, the drop across gate source terminals of M1 and M2 will be equal, which in turn transfer the voltage applied at the drain of M1 to the source terminal of M2. Current transfer from port X to port Y is achieved through the action of LVCM1 and LVCM2.

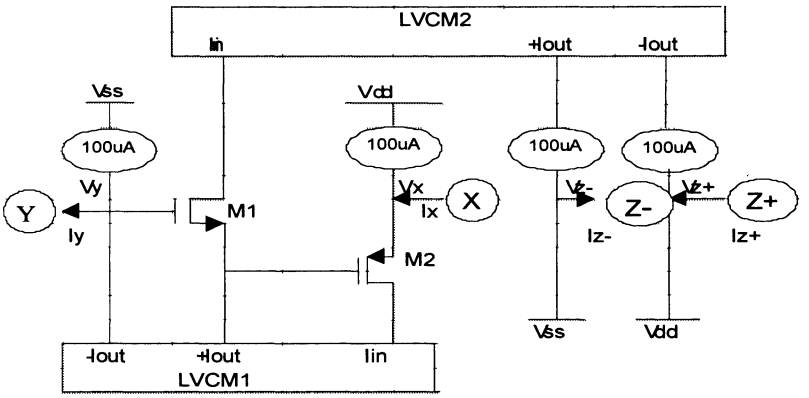

Figure 6. Proposed CCIII structure.

As evident from the figure the input signal can swing rail to rail for the positive inputs however, for negative voltages the input voltage swing is restricted to:

$$v_{in} \cup V_{SS} - V_T - V_{CM} \tag{16}$$

When V_{CM} is very low as in the case of proposed LVCM, the swing range increases approximately by 0.8V (the difference in the input voltage of proposed and conventional CMs).

4.1.2 Simulation Results

P-Spice simulations were carried out for CCIII structure. The aspect ratio for transistor M1 and M2 were taken to be 60 μm/1.2 μm and 240 μm/1.2 μm for NMOS and PMOS transistors respectively. The bias voltages are taken to be ±1.0 V. The output characteristics for the input current swing are

shown in Fig. 7. The maximum input current is ±100 μA. The voltage developed at the X terminal due to injected current is 100 mV.

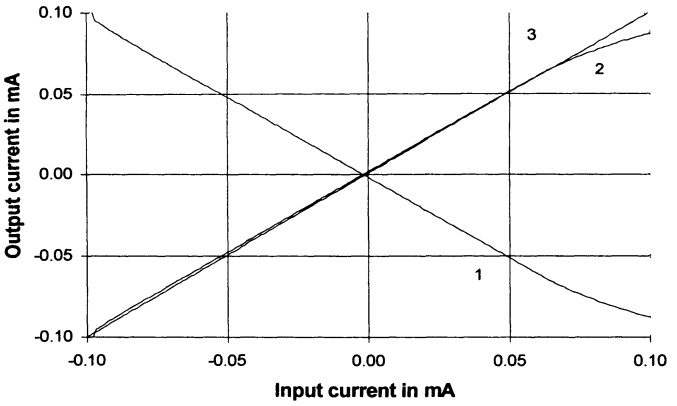

Figure 7. DC input output characteristics of the proposed CCIII (1---I_{Z+} , 2---I_{Z-}, 3---I_Y)

For the frequency response characteristics of the proposed CCIII, an ac current is injected at the input port X, and the resultant current in the Z + and Z- terminals are recorded and presented. The frequency response characteristics are given in Fig. 8. The power consumption is 2.7 mW and the circuit has 20 MHz bandwidth.

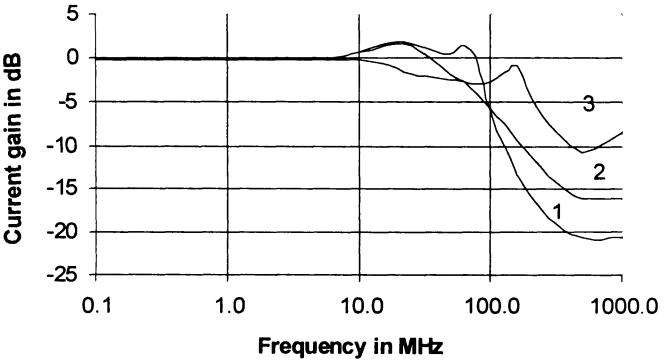

Figure 8. Frequency response of CCIII (1---Positive output current, 2---negative output current, 3---Current required at port Y).

4.2 Linear Voltage to Current Converter

Voltage to current (V-I) converters are known as trans-conductors which find many uses in signal processing circuits like analog filters. High linearity, low noise, large trans-conductance and low power dissipation are the few important parameters required for a high frequency trans-conductors The proposed LVCM is used to construct a linear trans-conductor.

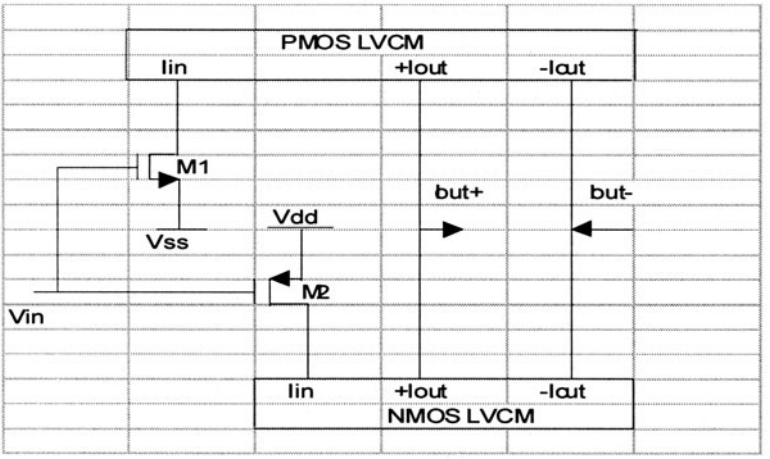

Figure 9. Proposed trans-conductor structure

4.2.1 Circuit Implementation

The circuit structure adapted for the realization of the trans-conductor is shown in Fig. 9. It is assumed that the transistor M1 and M2 operate in saturation, the currents flowing into the input transistors M1 and M2 are given by

$$i_{D1} \cup \frac{\beta_{n1}}{2}(V_{in1} - V_{TN})^2 \tag{17}$$

$$i_{D2} \cup \frac{\beta_{p2}}{2}(V_{in2} - V_{TP})^2 \tag{18}$$

Assuming $\beta_{n1} = \beta_{p2} = \beta$, $V_{in1} = V_{in}\text{-}V_{ss}$, $V_{in2} = V_{in}\text{-}V_{dd}$ and $V_{dd} = -V_{ss}$, the current at the output can be given as:

$$i_C = i_{D1} - i_{D2} \tag{19}$$

$$\cup 2\beta V_{dd}(V_{in} - V_{TN}) \tag{20}$$

Examination of the above equation yields that the trans-conductor will show a linear characteristic and the trans-conductance can be varied by suitably chosen values of β and/or supply voltages.

4.2.2 Simulation Results

For PSpice simulations of above trans-conductor, the aspect ratio for transistor M1 and M2 were taken to be 7.2 μm/2.4 μm and 30.6 μm/2.4 μm for NMOS and PMOS transistors respectively. The substrate contacts of these MOSFETs are assumed to be connected to the most positive terminal for the PMOS and the most negative terminal for the NMOS respectively and the supply voltages of ±1.0 V are taken for all simulations.

Output current versus input voltage characteristics of the circuit is depicted in Fig. 10 in which its rail to rail input voltage swing capability is evident. The trans-conductor consumes 0.6 mW power.

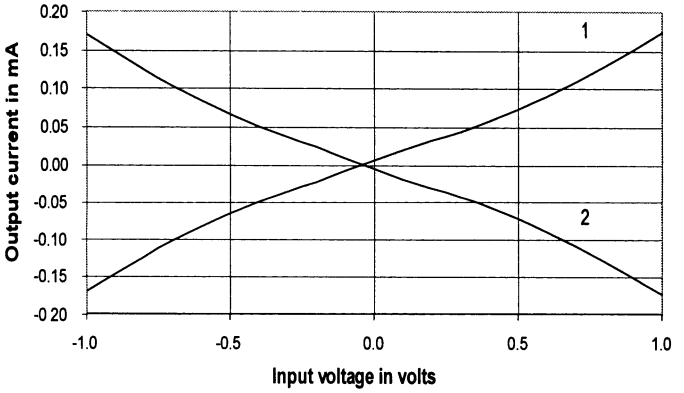

Figure 10. V-I conversion characteristics (1—I_{out+} and 2---I_{out-})

5. CONCLUSIONS

We have presented a modified low voltage, current mirror structure, capable of giving high input and output voltage swings. The operating current range of the LVCM extends from 1 μA to 500 μA with a bandwidth as high as 200 MHz. The input voltage requirement is also quite small (<0.4 V). The usefulness of the proposed LVCM over its conventional part of [8] makes it an attractive candidate for low voltage analog design.

The superiority of these LVCMs when used in the current conveyor structures and linear trans-conductor structures is also significant. The resultant CCIII and trans-conductor structures consume very low power and

can operate at sufficiently low voltages present at the input port. Thus the proposed LVCM can be used for low voltage, analog circuit applications.

6. ACKNOWLEDGEMENT

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