Substrate Noise: Analysis, Models, and Optimization

Edoardo Charbon

Cadence Design Systems, San Jose, CA 95134

charbon@cadence.com

Joel Phillips

Cadence Berkeley Laboratories, Berkeley, CA 94704

jrp@cadence.com

Abstract In this paper we address the main problems posed by substrate noise from two complementary points of view. We look at the effects of substrate noise on performance and reliability in digital, analog and mixed-signal circuits. The mechanisms underlying noise generation, injection, and transport are also analyzed. Solutions to the substrate noise problem using design and layout techniques, as well as accurate analysis and optimization are discussed.

Keywords: Substrate, Optimization, Scaling, Parasitic Extraction, Green's function, Fast Cosine Transform

1. INTRODUCTION

In the past decade, substrate noise has had a constant and significant impact in the design of analog and mixed-signal integrated circuits. Only recently, with the advances in chip miniaturization and innovative circuit design, substrate noise has begun to plague fully digital circuits as well. To combat the effects of substrate noise, heavily over-designed structures are generally adopted, thus seriously limiting the advantages of innovative technologies. For this reason, the modeling of substrate noise is receiving serious attention. Macro-models mimicking substrate noise sources and better simulation of transport mechanisms have been

The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: [10.1007/978-0-387-35498-9_57](https://doi.org/10.1007/978-0-387-35498-9_57)

L. M. Silveira et al. (eds.), *VLSI: Systems on a Chip*

© IFIP International Federation for Information Processing 2000

developed, thus allowing designers to detect potential problems before fabrication. Specific guidelines have also been drafted for more aggressive, substrate-aware design practices.

Accurately characterizing substrate noise is problematic for various reasons. The noise results from superposition of a large number of local and remote sources, each attenuated and delayed in a unique way. Modeling signal attenuation and delay individually may be extremely time consuming and would require accurate *ad hoc* characterization of all the sources, which is in itself a hard problem. Substrate noise can be decomposed, at a macroscopic level, in intrinsic and switching noise. Intrinsic noise is a background spurious signal originated in active and passive devices through various physical phenomena, namely thermal, shot and flicker noise. Switching noise originates in digital blocks where frequent state transitions, occurring in gates across the chip, cause current pulses to be absorbed from and transmitted to power and ground buses through direct feedthrough and the charge/discharge of loads. Such pulsing currents are partially injected into the substrate through impact ionization and capacitive coupling.

Switching noise coupled through the substrate is very destructive as it can be broadcasted over great distances and picked up by sensitive circuits, by way of capacitive coupling and body effect. The resulting threshold voltage modulation dynamically changes gate delays locally, thus impacting performance in ways that are difficult to predict. Switching noise has an especially detrimental effect on dynamic logic, memories and embedded analog circuits, such as phase lock loops.

Accurate estimation of substrate noise requires several techniques to model switching noise injection, transport, and reception mechanisms, both at the microscopic and macroscopic level. Moreover, means are necessary to embed substrate noise in optimization loops and trend analysis tools. This is critical to help designers detect substrate related problems as early as possible, tailoring design practices, in order to avoid lengthy redesign cycles.

The paper is organized as follows. In Section 2. the physical mechanisms underlying substrate noise generation, transport and absorption are outlined. Section 3. reviews several substrate noise analysis techniques, while Section 4. presents substrate-aware optimization methods applied to physical design problems.

Figure 1 Substrate cross-section of a CMOS inverter

2. NOISE COUPLING MECHANISMS

2.1 Noise Injection and Reception

Substrate noise is caused mainly by the switching activity of fast digital circuits and it is injected into the substrate via *impact ionization* and *capacitive coupling* mechanisms. Figure 1 shows a typical cross-section of substrate epitaxial layer on which a CMOS inverter is integrated. Impact ionization is caused by electron-hole pairs generated in the pinch-off region, when the electric field exceeds a given threshold. The excess holes are collected in the region of substrate under the device and from there they are transported throughout the chip. Impact ionization currents are evaluated as

$$I_{\text{impact}} = \int_{E_s}^{E_m} I_d A e^{-B/E(x)} dx. \quad (1.1)$$

where E_s , E_m , $E(x)$ and I_d are source electric field, maximum electric field, local electric field and drain current, respectively. Constants A and B are material related coefficients. Formulae relating these parameters to measurable quantities and the derivation of (1.1) can be found in [1]. Since $E_m \gg E_s$, integral (1.1) can be approximated to

$$I_{\text{impact}} \simeq \frac{A}{B} l E_m I_d e^{-B/E_m} = C_1 (V_{ds} - V_{dsat}) I_d e^{-\frac{C_2}{(V_{ds} - V_{dsat})}}, \quad (1.2)$$

where l , V_{ds} and V_{dsat} are effective channel length, drain-source voltage and saturation voltage, respectively. C_1 and C_2 are material related coefficients [1]. Equation (1.2) is used by most MOSFET models to represent impact ionization currents [2].

Switching noise can also be coupled into substrate capacitively through reverse biased junctions and metal-to-diffusion capacitances. All spurious currents injected into the substrate travel through the bulk reaching varying depths and resurfacing to be collected by low-resistivity pick-ups.

Figure 2 Current flow of substrate noise through low-resistivity substrate with different injector/receptor configurations, assuming grounded backplate

The paths followed by such currents are determined by the relative position of the injector, the pick-up and the other contacts in the circuit, the substrate doping profile, and the backplate potential. Figure 2 shows substrate current flow lines for the case of (a) distant and (b) close injector/receptor systems in a typical high-resistivity substrate. In the whole spectrum of silicon substrates available today, one can recognize two main types: one referred to as *high-resistivity* and the other as *low-resistivity* substrate. In general, the first substrate type is composed of a uniformly doped layer with a resistivity coefficient of $20 - 50 \Omega\text{cm}$. The second type consists of a thick, high-resistivity epitaxial layer ($d \simeq 10\mu\text{m}$, $\rho \simeq 10 - 15 \Omega\text{cm}$) and a low-resistivity bulk ($\rho \simeq 1\text{m} \Omega\text{cm}$). Low-resistivity substrates are generally preferred for their good latch-up suppression properties [1]. High-resistivity ones on the contrary, are better suited to block substrate noise by using guard rings and physical circuit separation. At low and medium frequencies, typically less than 5 GHz, all substrates show a resistive behavior.

Let us consider as an example the CMOS inverter from Figure 1, which we assume has been integrated into a high-resistivity substrate. The plot in Figure 3 shows the input waveform and the resulting injected signals for both High-to-Low and Low-to-High transitions and various slow rates at the input (note the different time scale in the various waveforms). The plot was obtained from SPICE simulations using

Figure 3 Noise spikes injected into substrate via impact ionization and capacitive coupling ($0.8\mu\text{m}$ and $0.6\mu\text{m}$ CMOS technologies). The waveforms shown were obtained with input waveforms of varying slew rates: note the different time scales of $2\mu\text{sec}$, 200 nsec , 20 nsec , and 2 nsec , while the input waveform is scaled accordingly

custom-fitted device models. Assuming that switching is synchronized with a clock signal, it can be shown that the power has energy components located in a wide spectrum, not necessarily centered at the clock frequency. A significant portion of this energy is usually concentrated around special frequency bands, e.g. at the inverse of the average gate delay. At DC or near DC frequencies, one also observes large spurious currents. This is due to the fact that impact ionization, for its very nature, only generates positive currents. Higher frequency components are due to glitches and fast switching phenomena occurring in large circuits [3].

Impact ionization has the following features: (a) the instant in which the maximum of the waveform is reached depends on the rising and

Figure 4 Normalized substrate noise spectrum of C6288 in dB vs. GHz

falling time of the input signal; (b) the duration of the pulse depends on the rising and falling time of the input signal; Impact ionization pulses have approximately the same shape in all shown frequencies while only their duration is different (again note the different time scales in Figure 3). Capacitive coupling (drain-substrate and source-substrate reverse-biased junctions) dominates for rising/falling times of less than 10ns .

In a typical logic circuit of several thousands gates, the effect of switching activity and glitches result in a cumulative injected noise, whose power spectrum represents a significant portion of the total energy absorbed by the circuit. As an illustration consider the MCN91 benchmark C6288. The circuit's spectrum, computed using SUBWAVE[3], is shown in Figure 4. One can recognize the DC, inverse delay and high frequency components. Notably, at the clock frequency, the spectrum is relatively flat. If a circuit with such a large spectrum of injected noise is integrated near sensitive components, then the noise present at the substrate's surface throughout the chip will be unevenly distributed.

2.2 Delay Effects

So far we have outlined the effects of substrate noise coupling on mixed-signal circuit performance. Digital circuits are not immune from substrate noise. The noise is injected by logic gates during switching and glitch transients through impact ionization and capacitive coupling, and it is picked up by active devices via capacitive coupling and body effect. As a result the delay of the datapath may increase, thus possibly exceeding the predefined clock period. Such behavior is known as *delay effect*.

Figure 5 Analogy between interconnect cross-talk and substrate capacitive coupling

Gate delay $t_{50\%}$ is a function of several factors, including fanout, supply voltage, transistor geometry, input waveform, and charge excess caused by charge sharing effects. Ignoring the loading due to interconnect wiring, the gate delay is usually approximated by [4]

$$t_{50\%} = R_{EFF} \times C_G,$$

where $C_G = C_{OX}WL$ is the gate capacitance. R_{EFF} , the effective resistance, is the average transistor resistance during the output voltage swing and is proportional to R_{tr} . with

$$R_{tr} = \frac{L/W}{\mu C_{OX}(V_{DD} - V_T)},$$

where L and W are the dimensions of the transistor, V_{DD} the supply voltage, C_{OX} the gate oxide capacitance, and V_T the threshold voltage. V_T is in turn proportional to the square root of the voltage V_{sb} applied between its substrate contact and the source. Hence,

$$t_{50\%} \propto \frac{1}{\sqrt{V_{sb}}}.$$

The second main contribution to parasitic gate delay is due to capacitive coupling. The analysis of this effect is essentially identical to that of cross-talk between interconnect lines. In this case the aggressor is the substrate underneath the victim interconnect line or device. Figure 5 shows the coupling model equivalence, with coupling capacitances $C_c = C_s$. Resistor R_1 represents the impedance which holds the victim node at ground potential. Using standard analytic charge coupling models [4] one can estimate the charge noise present in the interconnect line due to substrate noise. Figure 6 shows the model proposed for a typical cross-coupling system. A close form analytic model for the response voltage to charge injection $v_1(t)$ was derived in [4]. The voltage at the

Figure 6 Standard cross-coupling model

peak and the instant at which it occurs are respectively

$$t_p = \begin{cases} \tau_1 & \text{if } \tau_1 = \tau_2 \\ \frac{\tau_2 \tau_1}{\tau_2 - \tau_1} \ln\left(\frac{\tau_1}{\tau_2}\right) & \text{otherwise,} \end{cases} \quad v_1(t_p) = \begin{cases} \frac{C_c}{C_1 + C_c} e^{-1} & \text{if } \tau_1 = \tau_2 \\ \frac{C_c}{C_1 + C_c} \left(\frac{\tau_1}{\tau_2}\right)^{\frac{\tau_1}{\tau_2 - \tau_1}} & \text{otherwise,} \end{cases}$$

where $\tau_1 = (R_1 || R_2)(C_1 + C_c)$ and the waveform of the aggressor node is assumed to be a decaying exponential step with time constant τ_2 . From charge noise one can derive the extra delay present on a gate [4].

Empirical delay models based on cross-talk have been proposed in the literature. One such model, relating the length of the parallel running wire l and the average spacing s to the extra delay $\Delta\tau$, was proposed in [5]. The model computes $\Delta\tau$ as

$$\Delta\tau = \frac{\alpha l^m}{s^n},$$

where α is a fitting constant, while m and n are empirically observed to be near 2 and 1, respectively.

3. SUBSTRATE ANALYSIS

The goal of substrate analysis is to obtain a compact representation of the interactions of circuit elements that couple through the substrate. An equivalent circuit, or some other model that represents the (possibly frequency-dependent) impedance or admittance matrix describing substrate coupling must be obtained in order to include the substrate effects in circuit simulation or optimization. One approach is to perform experiments on a small number of contacts [6] and fit an empirical model to the results. The other is to address the differential equations that describe substrate transport in a numerical or semi-analytical manner [7, 8, 9, 10, 11].

The basic relation describing substrate transport is the continuity equation

$$\nabla \cdot (\sigma \nabla \Phi(x, y, z, t)) + \frac{\partial}{\partial t} (\nabla \cdot (\epsilon \nabla \Phi(x, y, z, t))) = 0, \quad (1.3)$$

where ϵ and σ are respectively the local dielectric permittivity and conductivity of the substrate. ϵ and σ are potentially spatially varying due to the substrate layer structure, device and well implants, and the presence of other integrated components. If the dielectric relaxation time, $\tau_e = \epsilon/\sigma$, is much smaller than any time-scale of interest, then the second term in Equation (1.3) may be neglected and the substrate treated as purely resistive. A complex conductivity $\sigma' = \sigma + j\omega\epsilon$ may be used to model dynamic effects without change to the basic analysis procedure, though model extraction is complicated since either an equivalent circuit must be fit to data obtained by solving the differential equation at several points in the frequency domain[12, 13] or a model reduction procedure[14, 15, 16] performed.

In uniform material, Equation (1.3) reduces to the Laplace equation

$$\nabla^2\Phi = 0. \quad (1.4)$$

Boundary conditions come from contacts, usually considered equipotential; edges, where zero-normal-current (Neumann) conditions hold; or material interfaces, where the current $\mathbf{J} = \sigma\nabla\Phi$ must be continuous, leading to the boundary condition $\sigma_+\partial\Phi/\partial n|_+ = \sigma_-\partial\Phi/\partial n|_-$ where $\partial\Phi/\partial n$ refers to the normal derivative, and σ_+, σ_- refer to conductivity on opposite sides of the interface. To extract a column of the impedance matrix corresponding to a specific contact, the potential of that contact is set to a single volt. The currents flowing into each of the other contacts, computed from integrating the normal derivative of the potential over each contact's surface, give the relevant mutual admittances. Solution of the equations governing the substrate requires sophisticated techniques, but, fortunately, the solution of the Laplace equation is one of the most well-studied problems in the applied mathematics literature.

Methods based on differential formulations of the Laplace equation can easily analyze substrates with spatially-varying resistivities. Finite difference[17] or finite element[18] techniques are usually used to discretize Equation (1.3). These methods convert the Laplace equation into a set of sparse algebraic equations, for example by replacing the derivatives of Φ by differences such as

$$\frac{\partial^2\Phi}{\partial^2x} = \frac{\Phi_{i+1,j,k} - \Phi_{i-1,j,k} - 2\Phi_{i,j,k}}{\Delta_i^2}, \quad (1.5)$$

where Δ_i is the x -directed grid spacing at the grid point indexed by $\{i, j, k\}$. These equations may be solved by standard sparse linear system [19] solution techniques based on Gaussian elimination but due to the large degree of matrix fill that occurs during the factorization of a matrix that derives from a three-dimensional mesh, iterative solution algorithms

often provide better performance in considerably less memory. Modern iterative schemes are usually Krylov-subspace [20] algorithms such as the conjugate-gradient or GMRES methods. For the discretization of elliptic differential equations, preconditioning is required to achieve convergence in a reasonable number of iterations. Incomplete factorization[21, 20] preconditioners are popular, but preconditioners based on multigrid[22] or multiresolutional ideas[23] can be considerably more effective.

When the material conductivities and permittivities are relatively homogeneous (e.g., the resistivity varies along one dimension and/or is piecewise-constant with not too many regions of different conductivity), then integral equation techniques are competitive. By translating the three-dimensional partial differential equation into an integral equation over the two dimensional surfaces that bound the problem domain (usually the substrate contacts), integral equation methods reduce the number of unknown variables that must be analyzed and can provide superior performance if efficient techniques are used to solve the linear equations.

The simplest integral equation encountered in the substrate context is the first-kind equation [24, 25]

$$\Phi(\mathbf{r}) = \int_S \mathbf{G}(\mathbf{r}, \mathbf{r}') j(\mathbf{r}') d^2 \mathbf{r}' \quad (1.6)$$

that relates injected contact currents $j(\mathbf{r}')$ to known contact potentials $\Phi(\mathbf{r})$. Physically, $\mathbf{G}(\mathbf{r}, \mathbf{r}')$ represents the potential at $\mathbf{r}$ due to a point charge placed at a point $\mathbf{r}'$ and is called a Green's function. Once the Green's function is known, Equation (1.6) allows one to determine the injected currents, from which the potential and currents at any point in the substrate can be computed.

In the absence of any boundaries, that is in the free-space case, the function $\mathbf{G}(\mathbf{r}, \mathbf{r}')$ reduces to $1/(4\pi\sigma|\mathbf{r} - \mathbf{r}'|)$. In principle the free-space Green's function may be used for substrate extraction calculations, however, the boundary conditions at domain boundaries must be explicitly enforced, which implies discretizing the boundaries[26]. In the substrate analysis problem, it is more convenient to derive a Green's function tailored to the layered media boundary conditions. These Green's functions, which incorporate any effects due to vertically-varying conductivity and possibly finite extent of the substrate, simplify the numerical procedure since the integral equation only needs be written over the multiply-connected surface defined by substrate contacts that are usually in the top layer of the material. However, the Green's function can be expensive to compute. Possible methods for evaluating the Green's func-

tion include image-based techniques[27, 28, 10], separation-of-variables (SOV)[29], and spectral domain analysis[30].

In the engineering community, the numerical solution of electromagnetic integral equations is usually done via method-of-moment[31] or boundary-element techniques. The simplest such scheme is to discretize the domain of the integral (in this case, the substrate contacts) into a number of polygonal sections called panels. Given Dirichlet boundary conditions on the panels, the unknowns are the injected currents, and on each panel the injected current is assumed to be constant. The potential $\bar{\Phi}_i$ of a contact panel is defined as the result of summing over the contribution from current injected at every other panel in the domain and averaging the potential over the panel,

$$\bar{\Phi}_i = \sum_j \frac{I_j}{A_j A_i} \int_{A_i} \int_{A_j} G(\mathbf{x}, \mathbf{x}') da_j da_i = \sum_j Z_{ij} I_j \quad (1.7)$$

where the sum runs over all panels j , A_i and A_j are the areas of contacts i and j respectively, and I_j is the current injected from panel j , and the integral is over the panel surfaces. This procedure produces a matrix equation

$$\mathbf{Z}\mathbf{I} = \bar{\Phi} \quad (1.8)$$

where the matrix $\mathbf{Z}$ is *dense*, that is, every entry is non-zero because a normal current injected from any panel induces a potential at *every* other panel in the substrate.

In realistic problems, the matrix in Equation (1.8) can be quite large. Constructing and directly inverting the full $\mathbf{Z}$ matrix for the entire substrate contact configuration can be prohibitively expensive, and so more efficient methods have been sought by many authors. Physically based heuristics involving approximations to the inverse of the $\mathbf{Z}$ matrix[29, 32, 9] can accelerate the matrix solution process as well as the following nonlinear simulation. Numerical stability and error control in these procedures can be difficult to quantify.

More rigorous analysis acceleration techniques typically exploit the analytic properties of the Green's function. For problems with bounded domains, the multilayer Green's function can be computed in $\mathcal{O}(n \log n)$ time using Fast Cosine Transform (FCT) techniques. The FCT can be used to build a technology-dependent table that is used to accelerate the matrix construction procedure for one of the direct techniques. When combined with a matrix simplification procedure and low-rank update techniques[33], the overall procedure can be effective, particularly when embedded in the loop of an optimization procedure.

When direct techniques are no longer feasible, iterative matrix solution algorithms such as GMRES[34] must be used. The dominant

computational cost in such an algorithm is the computation of a matrix-vector product with the matrix $\mathbf{Z}$. The speed of the FCT can be exploited to directly compute the matrix-vector products in such an iterative procedure [35] in nearly optimal time, if the contacts may be uniformly subdivided and are fairly densely spaced. For complicated contact distributions, several algorithms have been developed that can compute a matrix-vector product in close to $O(n)$ time and memory by approximating the action of the matrix $\mathbf{Z}$.

Most of the matrix approximation algorithms are based on the fact that the potential induced by an injected current has a spatially complex profile only near the injection source. Far away from the source it can be easily approximated to within a given error. FCT and FFT related techniques can be applied by using local corrections [36, 37] that remove any constraints on the relation between the FCT/FFT grid and the underlying discretization. The authors of [38] have developed an algorithm that interpolates the Green's function in a hierarchically spatially-decomposed manner, and then uses a procedure similar to the Singular Value Decomposition to further compress the interpolation elements.

Recently algorithms have been developed that combine the matrix approximation with an acceleration of the iterative matrix solution procedure itself. The multigrid method of [39] is based on constructing a hierarchical representation of the irregular problem domain. At each level of hierarchy, a coarser representation of the discretized problem is constructed by using a geometric-moment-matching scheme to approximate the rough features of the finer geometry. The coarser grid problems can be solved relatively cheaply, so the solutions to the coarse grid problems are used to accelerate the iterative solution of the linear systems on the finer levels. The convergence of the iterative solver is extremely rapid, requiring only a few iterations to converge to engineering tolerances. A similar multiresolution approach was described in [40], where a wavelet-like basis for the panel unknowns is constructed by matching moments of the multipole field expansions. The wavelet-like basis is used to perform rapid matrix-vector products and also provides a natural, and very effective, preconditioner.

4. OPTIMIZATION AND SCALING

Optimization phases typically performed in physical design include floorplanning and placement. The algorithms used in floorplanning and placement are based on incremental improvement techniques. Due to its "global" effects felt everywhere in the chip, substrate noise cannot be easily translated into a compact analytical model accounting for the

entire substrate area. Hence, even if a small incremental modification is performed on the chip, the whole substrate analysis needs be reevaluated. The traditional approach to this problem consists of using a scheme based on finite difference methods. To reduce the time complexity of the problem the density of the mesh that mimics the substrate bulk is drastically simplified, thus resulting in an accuracy reduction [8, 41]. Another potential problem with this approaches is a strict requirement of alignment between grid and layout objects.

An alternative method is one which transforms the substrate problem into a simpler one, for example using simplified analytical models of contact-to-contact resistances[6, 42]. Moreover, the presence in the design of even relatively small analog circuits complicates the substrate noise analysis problem.

Approaches based on integral equation techniques can make better use of the locality of incremental changes. The key of such techniques is a fast computation of *variations* and *trends* of substrate transport given changes in its physical structure. An often exploited technique is based on the fact that small adjustments in the position and orientation of layout elements results in a small change in the matrix $\mathbf{Z}$. Using the Sherman-Morrison update, $\mathbf{Z}^{-1}$ can be computed in quadratic time complexity. Another method is based on the use of sensitivities to determine the effect on substrate conduction by a small change in the contact organization. Sensitivities can be computed *a priori* efficiently and allow one to obtain a relatively accurate substrate noise map after several component moves.

Re-design generally involves scaling in x- and y- directions, while technology migration involves a three-dimensional scaling. Sensitivity analysis is performed to quantify the effects of small changes in doping profiles and doping concentrations to, for example, a grid of contacts and their associated substrate resistances. Similar regular structures can be designed to test the effects of migrating to a different technology.

Improvements on the performance degradation due to substrate-induced switching noise can be achieved by placing noise injecting and noise sensitive modules at a certain distance or by creating special structures, such as low-resistivity guard-rings, around noise injectors [29]. The first provision is generally implemented in a placement tool using the conventional Simulated Annealing (SA) move-set. The second issue is usually solved by extending the search space, allowing the annealing to choose from a number of alternative implementations for a module, including one with a guard-ring implemented around it.

In order for a placer to be effective in preventing violations to performance specifications, the following features are often implemented in

the tool. (1) A model for each noise injecting module, characterizing the *waveform* and the *spatial location* where the noise is injected as precisely as possible. (2) A model of substrate transport for efficient substrate current evaluation, possibly independent of the circuit configuration. (3) A model for substrate noise absorption and its effect on performance.

The evaluation of performance degradation due to substrate noise is generally the most time consuming. In [33] for example, such problem is approached in the following way:

1. generate constraints for each node of noise-sensitive modules
2. generate the resistive network associated with substrate
3. quantify violations to constraints

The calculation of all violations in step 3 to the given constraints is carried out by solving the underlying circuit and evaluating the appropriate parameters at each critical node.

At each stage of the annealing only steps 2 and 3 need be repeated, since step 1 is carried out only once for each chip. The efficiency of a simulator based on integral equation techniques, though high, is still insufficient for such computationally intensive algorithm as SA, hence, appropriate heuristics are generally developed. In SA, at high annealing temperatures, considerable reshuffling is allowed on the components of the layout. Hence, the locations of switching noise generators and receptors can be significantly modified. On the other hand, only when changes in component location reflect a significant change in any performance measure, the entire substrate network should be evaluated along with the estimate of performance degradation. This observation is generally used to create combined heuristics for the evaluation of substrate effects after each tentative annealing move.

The placement algorithm has been proven to converge to a global minimum under the Romeo/Hajek conditions [43] when it is modified to account for noise substrate transport evaluation [44]. A tool based on this algorithm was used extensively in the design of a RAMDAC chip, which was eventually fabricated and successfully tested [45].

5. CONCLUSIONS

The main problem associated with substrate noise is a generalized degradation of performance induced mainly by the appearance of spurious currents generated by the circuit's digital switching activity. The paper focuses on the models of noise transport in view of creating optimized circuits or technologies in mixed-signal and digital designs. Solutions to the substrate noise problem are presented in light of the results obtained from industrial examples.

References

- [1] C. Hu, *VLSI Electronics: Microstructure Science*, volume 18, Academic Press, New York, 1981.
- [2] Y. Cheng, M. Chan, K. Hui, M. Jeng, Z. Liu, J. Huang, K. Chen, J. Chen, R. Tu, P. K. Ko and C. Hu, *BSIM3v3 Manual*, University of California at Berkeley, Berkeley, CA, 1996.
- [3] E. Charbon, P. Miliozzi, L. Carloni, A. Ferrari and A. L. Sangiovanni-Vincentelli, "Modeling Digital Substrate Noise Injection in Mixed-Signal ICs", *Trans. on Computer Aided Design*, vol. CAD-18, n. 3, pp. 301 310, March 1999.
- [4] D. A. Kirkpatrick, *The Implications of Deep Sub-micron Technology on the Design of High Performance Digital VLSI Systems*, PhD thesis, University of California at Berkeley, December 1997.
- [5] P. Parakh and R. B. Brown, "Crosstalk Coustrained Global Route Embedding", in *Proc. ACM International Symposium on Physical Design*, pp. 201 206, April 1999.
- [6] D. K. Su, M. Loinaz, S. Masui and B. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", *IEEE Journal of Solid State Circuits*, vol. SC-28, n. 4, pp. 420 430, April 1993.
- [7] F. J. R. Clement, E. Zysnan M. Kayal and M. Declercq, "LAYIN: Toward a Global Solution for Parasitic Coupling Modeling and Visualization", in *Proc. IEEE Custom Integrated Circuit Conference*, pp. 537 540, May 1994.
- [8] B. R. Stanisic, N. K. Verghese, D. J. Allstot, R. A. Rutenbar and L. R. Carley, "Addressing Substrate Coupling in Mixed-Mode ICs: Simulation and Power Distribution Synthesis", *IEEE Journal of Solid State Circuits*, vol. SC-29, n. 3, pp. 226 237, March 1994.
- [9] N. K. Verghese, T. Schnerbeck and D. J. Allstot, *Simulation Techniques and Solutions for Mixed-Signal Coupling in ICs*, Kluwer Academic Publ., Boston, MA, 1995.
- [10] T. Smedes, N. P. van der Meijs and A. J. van Genderen, "Extraction of Circuit Models for Substrate Cross-Talk", in *Proc. IEEE International Conference on Computer Aided Design*, pp. 199 206, November 1995.
- [11] R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in ICs", *IEEE Journal of Solid State Circuits*, vol. SC-31, n. 3, pp. 344 353, March 1996.

- [12] M. Pfof and H. M. Rein, "Modeling and Measurement of Substrate Coupling in Si-Bipolar ICs up to 40GHz", *IEEE Journal of Solid State Circuits*, vol. SC-33, n. 4, pp. 582 591, 1998.
- [13] C. P. Coelho, J. R. Phillips and L. M. Silveira. "Robust Rational Function Approximation Algorithm for Model Generation", in *Proc. IEEE/ACM Design Automation Conference*, pp. 207 212, June 1999.
- [14] X. Huang, V. R. Raghavan and R. A. Rohrer, "AWESim: A Program for the Efficient Analysis of Linearized Circuits", in *Proc. IEEE International Conference on Computer Aided Design*, pp. 534 537, November 1990.
- [15] P. Feldmann and R. W. Freund, "Efficient Linear Circuit Analysis by Pade Approximation via the Lanczos Process", *IEEE Trans. on Computer Aided Design*, vol. CAD-14, n. 5, pp. 639 649, May 1995.
- [16] L. M. Silveira, M. Kamon, I. Elfadel and J. White. "A Coordinate-Transformed Arnoldi Algorithm for Generating Guaranteed Stable Reduced-Order Models of RLC Circuits", in *Proc. IEEE International Conference on Computer Aided Design*, pp. 288 294, November 1996.
- [17] W. F. Ames, *Numerical methods for partial differential equations*, Academic Press, San Diego, 1992.
- [18] G. Strang and G. J. Fix. *An Analysis of the Finite Element Method*, Prentice-Hall, Englewood Cliffs, NJ, 1973.
- [19] I. S. Duff, A. M. Erisman and J. K. Reid, *Direct Methods for Sparse Matrices*, Clarendon Press, Oxford, 1986.
- [20] Y. Saad, *Iterative Methods for Sparse Linear Systems*, PWS Publishing, Boston, MA, 1996.
- [21] J. A. Meijerink and H. A. van der Vorst, "An Iterative Solution Method for Linear Systems of which the Coefficient Matrix is a Symmetric M-Matrix", *Mathematics of Computation*, vol. 31, pp. 148 162, January 1977.
- [22] W. Hackbusch, *Multigrid Methods and Applications*, volume 4 of *Computational Mathematics*, Springer, Berlin, 1985.
- [23] J. H. Bramble, J. E. Pasciak and J. Xu. "Parallel multilevel preconditioners", *Mathematics of Computation*, vol. 55, pp. 1 22, 1990.
- [24] D. Colton and R. Kress. *Integral Equations Methods in Scattering Theory*, Krieger, Malabar, Florida, 1992.
- [25] K. E. Atkinson. "A Survey of Boundary Integral Equation Methods for the Numerical Solution of Laplace's Equation in Three Dimensions", in M. A. Goldberg, editor, *Numerical Solution of Integral Equations*, pp. 1 34, Plenum Press, New York, 1990.
- [26] S. M. Rao, T. K. Sarkar and R. F. Harrington, "The Electrostatic Field of Conducting Bodies in Multiple Dielectric Media", *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-32, n. 11, pp. 1441 1448, November 1984.
- [27] W. T. Weeks, "Calculation of Coefficients of Capacitance of Multiconductor Transmission Lines in the Presence of a Dielectric Interface", *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-18, n. 1, pp. 35 43, January 1970.
- [28] T. Smedes, N. P. van der Meijis and A. J. Genderen, "Boundary Element Methods for 3D Capacitance and Substrate Resistance Calculations in Inhomogeneous Media in a VLSI Layout Verification Package", *Advances in Engineering Software*, vol. 20, n. 1, pp. 19 27, 1994.

- [29] R. Gharpurey, *Modeling and Analysis of Substrate Coupling in ICs*, PhD thesis, University of California at Berkeley, May 1995.
- [30] R. Crampagne, M. Ahmadpanah and J. L. Guiraud, "A Simple Method for Determining the Green's Function for a Large Class of MIC Lines Having Multilayered Dielectric Structures", *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-26, pp. 82-87, 1978.
- [31] R. F. Harrington, *Field Computation by Moment Methods*, MacMillan, 1968.
- [32] A. J. van Genderen, N. P. van der Meijis and T. Smedes, "Fast Computation of Substrate Resistances in Large Circuits", in *Proc. European Design and Test Conference*, pp. 560-565, March 1996.
- [33] E. Charbon, R. Gharpurey, R. G. Meyer and A. L. Sangiovanni-Vincentelli, "Analysis and Optimization of Substrate Noise in VLSI ICs", *IEEE Trans. on Computer Aided Design*, vol. CAD-18, n. 2, pp. 172-190, February 1999.
- [34] Y. Saad and M. Schultz, "GMRES: A Generalized Minimal Residual Algorithm for Solving Nonsymmetric Linear Systems", *SIAM Journal on Scientific and Statistical Computing*, vol. 7, n. 3, pp. 856-869, July 1986.
- [35] J. P. Costa, M. Chou and L. M. Silveira, "Efficient Techniques for Accurate Modeling and Simulation of Substrate coupling in mixed-signal ICs", in *Design, Automation and Test in Europe*, pp. 892-898, February 1998.
- [36] J. R. Phillips and J. K. White, "A Precorrected-FFT Method for Electrostatic Analysis of Complicated 3D Structures", *IEEE Trans. on Computer Aided Design*, vol. CAD-16, n. 10, pp. 1059-1072, 1997.
- [37] J. P. Costa, M. Chou and L. M. Silveira, "Precorrected-DCT Techniques for Modeling and Simulation of Substrate coupling in mixed-signal ICs", in *Proc. IEEE International Symposium on Circuits and Systems*, volume 6, pp. 358-362, May 1998.
- [38] S. Kapur and D. E. Long, "IES³: Efficient Electrostatic and Electromagnetic Simulation", *IEEE Computational Science and Engineering*, vol. 5, n. 4, pp. 60-67, October-December 1998.
- [39] M. Chou and J. White, "Multilevel integral equation methods for the extraction of substrate coupling parameters in mixed-signal ICs", in *Proc. IEEE/ACM Design Automation Conference*, pp. 20-25, June 1998.
- [40] J. Tausch and J. White, "A Multiscale Method for Fast Capacitance Extraction", in *Proc. IEEE/ACM Design Automation Conference*, pp. 537-542, June 1999.
- [41] S. Mitra, R. A. Rutenbar, L. R. Carley and D. J. Allstot, "Substrate-Aware Mixed-Signal Macro-Cell Placement in WRIGHT", in *Proc. IEEE Custom Integrated Circuit Conference*, pp. 529-532, May 1994.
- [42] K. Joardar, "A Simple Approach to Modeling Cross-Talk in Integrated Circuits", *IEEE Journal of Solid State Circuits*, vol. SC-29, n. 10, pp. 1212-1219, October 1994.
- [43] F. Romeo, *Simulated Annealing: Theory and Applications to Layout Problems*, PhD thesis, University of California at Berkeley, March 1989.
- [44] E. Charbon, *Constraint-Driven Analysis and Synthesis of High-Performance Analog IC Layout*, PhD thesis, University of California at Berkeley, December 1995.
- [45] I. Vassiliou, H. Chang, A. Demir, E. Charbon, P. Miliozzi and A. L. Sangiovanni-Vincentelli, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology", in *Proc. IEEE International Conference on Computer Aided Design*, pp. 463-468, November 1996.