Single Ended Pass-Transistor Logic

A comparison with CMOS and CPL

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Abstract: SPL (Single-rail Pass-transistor Logic) is one of the most promising logic styles for low power circuits. This paper examines some key issues in the implementation of SPL: swing restoration, optimum number of pass-transistor stages between buffers and SPL circuits with two supply voltages. Simulation results based on netlists extracted from layout are presented to compare SPL, CPL and standard CMOS.

1. INTRODUCTION

In a survey of low power circuit design we concluded that pass transistor logic styles, and especially SPL (Single-rail Pass-transistor Logic also known as Single-ended Pass-transistor Logic or LEAP - Lean Integration with Pass-Transistors [5]), are very promising for low power circuits.

This paper presents the results that we have obtained from simulations of SPL circuits and it will examine some key issues in the implementation of SPL: swing restoration, optimum number of pass transistor stages between intermediate buffers and SPL circuits with two supply voltages. A number of simple circuits were implemented in three logic styles: SPL, CPL and CMOS using GSC200 MITEL CMOS standard library cells and simulated under a variety of conditions.

All the circuits presented in this paper were implemented in the Mitel 3.3V 0.35 μ m CMOS technology and all of the simulations were performed using Cadence Spectre simulator. The simulations were performed using

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netlists extracted from layout using supply voltages between 1.8 and 3.3Volts (3.3V is the maximum allowable supply voltage while 1.8V is the minimum supply voltage for the Mitel standard cell library).

2. SPL OVERVIEW

Our survey of contemporary low power techniques concluded that the SPL logic style is a promising logic style for low power design. One of the papers that popularised the SPL logic style is [5]. In [6], SPL is also reported to be a promising pass-transistor style: it has the advantage of efficient implementation of complex functions, especially arithmetic functions and, because it uses only NMOS transistors, the layout is very compact, simple and regular.

Figure 1. Full adder: BDD representation and the SPL circuit

The advantages of SPL are:

- Circuits are easy to synthesise starting from the Boolean expressions using Binary Decision Diagram (BDD) graphs. A pass-transistor network maps directly to a BDD diagram (Figure 1). The circuits in Figure 1 are the SPL implementation of the BDD diagrams for a full adder (two good introductory papers about BDDs are [1])
- An SPL cell library has no more than 10 basic components [5]. These components are simple pass transistors cells, simple inverters and inverters with swing restoration
- The pass transistor network has fewer transistors than a CMOS network, especially for large functions and functions based on multiplexers and XORs

- The transistors in the pass network are all N-type transistors
- The circuit layout is very compact and regular because the pass transistor network contains only N type transistors. So the layout consist of rows of inverters alternating with pass transistor networks

The disadvantages of SPL are:

- Difficult to integrate with existing circuit synthesis tools
- The delay of the circuit is more sensitive to voltage scaling than for complementary CMOS logic. More factors have to be taken into account when designing SPL for low voltages. Simulation results presented later in this paper show that the delay of SPL circuits increases dramatically when the supply voltage approaches $V_{TN}+V_{TP}$, the theoretical lower limit of the supply voltages for SPL circuits. However [3] shows that using dynamic threshold pass-transistor logic, SPL and CPL circuits can work with a reasonable delay at very low supply voltages

3. IMPORTANT ISSUES FOR SPL

3.1 Swing Restoration

Because the SPL logic style uses only N type transistors in the pass-transistor network, the voltage swing at the end of a pass transistor network will be 0V to $V_{dd}-V_{TN}$, (V_{TN} is the threshold of the N type transistor). Therefore, the buffers inserted in the pass-transistor network, or at the outputs of the pass-transistor network, must have a swing restoring circuit in order to minimise the leakage currents through the inverters. In [4] a generalised circuit for converting low voltage swings to full swing is presented. Other approaches use amplifiers, but this is not good for low power design because of the permanent static current of the amplifiers. In the next section we will show that using two supply voltages it is possible to replace swing restoring inverters with simple inverters. In, *Figure 2* four versions of swing restoring inverters are presented (A, B, C and D).

Version A is the simplest and the most commonly used. B is a “faster” version of the swing restoring buffer because it loads the output with a smaller gate capacitance (M_{P2}) and the M_{P3} transistor is always on. However, simulation results show that the power consumption and the delay of this inverter are about the same as the simplest one while the area of the cell layout is bigger. By connecting the gate of the transistor M_{P3} to an enable line, it is possible to enable or to disable the swing restoring circuit.

Figure 2. Swing restored inverters

The problem with the inverters A and B is that the swing restoring circuit is activated after a low to high transition is propagated through the inverter. This propagation time is affected by the load of the inverter, especially at low supply voltages. C and D avoid this problem by making the load of the inverter connected to the swing restoring transistor (M_{p3}) constant. *Figure 3* presents simulation results for swing restoring inverters. The results include the power and delay of a 4 pass transistor chain connected before the inverters and a large load. The circuits were simulated using a random input signal with an activity factor $\alpha=0.5$ and frequency of 100 MHz.

Figure 3. The Power consumption and delay of four pass transistors followed by different swing restoration inverters. Circuit load is 1mm metal track and 10 or 25 inverters

For large loads we prefer version D to version C because it uses tapered inverters. In this way the power consumption can be optimised [2]. This is confirmed by the results in *Figure 3*. However, within a pass-transistor network, a buffer with a big fan-out can be replaced by more smaller inverters within each branch.

3.2 Using Two Supply Voltages

Simulation results in the previous section show that the swing restoring inverter circuit is an important contributor to the delays of SPL circuits especially at low supply voltages or if the output is connected to a large load. By using two supply voltages it is possible to replace some of the swing restoring inverters with simple inverters. This approach reduces the power consumption of SPL circuits.

It can be noted that the only difference between the circuits in *Figure 7* and *Figure 8* is that the swing restoring inverters are replaced by normal inverters supplied at $V_{dd}-V_{TN}$. Given that the voltage swing at the end of a pass transistor network is 0V to $V_{dd}-V_{TN}$, swing restoration circuits are not required.

Not all the swing restoring inverters can be replaced in this way. If the output of an inverter is connected to a pass transistor gate, it has to have full swing on the output (0V to V_{dd}). In this case, if the inverter were to be supplied at $V_{dd}-V_{TN}$, another V_{TN} would be lost through the N-type pass transistor so the swing at the output would be 0V to $V_{dd}-2V_{TN}$.

Simulations show that the optimum power-delay product is obtained if the second supply voltage is about $V_{dd}-V_{TN}$. It is not practical to reduce the second supply voltage further without reducing the other supply voltage as well. In sections 4 and 6 simulation results of SPL circuits with two supply voltages are presented.

3.3 Long Pass-Transistor Chains

The delay of a pass transistor chain increases quadratically with the number of stages. To improve the delay of the pass transistor chain, intermediate buffers can be inserted. We have simulated a 60 pass-transistor chain with buffers inserted every 1,2,3,4,5 or 6 stages. *Figure 4* shows the power and the delay of the pass transistor chain at a supply voltage of 3.3V (the curves look similar for other supply voltages). The contours on the graph mark the constant power-delay product curves.

The goal of these simulations is to find the optimum power-delay product and this is obtained for a buffer every 4 or 5 stages in both cases. In real circuits it is probable that the buffers will be inserted every 3 or 4 stages. Real circuits are more complex than simple pass transistor chains, so the parasitic capacitances of the pass-transistor networks are bigger. Another reason is that this avoids high complexity of the pass-transistor networks between the buffer rows. Additionally, it must be noted that there is a significant trade-off between power and speed for varying the number of

buffers and depending on the requirements of the design, circuits can be optimised differently.

Figure 4. The power and delay of a 60 stage pass transistor chain with inserted buffers. $V_{cc}=3.3V$ (3.3V and 2.5V in the two supply voltages case)

4. FULL ADDER SIMULATION RESULTS

The full adder is one of the most widely used circuits in comparing logic styles. It is implemented very efficiently in pass transistor styles, so we expect that it will perform well in SPL: simulation results confirm this fact.

Figure 5. CPL full adder

We compared a standard cell, a SPL (Figure 1) and a CPL full adder (Figure 5). All of these adders were simulated in identical conditions:

- Stimulus: random; activity factor $\alpha=0.5$; simulation interval: 0 to $2\mu s$
- Frequency: 100MHz for all 3 inputs; rise and fall times: 1ns
- Load circuit: RC circuit modelling a $100\mu m$ metal track followed by 1, 4 or 10 parallel inverters

Figure 6 shows the power and delay for SPL, CPL and standard cell full adders. In all cases, the power consumption of the SPL full adder is about

half of the standard cell library element. At 3.3V, the delay of the SPL full adder is slightly greater but is significantly greater for lower supply voltages. The power-delay product of the CPL circuit is about the same as the power-delay product of the CMOS standard cell.

At 1.8V the SPL full adder is more than twice as slow as the standard cell adder. The reason for this is the P-type swing restoring transistor on the output inverters. This inverter must be replaced with the more complex version of the swing restoration inverter. We used version D presented in section 3.1 and both cases are displayed in *Figure 6b*.

Figure 6. Power and delay for SPL, CPL and standard cell full adders. Circuit load is 100mm metal track followed by 1,4 or 10 standard inverters

CPL circuits are generally slower than SPL circuits. The reason is that the drive capability of the pass transistor network is poorer than the drive capability of an inverter in the SPL case. Only at very low supply voltages for large loads do the simulation results show that CPL circuits are faster than SPL. At 1.8V supply voltage the CPL circuits are slightly faster than SPL, but at higher supply voltages the SPL circuits become faster.

The layout area of the SPL full adder is smaller than the area of the standard cell. The SPL full adder cell is $26.8 \times 10.3 \mu m$ ($276.04 \mu m^2$) comparing with $32.2 \times 12.6 \mu m$ ($405.72 \mu m^2$) of the smallest full adder from the standard library.

5. 4 BIT ADDERS

5.1 SPL Carry Chain Versions

As for any adder, the critical part of an SPL adder is the carry circuit. We tested three possible versions obtained by reordering the circuit inputs. This reordering does not affect the circuit structure because the carry function is

symmetrical. However reordering does affect the power consumption, the delay and, to a small degree, the area of the circuit.

Figure 7. SPL carry chain (SPL1)

The carry chain in *Figure 7* is the simplest one. It is obtained by cascading the carry circuit of the SPL full adder (*Figure 1*). The only trick is that the inputs of the second stage are inverted, which means that the second carry will be inverted. This is a consequence of a basic BDD property [1] and it is used to avoid double inverters between two stages.

Figure 8. SPL carry chain with two supply voltages (SPL1 version)

Figure 8 shows the same circuit as *Figure 7* but in this case the two supply voltage scheme is used.

The circuit in *Figure 9* is an attempt to make the carry chain faster. Instead of passing the carry signals through all the pass transistor network, they are applied directly to the last pass transistor stage of the carry circuit.

Figure 9. Faster SPL carry chain (SPL2)

Figure 10 shows the best version of a SPL carry circuit. In this case the buffers are inserted only every 4 pass-transistor stages. This also matches the optimum number of pass transistor stages between buffers, as presented in section 3.3. Simulation results in the next section show that this version is as fast as the previous one (Figure 9), but the power consumption is reduced.

Figure 10. Low power SPL carry chain (SPL3)

For the last two versions (Figure 9 and Figure 10) the swing restoring inverters cannot be replaced by a normal inverters supplied at $V_{dd}-V_{TN}$ as the outputs of a carry stage are connected to pass transistor gates in the next stage.

5.2 Simulation Results

All of the simulated adders were implemented in the same technology and simulated with identical conditions. The simulation scenario is similar to the one presented in the previous section, except that, for simulation speed reasons, the load for each output consist of a 20fF capacitor.

Figure 11 shows the power and the delay for the four versions of SPL adders and a 4 bit ripple carry adder made of standard cell full adders. In all the cases the power is the total power of the 4 bit adder and the delay is the delay of the carry chain (measured from carry input to carry output). The graph in Figure 11a corresponds to a supply voltage of 3.3V and in Figure 11b to a supply voltage of 2V. For the case of two supplies, the voltages

used are 3.3V and 2.5V in the first case and 2V and 1.2V in the second case (Note: these results cannot be compared directly with the results for the single bit adder because circuit loads vary).

Figure 11. Power and delay of a 4bit ripple carry adder composed of full adder standard cells and 4 versions of SPL 4bit adder

At both supply voltages the power consumption of the SPL adders is half or less than standard cell adder, but the delay is worse. One of the reasons is that the driving capability of the inverters on the output of the SPL circuits is smaller. More significant is the fact that the power delay product is better for the SPL adders in almost all the cases. As we expected, the performance of the SPL adder degrades faster than the one made of standard cells when the supply voltage is decreased. For this technology $V_{dd} = 2\text{V}$ is quite close to the limit of the supply voltage for the SPL circuit, which is about 1.3V - the sum of the N-type and P-type threshold voltages.

Another important conclusion is that SPL1 with two supply voltages (Figure 8) has the best power-delay product in both cases and the single supply version of this circuit (Figure 9) is the worst among the SPL circuits.

6. SIMPLE GATE - SIMULATION RESULTS

Small gates that are very well implemented in CMOS logic style are not very efficiently implemented in SPL. This means that SPL circuits must be designed as large circuits in one step rather than breaking them into gates and implementing each gate in SPL.

We chose a simple gate from the standard library whose function is $(A'B') + CD$. In CMOS it can be implemented with two inverters and a one stage 4 input gate. Figure 12 shows the SPL implementations that we simulated (the CPL circuit has two similar pass transistor networks).

It is obvious that, for such simple gates, the SPL implementation is more complex and requires more transistors than the CMOS implementation. The SPL implementation requires 17 transistors and the CMOS implementation 12 transistors (the CPL implementation uses 28 transistors).

Figure 12. SPL implementation of $(A'B') + CD$ Boolean function

Even though the SPL circuit is more complex, its performance is not much worse than that of the CMOS circuit. Figure 13 shows the simulation results for $V_{dd}=3.3V$ and $2V$. The load of the circuit consists of a 20, 80 or 200fF capacitor. The results are consistent with the results for the adders presented in the previous sections. The CPL circuit is slower and has a greater power consumption than the SPL circuit. Again we can see that the performance of the SPL and CPL circuits is degraded at low supply voltages.

Figure 13. Power and delay for a simple gate implemented in SPL, CPL and CMOS (std. cell)

7. CONCLUSIONS

We have presented simulation results that show the type of functions that are best implemented in SPL and the type of functions that are not

efficiently implemented. The conclusion is that SPL is a good low power alternative if:

- The implemented functions are arithmetic, XOR and MUX based circuits
- SPL circuits are not efficiently implemented if we try to replace the basic cells in a CMOS standard library with SPL based cells
- The supply voltage of the circuit is not too close to $V_{TN}+V_{TP}$, the theoretical lower limit of the supply voltages for SPL circuits. Simulations that we performed have shown that an optimum supply voltage is about $2(V_{TN}+V_{TP})$

We also presented some important issues about SPL and concluded that:

- For the swing restoring buffers with big loads the best approach is to use tapered inverters with the first one using a swing restoring circuit
- For the technology used, the optimum number of pass transistor stages between buffers is 4 or 5
- Two voltage supply scheme makes circuits faster and less power hungry

Further work is being undertaken to implement large complex circuit blocks in SPL logic. These larger circuits will demonstrate how efficient, from the point of view of power consumption and area, the SPL logic style is in practical cases.

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