Boundary-Scan Testing for Mixed - Signal MCMs

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Abstract

A multi-chip module implementation is shown which provides new features and conditions for mixed-signal boundary-scan testing of MCMs. Assembled non boundary-scan mixed-signal bare dies and integrated passive devices can be tested using active-substrate DFT circuits. The MCM-D is very well suited for electron-beam diagnosis.

Keywords: Mixed-signal/analogue testing, MCM testing, P1149.4 boundary-scan, e-beam testing

1. INTRODUCTION

In the past years, multi-chip module (MCM) techniques which were previously only used in expensive high-speed computers or military applications, are now also beginning to find their way in high-volume consumer microsystems. Examples of their use can be found in high-end televisions, mobile telephones or a compass wristwatch (Tangelder, 1997).

A cost-effective approach in testing PCBs makes use of digital boundary-scan (BS) techniques as specified in the IEEE standard 1149.1 (Bleeker, 1993). Since 6 years, work has progressed with regard to an extension of the 1149.1 standard towards the 1149.4 mixed-signal boundary-scan standard (Sunter, 1996).

In recent years, digital BS techniques are also being introduced for testing MCMs (Zorian, 1992). In practice, unfortunately not all bare dies on an MCM substrate incorporate BS cells. This holds for digital BS cells and, in the current absence of a 1149.4 standard, **certainly** for analogue BS cells. This reduces the effectiveness of the boundary-scan approach in a microsystem, especially with regard to the detail of diagnosis.

In this paper, an implementation is shown of a silicon-substrate based MCM-D. All interconnection wiring and passive as well as active devices can be integrated in this substrate. Based on this implementation, different constraints apply in terms of the requirements of mixed-signal BS hardware as compared to a PCB environment. As a result, a selected set of new BS cells have been designed based on our MCM-D design rules. Also the associated test-control hardware has been designed. This set of DfT circuits provides excellent testing possibilities for MCM-Ds.

Although only briefly discussed in this paper, the completely planar structure of the MCM-D implementation is very suitable for electron-beam diagnostics of **complete** MCMs.

2. PLANAR MCM-D IMPLEMENTATION

In order to implement a **high-density** MCM for a microsystem (Tangelder, 1996), a test MCM-D has been designed, implemented and evaluated to investigate its potentials. The manufacturing process has not been presented before, although some elements can be found in other publications (Hopper, 1992).

The MCM-D substrate used is p-type silicon. It forms the basis for a conventional CMOS process flow, currently employing two metal levels and two poly-silicon layers. The latter are used to implement passive devices (R, C). There is however a difference between the MCM-D process and our conventional CMOS process with regard to the minimum dimensions used. This has to do with the direct-contact (1:1) MCM-D lithography.

The interconnections on the substrate are established by the first and second metal, **except** for the **bridge** from the substrate to the bare dies. These bridges, implemented in third metal, replace the relatively error-prone wire-bondings at the cost of an additional IC mask.

A cross-view drawing of the substrate with an embedded bare die is shown in Figure 1. A photomicrograph of part such an MCM is seen in Figure 2. The overall dimensions of this MCM are 210mm by 220 mm. For the sake of clarity, one hole for a guest bare die has been left open, while the other one is populated with a 50k digital Sea-of-Gates chip.

Figure 1 Cross-view of the populated MCM-D

Figure 2 Photomicrograph of the partly completed MCM

The substrate is covered on both sides with silicon nitride acting as a "hole" mask. Next, holes are anisotropically etched in the substrate.

Therefore the hole in front is slightly larger than the dimensions of the guest bare die, while the back-end is larger. This is favourable for the thixotropic paste to mount the bare die within the substrate.

3. MIXED-SIGNAL BOUNDARY-SCAN IN MCM-DS

The MCM-D environment is different from the one in a PCB with regard to boundary-scan testing. This has a direct impact on the electrical requirements of the mixed-signal (MS) BS cells. As previously discussed, the design rules for these MCM-Ds are less aggressive than those in current advanced CMOS processes which influences the BS-cell capabilities. All these constraints resulted in the design of dedicated mixed-signal BS cells in our MCM-D process.

3.1 Mixed-Signal BS in active-substrate MCM-Ds

Although criticised by several semiconductor companies and not yet an IEEE standard, the current P1149.4 draft provides sufficient information for designing and evaluating several realisations of the suggested hardware (Lofstrom, 1996).

In many libraries of semi-custom semiconductor manufacturers, digital boundary-scan cells are available now, including the associated test control such as the TAP controller (Koopman, 1992). However, a full coverage of bare dies for MCMs which are completely boundary-scan testable (1149.1/P1149.4) is not available nowadays and it remains the question whether this will ever be achieved.

A full boundary-scan bare-die population is not a prerequisite for the BS concept in MCMs. Furthermore, the research on testing non-BS **clusters** is progressing (Lubaszewski, 1994), but the testability of separate bare dies and passive components within the clusters will remain limited. In many cases this is not acceptable, as several (potentially good) bare dies have to be removed, replaced and rewired for often one faulty bare die.

We compensate for this limitation by introducing digital as well as analogue BS cells around the non-BS bare dies in the substrate of the MCM. To use the active substrate of an MCM for introducing **digital** BS cells in the case of non-boundary-scan cells has already been presented earlier (Maly, 1994). For mixed-signal MCMs, no investigations have been carried out yet.

It can be calculated (Oliver, 1996) that in several cases it is even **more cost-effective** to implement BS cells in the active substrate instead of in the bare dies. In the extreme case, the bare dies can be glued on top of the active-substrate BS cells, and subsequently interconnected.

For the sake of simplicity, Figure 3 shows a symbolic representation of an example of an MCM-D with two non boundary-scan bare dies and a passive component Z. Furthermore, each bare die is assumed to have analogue and digital parts. In a practical situation, more passive components and several analogue as well as digital bare dies are involved of which some digital ones will feature digital boundary-scan facilities.

The black boxes in the bare dies are the bonding pads which are connected to digital I/O buffers (D-I, D-O) and analogue input and output buffers (A-I, A-O). In our MCM-D approach, these bare-die bonding pads are connected to the BS cells via small metal **bridges** (see Figure 1). Bare-die digital I/O can be connected to bidirectional digital BS cells (DBC = Digital Boundary Cell) and analogue inputs and outputs to bidirectional analogue BS cells (ABC = Analogue Boundary Cell). It is of course also possible to design and use unidirectional cells.

In both cases, additional **ESD protected buffering** (grey triangles in Figure 3) is required for BS cells connected to MCM input and output bonding pads. The black boxes in the MCM-D substrate are the MCM bonding pads to be used for wire bonding to the ceramic PGA package.

Figure 3 Example of active BS architecture in an MCM-D

Besides the MCM system digital input (DI) and output (DO) and their analogue counterparts (AI, AO), also bonding pads are incorporated for BS testing purposes.

For simplicity, the BS control pads (TDI, TDO, TMS, TCK, TRST*) have not been connected to the test controllers (TCON) in Figure 3. The internal TDO of the

first controller is connected to the internal TDI of the second one. Hence, the shown TDO and TDI pads are the external ones.

A TCON consists of an extended 1149.1 TAP controller, instruction register and decoder. The external analogue test bus (AT1, AT2) is connected to the Analogue Test Bus Control (ATBC), which is the circuit controlling the routing between the external bus and internal bus (AB1, AB2). It is possible to share parts of the hardware in the TCONs and ATBCs.

Figure 3 shows that the concept of Known Good Substrate (KGS) testing requires more effort in our MCM-D case than in other approaches. It basically requires mixed-signal wafer testing. For this reason, bridging pads and ESD protection and some form of buffering is also required at the "bridge"-side of the active-substrate BS cells because of substrate test handling.

3.2 Requirements of BS cells in MCM-Ds

The mixed-signal BS cells were primarily designed for application in our type of sensor-based microsystems (Tangelder, 1997), which generally feature low frequencies ($<10\text{MHz}$) and modest voltage and current levels. Hence, the requirements of the analogue switches in the ABCs (Sunter, 1996) and (Lofstrom, 1996) are relatively modest. The use of BS in MCM-Ds in the current approach requires several types of buffers for different purposes:

1. ESD-protected, full-size buffers for the MCM-D analogue and digital inputs and outputs, able to handle electrical requirements at the PCB level. Standard CMOS bond-pad buffering circuits can be used.
2. ESD-protected, medium-size input and output buffers between bridges and BS cells to enable KGS testing with active probes (0.1 pF , $\text{ILEAK} < 0.1\text{ pA}$)
3. Non-ESD protected, small output buffers to interconnect BS cells from different bare dies on the substrate.

In principle, buffer 1 can do all jobs but this is rather inefficient in terms of area and power consumption. The buffer 1 type is located around the MCM bonding pads.

Buffer 2 is integrated in the BS cell together with a number of switches, such as the ones for "core disconnect" and the ones to the V+ and V- in the analogue case (Sunter, 1996), (Lofstrom, 1996). Buffer 2 can also do the job of buffer 3.

Buffer 3 is also integrated in the BS cell.

As Figure 3 indicates, the location of BS cells differs in the MCM-D approach from PCBs and "conventional" MCMs. In the case of an active substrate, the BS cells are equally distributed around the bare die.

In an MCM-D, the analogue or digital **cores** as specified in standard (1149.1) and draft (P1149.4) are only accessible via ESD-protected I/O buffers. In most (analogue) cases, these have no facility to be put in an off-mode state, and hence the conceptual switch (**core disconnect**) (Sunter, 1996 and Lofstrom, 1996) should be incorporated in the BS cells.

Another difference of the MCM-D with a PCB has to do with the passive components. Whereas in PCBs missing components and wrong component types are reality, this situation is very unlikely to occur in MCM-Ds. The passive components (as well as the active) are evaluated during the Known-Good Substrate (KGS) tests. Hence, BS facilities for evaluating passive devices are rarely used.

As result of our implementation technique, also other design considerations emerged for the BS cells. It was assumed that the dimensions of the bare-die **bonding pads** are basically governed by required mechanical spacing of conventional wire-bonding techniques. The minimum size to be expected is around 80 by 80µm and the spacing is minimal 100µm. In our concept this does not hold for the **bridging pads** in the substrate. As it is still required to be able to carry out "Known-Good Substrate" tests, especially if active devices are incorporated, the **bridging pads** have to be around 25µm by 25µm to enable the use of active microprobe access. In the case of conventional wafer probing, bridging pads of 80µm by 80µm are required. We have chosen for the last option in this first test. The distance between these bridging pads is governed by the spacing of the bare-die bonding pads (~100µm). The bridging pads are integrated in the BS cells. The distance of the BS cells from the etched holes (Figure 1) is (200µm + 20µm=) 220µm, where the first value accounts for the slope and the second one for the distance between the mask of the hole and the cell. With all the above data, the architecture, pitch and position of the BS cells is now fixed. To reduce the substrate wiring, the test-control circuits are located near the bare dies.

3.3 Design of BS-cells in active substrate

Although digital BS cells and the associated TAP controller have been designed in the past at our institute using the Sea-of-Gates design methodology (Koopman, 1992), a full-custom redesign had to be made in the MCM-D process. The design of the selected BS cells was implemented such, that abutment of neighbouring cells is possible. If the distance between the bare-die bond pads is larger than the minimum, a flexible metal-interconnection cell of variable width can be

automatically inserted between neighbouring BS cells. These interconnection cells have to be transparent to enable incoming and outgoing signals which do not require BS cells, such as the power-supply lines.

The DBC has been designed according to the 1149.1 standard (e.g. Bleeker, 1993), employing a D-Flipflop, a D-latch and two MUXs. In the design they are combined with buffers.

The ABC uses the same type of flipflops, latches and MUXs as the DBCs. The difference lies in additional control logic for the analogue switches, and of course the requirements of the different switches. A detailed scheme of the 5-switch ABC can be found in (Sunter, 1996) and (Lofstrom, 1996). One can recognise a sliced architecture in this cell. A symbolic scheme of such a slice is shown in Figure 4.

The switches have different capabilities and implementations. The core disconnect and V+ and V- have been integrated in the **"bridge"** buffers, which are required for KGS testing anyhow. The other switches have been implemented on the basis of transmission gates with different widths. As stated before, our application area does not require very high performance switches.

Figure 4 Control slices and transmission-gate switches and switched buffers in the ABC

The transistor gate dimensions used in the MCM-D process are $3\mu\text{m}$ by $15\mu\text{m}$ for the NMOS and $3\mu\text{m}$ by $45\mu\text{m}$ for the PMOS transistors. The boundary-scan cell

slice comprises an inverter, D-Flipflop, D-latch and simple logic. Including an analogue transmission-based switch, it measures $180\mu\text{m}$ by $180\mu\text{m}$ and incorporates 30 transistors. The layout of this type of boundary-scan cell slice in our MCM-D process is shown in Figure 5.

The extended TAP controller has been automatically synthesised using the "Compass logic synthesiser", employing custom-made logic primitive blocks (Inverter, NAND, NOR and FlipFlop) in our MCM-D process. After automatic placing and routing the layout required an overall area of $1050\mu\text{m}$ by $1535\mu\text{m}$.

The ATBC is implemented with the same slices as discussed previously. The TECON and ATBC are located near the bare die BS cells.

Figure 5 Layout of the Boundary-Scan cell slice in our MCM process

4. INITIAL RESULTS

As could be expected from the relatively large minimum dimensions as dictated by the MCM-D process, there were speed limitations in terms of correct operation. Above 30 MHz, the signals in the BS cell slice deteriorated to the extent that correct operation of the cells could not be guaranteed anymore. This also holds for the test control parts. The resistance values of the analogue switches have an influence on the analogue testing capabilities in the BS concept. The difference in

"on" and "off" resistance of the designed transmission gates was limited, around a ratio factor of 100; this can be increased, by enlarging the width at the cost of speed or by incorporating an operational amplifier at the cost of increased active area.

5. ADVANTAGES FOR ELECTRON-BEAM DIAGNOSIS

Although the practice of using electron-beam probers for testing planar MCM **substrates** has been shown before by using charge / discharge techniques (Brunner, 1993), the suggested MCM implementation in this paper has a number of advantages in comparison with conventional MCM implementations in electron-beam testing of the **entire MCM**. By this is meant the populated substrate, including the bare dies.

In the conventional case, thick ($\sim 800\ \mu\text{m}$) bare dies are mounted on top of a substrate, hence causing focusing problems in the beam switching between substrate and bare dies. In addition, high-rising bonding wires around the bare dies can create disturbances of the beam (generated magnetic fields). In our **completely planar MCM** these problems can not occur, hence easing the road to electron-beam diagnosis of **complete** MCMs (including bare dies !). For the analogue parts, there are of course clear limitations in achievable sensitivity and frequency range.

First diagnostic experiments with an electron-beam prober have started using an extended wafer stage for MCMs able to accommodate MCM sizes up to $8 * 8\ \text{cm}$. Subsequent repair of planar MCM-Ds is only confined to repair of metallisation tracks on the substrate, bridges and bare dies. Our experience shows that this can be successfully accomplished with focused ion-beam systems if required.

6. CONCLUSIONS

In this paper, a design has been made of complementary mixed-signal boundary-scan cells in the active substrate of an MCM-D. Specific requirements have been presented to support this environment. The current implementation of the boundary-cells is larger in area and slower in speed than could be achieved in an advanced IC process. It is stressed that the active devices are **only** used to implement boundary-scan cells for non-boundary-scan bare dies and associated registers and controllers, in order to keep the occupied active area and hence yield of the substrate to acceptable levels. However, it makes a completely mixed-signal boundary-scan based testing approach feasible in complex MCM-D microsystems. The planar structure is also very well suited to provide electron-beam diagnosis of the substrate and bare dies at the same time.

7. REFERENCES

- Tangelder, R. , Diemel, G. and Kerkhoff, H. (1997) Smart Sensor System Application: an Integrated Compass *Proc. European Design & Test Conference*, Paris.
- Bleeker, H., et al. (1993) Boundary-Scan Test. Kluwer Academic Publ.
- Sunter, S. (1996) The P1149.4 Mixed Signal Test Bus: Costs and Benefits *Proc. International Test Conference*, 444-450.
- Zorian, Y. (1992) A Universal Test Strategy for Multi-Chip Modules based on BIST and Boundary-Scan *Proc. IEEE ICCD*, 59-66.
- Hopper, A., et al. (1992) A Feasibility Study for the Fabrication of Planar Silicon Multi-Chip Modules using Electron Beam Lithography for Precise Location and Interconnection of Chips *IEEE Trans. on Components, Hybrids and Manufacturing Technology*, Vol. 15, No.1, 97-101.
- Lofstrom, K. (1996) A Demonstration IC for the P1149.4 Mixed-Signal Test Standard, *Proc. International Test Conference*, 92-98.
- Koopman, R. and Kerkhoff, H. (1992) A High-Density Sea-of-Gates Architecture incorporating Testability Support *Proc. of the ISCAS*, 2977-2980.
- Lubaszewski, M. et al. (1994) A Pragmatic Test and Diagnosis Methodology for Partially Testable MCMs *IEEE MCM Conference*, 108-113.
- Maly, W., et al. (1994) Smart-Substrate Multi-Chip Module Systems *IEEE Design and Test of Computers*, 64-73.
- Oliver, J. and Kerkhoff, H. (1996) A Cost Analysis Study for Testability Purposes on Silicon Active Substrates *IEEE Trans. on Components, Packaging and Manufacturing Technology*, Vol. 19. No. 2, 179-186.
- Brunner, M. and Schmid, R. (1993) Electron-beam MCM Substrate Tester *IEEE MCM Conference*, 62-68.