E-TSPC: Extended True Single-Phase-Clock CMOS circuit technique

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Abstract

The Extended True Single-Phase-Clock (E-TSPC), an extension of the TSPC CMOS circuit technique, is proposed and analysed. This technique consists of a set of composition rules to build CMOS single-phase circuits. The composition rules are provided to avoid race problems and to preserve data during the holding phases. The used CMOS blocks are the conventional static CMOS logic, n/p dynamic logic, n/p latch, data precharged, and the new N-MOS like blocks. Design results show that the E-TSPC can achieve 70% speed improvements, comparing with conventional TSPC techniques, and large power and area savings. A complete dual-modulus prescaler (divide-by-128/129) was implemented in a 0.8 μ m CMOS process, and a 1.61GHz rate was achieved with a 14.2mW power consumption.

Keywords

VLSI design, high speed digital CMOS, clock strategy,

1 INTRODUCTION

Several CMOS clocking policies have been proposed to design VLSI systems. The pseudo-two-phase logic was one of the earliest techniques (West, 1985). Later on two-phase logic structures were proposed, like the Domino technique (Krambeck, 1982) and the NORA technique (Goncalves, 1983 and 1984). A single-phase clock policy was first introduced in (Yuan, 1987) (the True Single-Phase-Clock (TSPC)) and subsequently advanced by (Afghahi, 1990).

In this work we introduce and analyse the new Extended True Single-Phase-Clock CMOS circuit technique (E-TSPC). E-TSPC is an extension of the TSPC technique and consists of a full set of composition rules to build CMOS single-phase circuits, which uses static, dynamic, latch, data precharged, and N-MOS like blocks. The

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new N-MOS like blocks enhance the capability of the technique, since they allow building p-MOS chains with speed comparable to n-MOS. The result is a powerful technique which permits the design of complex and fast circuits.

Next section presents the main design rules of the E-TSPC technique, the proofs of their correctness, and an exception rule. The new N-MOS like blocks are introduced in section 3. Some design examples are considered in section 4, and the main conclusions are drawn in section 5.

2 COMPOSITION RULES FOR THE E-TSPC CMOS TECHNIQUE

We will present in this section the composition rules for E-TSPC. They were built in a way similar to that of NORA (Goncalves, 1984). The NORA technique is based on two-phase logic structures, and it uses static, n/p-dynamic, and C²MOS logic blocks. The composition rules in NORA were provided to avoid race problems.

2.1 Basic CMOS blocks

An E-TSPC circuit can use static CMOS logic, n/p-dynamic blocks, n/p-latches, and high (PH)/low (PL) data precharged blocks (Dp blocks) (Figures 1 and 2).

Figure 1 Construction blocks of the E-TSPC technique.

Dp blocks require a more detailed explanation (Yuan, 1993). In Figure 2 we show how PH and PL blocks can be formed, using as example the logic function $d = \overline{a(b+c)}$. The circuits are structured starting from the static block. When a PH block is desired, for instance, we modify the n-transistor logic by handling the parallel branches. For each group of k parallel branches, we cut $(k-1)$, leaving only one branch. This process is depicted in Figure 2, and the two resulting PH blocks, in Figure 2b. Similarly, a PL block can be obtained if p-transistor branches are modified. The final speed of the Dp block depends on the cut transistors.

The PH block inputs which are connected to the block n-transistors and the PL block inputs, connected to the p-transistors, are called precharged inputs (pc-inputs). The PH blocks whose pc-inputs are high, when the clock is low, and the PL blocks whose pc-inputs are low, when the clock is low, are called n-Dp blocks. Similarly, a

p-Dp block denotes a PH block with pc-inputs at high or a PL block with pc-inputs at low whenever the clock is high.

Figure 2 Transformation from a static block (a) into Dp blocks: (b) PH blocks; (c) PL blocks.

2.2 Composition rules

We will present the composition rules. First, the concept of data chain is done.

Definition 1: A **n-data chain** is any not cyclic signal propagation path:

1. containing at least one n-latch, or one n-dynamic, or one n-Dp block;
2. starting in a circuit external input, or in the output of a p-latch, or p-dynamic, or p-Dp block; when this output is followed by static blocks in the normal data flow, the data chain starts in the output of the last static block;
3. going through static, n-dynamic, n-Dp, or n-latch blocks;
4. regardless of the number and ordering of the blocks defined above;
5. finishing in a circuit external output, or in the input of the first p-latch, or p-dynamic, or p-Dp block.

For the p-data chain, equivalent definition applies, changing n by p and vice-versa everywhere in the definition (we will use χ -data chain, where χ is n or p).

Except for clock skew race, TSPC systems are subject to race errors and connection limitations, which are equivalent to NORA two-phase race and connection difficulties. Additionally, new connection rules should be incorporated to warrant the correct operation of the n/p-latch (Yuan, 1987 and Afghahi, 1990) and the PL/PH blocks (Yuan, 1993).

Five composition rules are proposed below for the E-TSPC technique. Any data chain should observe all rules for correct operation.

Composition rule 1 (r_1): Consider any χ -data chain. The χ -data chain input should be: an input of a dynamic block, an input of a latch, or a not pc-input of a Dp block.

Composition rule 2 (r_2): Consider any χ -data chain. A χ -latch must not drive,

directly or through static blocks, a χ -dynamic or a χ -Dp block.

Composition rule 3 (r_i): Consider any χ -data chain. The number of inversions between:

- r_{3a} . any two adjacent χ -dynamic blocks must be odd;
- r_{3b} . any two adjacent Dp-blocks of the same type must be odd;
- r_{3c} . any two adjacent Dp-blocks of complementary types must be even;
- r_{3d} . a PH (PL) block adjacent to a n (p)-dynamic (or vice versa) in a n (p)-data chain must be even;
- r_{3e} . a PL (PH) block adjacent to a n (p)-dynamic (or vice versa) in a n (p)-data chain must be odd.

Where two blocks are called adjacent if there are only static blocks between them.

Composition rule 4 (r_d): Consider any χ -data chain and the last dynamic block in this data chain (when it exists). The number of signal inversions, from this dynamic block up to at least one χ -latch, must be even.

Composition rule 5 (r_s): Consider any χ -data chain. It must have one of the two configurations:

- r_{5a} . at least one dynamic block and one latch;
- r_{5b} . at least two latches and an even number of inversions between them.

2.3 Analysis of r_i - r_s correctness

We will present six theorems which show that when the composition rules r_i - r_s are obeyed, **no problems** due to discharge, pre-charge, and data holding occur. The proofs of the theorems demand two additional hypotheses:

Hypothesis 1 (hyp_1): The clock phases of the system are long enough to permit all data chain input signals and output of dynamic blocks in holding to propagate up to the data chain outputs.

Hypothesis 2 (hyp_2): The circuit external inputs should be stable during the evaluation phase of the data chains. Therefore, the external inputs of n-data chains should be stable when clock= "1" (ϕ ="1"); the external inputs of p-data chains should be stable when clock= "0" (ϕ ="0").

Additionally, a definition of block order is necessary in the theorem proofs.

Definition 2: Consider a Dp or a dynamic block B_q , and the set $F = \{ \text{all } \chi\text{-data chains which go through } B_q, \text{ where if } B_q \text{ is a n-block, } \chi \text{ is n, and if } B_q \text{ is a p-block, } \chi \text{ is p} \}$. We call the number $\Theta(B_q) = \text{maximum}\{(\text{number of } \chi\text{-Dp blocks which precedes the } B_q \text{ block in the data chain } D_c) \forall D_c \in F\}$ the B_q order.

The theorems and their proofs will follow.

Theorem 1 (2): If the composition rules are obeyed by all data chains, then the output of a n-Dp (**p-DP**) block will reach the

"1" value, for a PL block, or "0" value, for a PH block, after some time in holding phase, and it will keep this value while ϕ ="0" (ϕ ="1").

Proof for theorem 1 (for theorem 2, it is analogue): To proof this theorem, we will proceed by mathematical induction with respect to the block order.

First, we should establish that the theorem is true for any n-Dp block B_0 with **zero order**. There are two possibilities (r_1 and r_2):

- i. B_0 is a PL block; in this case, all data chains going through the B_0 pc-inputs are connected to n-dynamic blocks, and there is an odd number of inversions between B_0 and the dynamic block (r_{3e});
- ii. B_0 is a PH block; in this case, all data chains going through the B_0 pc-inputs are connected to n-dynamic blocks, and there is an even number of inversions between B_0 and the dynamic block (r_{3d}).

When $\phi = "0"$, the n-dynamic outputs are "1", and consequently all pc-inputs are "0" and "1" for PL and PH blocks, respectively. The pc-inputs will force the PL output to "0" and the PH output to "1"; thus, the theorem is true for **zero order** blocks.

It remains to show that if the theorem is true for any n-Dp block of order **N or less**, it is also true for a n-DP block B_{N+1} with **order equal to N+1**.

First, let us take the B_{N+1} as a PL block. Any data chain going through a pc-input of B_{N+1} has one of the following blocks:

- i. a n-dynamic block, and there is an odd number of static inversions between B_{N+1} and this block (r_{3e});
- ii. a PL block, and there is an odd number of static inversions between B_{N+1} and the PL block (r_{3b});
- iii. a PH block, and there is an even number of static inversions between B_{N+1} and the PH block (r_{3c}).

In the case (i), the dynamic block will impose "0" to the B_{N+1} pc-inputs when $\phi = "0"$; it is similar to zero order blocks. On the other hand, the PL and PH blocks connected to B_{N+1} , cases (ii) and (iii), have **order N or less**. In consequence, their outputs are all at "1", for PL blocks, or "0", for PH blocks, when $\phi = "0"$. These signals will arrive at the B_{N+1} inputs, after passing through the inversions, with value "0". Hence, all B_{N+1} pc-inputs will be at "0", and its output will be at "1".

A similar reasoning can be applied if B_{N+1} is a PH block so the theorem is true for any block with **N+1 order**. Hence, by induction, the theorem is true for any n-DP block. ■

Theorem 3 (4): Consider a n-data (p-data) chain, and let δ be the output of the data chain last latch. If the composition rules are obeyed by all data chains, then δ is stable during the whole holding phase ($\phi = "0"$ ($\phi = "1"$)).

Proof for theorem 3 (for theorem 4, it is analogue): Consider all data chains D_{C1} , D_{C2} , .. D_{CM} which go through δ . They are all n-data chains. The δ value will be modified only if (we use *hyp₁*):

- a. the input of any n-data chain D_{Ci} was modified, and the signal propagates to δ ;
- b. the pre-charge of a dynamic block of any data chain D_{Ci} propagates to δ .

We will show that none of these arrangements can occur. Consider the data chain D_{Ci} . Two cases are possible:

- i. the data chain has two n-latches, and there is an even number of inversions

between them (r_{sb});

- ii. the data chain has at least one dynamic block, and there is an even number of inversions between the last dynamic block and one n-latch (r_d, r_{sa}).

First, consider the case (i); B_1 and B_2 designate, respectively, the first and the second latch of D_{C1} . After B_1 no dynamic block is allowed (r_2). Thus the data chain D_{C1} can modify δ only when a signal propagates from B_1 input up to δ . Suppose that a B_1 input has a "0" $\rightarrow$ "1" transition. This transition can not modify the block output and, consequently, the δ value. Alternatively, if, during the $\phi = "0"$ phase, any B_1 input changes from "1" to "0", the transition may act on the B_1 output, putting it at "1", and propagate to the B_2 input; as a result, "0" $\rightarrow$ "1" transition is imposed on B_2 input (if the signal does not propagate to B_2 input, it does not cause δ modification). This type of transition does not change the B_2 output value, so the signal propagation is blocked. Hence, in case (i) there is not propagation up to δ .

Consider now the case (ii); the last dynamic block will be called B_1 , and the latch which follows B_1 after an even number of inversions, B_2 . When $\phi = "0"$, B_1 is pre-charged at "1". The B_1 pre-charge arrives at B_2 input with "1" and can not propagate through this latch; additionally, any transition which arrives at a B_1 input is stopped since the block is pre-charging. In conclusion, δ keeps its value both in the case (i) and in the case (ii), so the theorem is true. ■

Theorem 5 (6): Consider a n-data (p-data) chain in evaluation phase ($\phi = "1"$ ($\phi = "0"$)). If the composition rules are obeyed by all data chains, then can only appear transitions of:

"0" $\rightarrow$ "1" ("1" $\rightarrow$ "0"), in the inputs of dynamic blocks,

"0" $\rightarrow$ "1", in the inputs of PL blocks, or

"1" $\rightarrow$ "0" in the inputs of PH blocks.

Proof for theorem 5 (for theorem 6, it is analogue): In order to proof this theorem, we will proceed by mathematical induction with respect to the block order.

First, we should establish that the theorem is true for any block B_0 with **zero order**. Let us start with a n-dynamic or a PL block. A B_0 input is connected to:

- i. one circuit external input (r_i , except for pc-inputs);
- ii. the output of one or more blocks B_{di} , where B_{di} is a:
 - a. p-latch, and there is any number of static inversions between B_0 and B_{di} (r_i);
 - b. n-dynamic block, and there is an odd number of static inversions between B_0 and B_{di} (r_{3a}, r_{3e});

In the case (i), the external input is stable when $\phi = "1"$ (*hyp*₂). Hence, no transitions occur in B_0 input for the case (i). In the case (ii), the B_0 input will be modified only if a B_{di} output is modified, and it propagates up to B_0 . When B_{di} is a p-latch, (ii.a), the modification is not possible since B_{di} output is stable while $\phi = "1"$ (theorem 4). Alternatively, when B_{di} is a n-dynamic, (ii.b), only "1" $\rightarrow$ "0" transitions are possible at its output during the evaluation phase, and, except for "0" $\rightarrow$ "1", B_0 input has no transitions. A similar reasoning can be applied to PH blocks. Thus, the theorem is true for **zero order** blocks.

It remains to show that if the theorem is true for any block of order **N or less**, it is also true for a block B_{N+1} with **order equal to N+1**.

Suppose that B_{N+1} is a n-dynamic or a PL block. A B_{N+1} input is connected to:

- i. one circuit external input (r_i , except for pc-inputs);
- ii. the output of one or more blocks B_{Di} , where B_{Di} is a:
 - a. p-latch, and there is any number of (static) inversions between B_{N+1} and B_{Di} (r_i);
 - b. n-dynamic block, and there is an odd number of (static) inversions between B_{N+1} and B_{Di} (r_{3a}, r_{3e});
 - c. PL block, and there is an odd number of (static) inversion between B_{N+1} and B_{Di} (r_{3b}, r_{3e});
 - d. PH block, and there is an even number of (static) inversion between B_{N+1} and B_{Di} (r_{3c}, r_{3d}).

For the case (i), the reasoning is the same as the zero order blocks. In the case (ii), the B_{N+1} input will be modified only if a B_{Di} output is modified, and it propagates up to B_{N+1} . For (ii.a) and (ii.b), the arguments are also the same as zero order blocks. For (ii.c), B_{Di} has order **equal to or less than N**, so the inputs of the block have only "0"→"1" transitions; therefore, its output has transitions of "1"→"0", and, due to the odd number of inversions, the B_{N+1} input may have only "0"→"1" transitions. In (ii.d), B_{Di} has order **equal to or less than N**, so its inputs have only "1"→"0" transitions, and again the inputs of B_{N+1} may have only "0"→"1" transitions.

A similar reasoning can be applied to PH blocks so the theorem is true for any block with **N+1 order**. Hence, by induction, the theorem is true for any block. ■

2.4 Exception rule

Although the above described rules are necessary to avoid race problems, typical TSPC systems do not follow some of them. The most common exception is found in connecting two D-flip flops (Figure 3). In such configuration p-data chains (B_{L1} or B_{L4}) appear with only one p-latch (r_i violation). In consequence, the p-latch output may change during the holding time.

Figure 3 Two TSPC D-flip flops connected in series.

Normally the delay between nodes a_i and b_i is long enough to ensure that b_i is fully discharged through transistors N_1 and N_2 . In this case, the second D-flip flop works properly.

We introduce a simple exception rule which covers the D-FF connection case.

Exception rule (r_j): Configurations similar to the one of Figure 3, where rules r_i and r_s are not obeyed, are accepted.

3 N-MOS LIKE LOGIC EXTENSION

The given rules allow extremely complex logic designs. When high speed is also a requirement, restrictions on the use of p-dynamic and p-latch blocks should be imposed. These blocks have at least two p-transistors in series, which may considerably reduce the maximum speed. Normally in such applications, the p-data chains are limited to one block, and most logic operations are handled with n-data chains. Of course, when designs are done in this way, part of the rules strengths are lost, and deeper pipelines are necessary.

We can minimise this difficulty and also increase the n-data chain speed by means of N-MOS like blocks. Similar technique was used in (Chang, 1996), but the authors restrained the changes to D-flip flops.

The presence of two complementary logic blocks, one with p-transistors and the other with n-transistors, is one characteristic of CMOS logic; conversely, in N-MOS logic, complementary blocks do not appear, and the correct operation is guaranteed through the transistor sizing. New N-MOS like blocks are built from the dynamic blocks and latches, and their operation is based on transistor sizing too. Figure 4 shows dynamic/latch blocks and their N-MOS like version.

Figure 4 Conversion to N-MOS like blocks.

The transistor dimensions of the modified blocks should follow the Table 1 constraints. Those constraints specify which part of the circuit, n or p-transistors, must impose the output value when both n and p-logic blocks are conducting. In Figure 4 the dominant parts are drawn with bold lines.

Since the modified blocks have a reduced number of transistors in series, they are

faster but consume more power. In consequence, they should be only used in critical data chains, where the desirable speed has not been reached. The exchange of blocks, N-MOS like for normal blocks, is easily performed since both types of blocks are subject to exactly the same rules (r_1 , r_s or r_e). The composition rules, r_1 , r_s and r_e , the static blocks, the n/p-dynamic, the n/p-latch, the PH/PL data precharged, and the N-MOS like blocks compose the E-TSPC technique.

Table 1 Conditions for correct operation in the N-MOS like blocks

<i>Circuit block</i>	<i>clock=high</i>	<i>clock=low</i>
N-MOS like n-dynamic	no constraint	output is high (independently of inputs)
N-MOS like p-dynamic	output is low (independently of inputs)	no constraint
N-MOS like n-latch	output=high if the p-trans. logic is conducting; otherwise, low	no constraint
N-MOS like p-latch	no constraint	output=low if the n-trans. logic is conducting; otherwise, high

4 DESIGN RESULTS

The full strength of the E-TSPC technique, mainly for high speed applications, is only evaluated through circuit examples. A high-speed dual-modulus prescaler (divide-by-128/129) was designed using a standard 0.8 μ m CMOS bulk process (the effective length is 0.7 μ m).

Figure 5 shows a schematic of the circuit. The cross-hatched part of the circuit, composed of three D-FFs and two logic gates, forms a divide-by-4/5 counter. The signal *div32* selects if it counts up to 4 (*div32=high*) or up to 5 (*div32=low*). The five D-FFs at the bottom of the figure form a divide-by-32 counter. The fractional division ratio of the prescaler, 128 or 129, is selected according to *Sm* signal.

The complete layout of the divide-by-4/5 counter, which composes the high speed critical part of the prescaler, was drawn, and SPICE netlists were extracted for four different approaches. These approaches are:

D_{c1} : design with conventional rise edge-triggered TSPC D-FF (Figure 3);

D_{c2} : design with rise edge-triggered D-FF, and further optimisation applying the E-TSPC technique;

D_{c3} : design with a modified fall edge-triggered D-FF (Chang, 1996);

D_{c4} : design with fall edge-triggered D-FF, and further optimisation applying the E-TSPC technique (Figure 6).

In consequence, the achieved area and power consumption are very high. Fall-edge-triggered TSPC D-FFs modified with N-MOS like blocks and with small sized transistors are used in (Chang, 1996). The resulting circuit has small area and lower power consumption. Our implementation, with the E-TSPC technique and small sized transistors, resulted in the smallest area and the lowest power consumption; the speed, in addition, is comparable to (Huang, 1996).

Figure 6 Transistor schematic of the D_{64} approach. The transistor width/length, in μm , or only the width is indicated in the figure (in this case the length is $0.8\mu\text{m}$).

It is clear from the previous examples that the application of the composition rules and the N-MOS like blocks (the E-TSPC technique) can significantly improve the circuit characteristics on area, speed, and power.

Table 3 Area, speed, and power consumption results for three different prescalers

Prescaler	Technology (μm)	Area (10^3mm^2)	Speed (GHz)	Power ($\mu\text{W}/\text{MHz}$)
(Huang, 96)	1.0	39.1	1.6	31.2
(Chang, 96)	0.8	13.7	1.22	20.9
(this work)	0.8	12.6	1.61	8.9

5 CONCLUSIONS

The new Extended True Single-Phase-Clock (E-TSPC) CMOS circuit technique was presented and analysed. The E-TSPC technique represents an improvement in the following aspects:

- the composition rules are little restrictive allowing the designer to take full advantage of the blocks potential;
- the N-MOS like blocks can increase the speed of the circuit everywhere it is necessary. Moreover, since the conventional and N-MOS like blocks follow the same composition rules, they are exchangeable, and the cost of any substitution, in terms of time, is very small;
- p-data chains can be designed to be as fast as n-data chains. In fact, p-data chains can use only N-MOS like p-latches, which have the logic implemented with n-transistors.

Some design results show that speed increases and power/area savings are found with the E-TSPC technique application. A complete high-speed dual-modulus prescaler (divide-by-128/129) was designed in a 0.8 μ m CMOS process, and simulations of the extracted circuits from layout reached 1.61GHz with power consumption of 8.9 μ W/MHz.

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