Design and Verification for Hierarchical Power Efficiency System (HPES) Design Techniques Using Low Power CMOS Digital Logic

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Abstract. This paper presents the design implementation of digital circuit and verification method for power efficiency systems, focused on static power consumption while the CMOS logic is in standby mode. As complexity rises, it is necessary to study the effects of system energy at the circuit level and to develop accurate fault models to ensure system dependability. Our approach to designing reliable hardware involves techniques for hierarchical power efficiency system (HPES) design and a judicious mixture of verification method is verified by this formal refinement. This design methodology is validated by the low power adder with functional verification at the chip level after satisfying the design specification. It also describes a new HPES integration method combining low power circuit for special purpose computers. The use of new circuits and their corresponding HPES design techniques leads to minimal system failure in terms of reliability, speed, low power and design complexity over a wide range of integrated circuit (IC) designs.

1 Introduction

The most important role of design and verification work is to make sure that all circuits and systems operate safely. Some designers devote countless hours to rigorously testing all integrated circuits (ICs) as part of designer's responsibility to help ensure that the system remains fail-free with minimal energy usage.

These days special purpose computers associated with energy-efficient designs are becoming more important in telecommunications, and networking systems. As one possible way of implementing energy-efficient system design, we propose the hierarchical power efficiency system (HPES) design techniques which include low power CMOS digital logic focused on stable system fault coverage.

This special purpose requirement, a low power adder design with HPES, is therefore a good example of the development of fail-free environments because it contains a well established logical prover, and uses a variety of logic.

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The implementation in this paper differs from others in the following aspects. This paper proposes a new low power design method by providing a fast logical approach and low power dissipation. The outcome, such as a low power adder is introduced and a new method is derived by extending and modifying a conventional adder for the performance comparison.

To explore the design methodology for these special purpose computers, we should consider power efficiency with circuit-level implementation as well as system-level dependability. Therefore, we discuss validation of a HPES design techniques, comparing performance issues, in order to clarify the essence of design methodology in the design and verification work. By design of circuit and system validation, we show an empirical analysis of the full system reliability and emphasize the overall power efficiency.

2 Low Power CMOS Digital Circuit Design

Based on logic evaluation methods, CMOS circuits are classified into static CMOS and dynamic CMOS circuits. Static CMOS circuits have both pull-down and pull-up paths for the logic evaluation [1]. Table 1 shows the criteria of CMOS logic styles for high performance microprocessors [2].

In addition, the static power dissipation ($P[x]_{static}$) will be reduced since the threshold voltage V_t will be high when the transistors are off. So, the static power dissipation formula can be added,

$$P[x]_{static} = \frac{I_{d0n} + I_{d0p} V_{DD}}{2} \tag{1}$$

where $I_{d0x} = exp\frac{-Vt}{nV_{th}}$, n is approximately 1.5, and x can be defined as the leakage current of nMOS and pMOS. Consequently, the peak power consumption ($P[x]_{peak}$) can be summarized as follows.

$$P[x]_{peak} = i_{peak} V_{peak} = \max[p(t)] \tag{2}$$

$$P[x]_{avg} = \frac{1}{T} \int P(t)dt = \frac{V_{DD}}{T} \int i_{supply}(t)dt \tag{3}$$

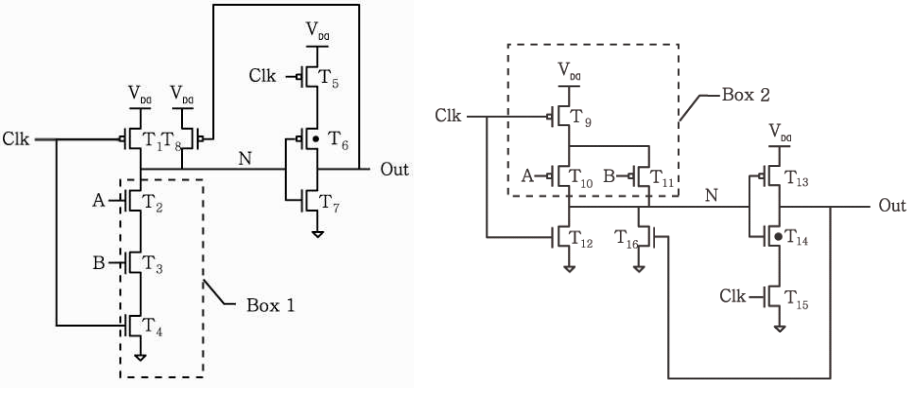
We can represent the output of a circuit by a mathematical equation such as equation (3). $P[x]_{avg}$ may be a simple linear function for a linear circuit, or a complicated non-linear function for a non-linear circuit. The output of a circuit depends on the current input as well as the previous output and the values of energy storage elements such as capacitors. To build a circuit model, hspice simulation was done to gather input/output data. Then, coefficient for the linear model was determined by least mean square (LMS) error criterion, as shown in equation (2). As expected, this simple linear circuit model generates less accurate simulation result for output signal results.

Additionally, the lower the threshold voltage of a given transistor, the higher the leakage currents (I_{off}) in that transistor. Higher leakage currents may result

Table 1. Criteria of CMOS Logic Styles

Operation Structure	Remarks
Static	**Static Complementary**: CVSL(Unclocked), Complementary, Differential split-level **Static Non-Complementary**: pseudo nMOS
Dynamic	**Dynamic Complementary**: CVSL(Clocked) **Dynamic Non-Complementary**: Domino, Zipper1, Zipper2, Nora , Latched Domino

in higher static power dissipation in typical circuits as the threshold voltages decrease, and the leakage currents increase [3]. In one embodiment, the precharge transistor and the evaluate circuit transistors may be high-V_t transistors and may contribute to low static power dissipation since low leakage current is generated. In Figure 1, a low power CMOS digital logics are implemented.



(a) Low power CMOS digital logic (b) Its complementary circuit

Fig. 1. Schematic view of low power CMOS digital circuits

A transistor having the lower threshold voltage is referred to herein as a low-V_t transistor which is illustrated in the drawings with a dot in the center, T_6, in Figure 1(a) [4]. This circuit is meant to simultaneously control leakage currents and enhance performance could provide a boost to circuit design as V_{DD} drops below $1V$. If low power CMOS digital logic provides as much performance as it promises, this work would help provide incentive for future technology generations to have better body contacts and change the way that transistors are optimized.

Therefore, this development through the low power CMOS digital logic, is the key idea to overcome energy limitation in this special purpose computers.

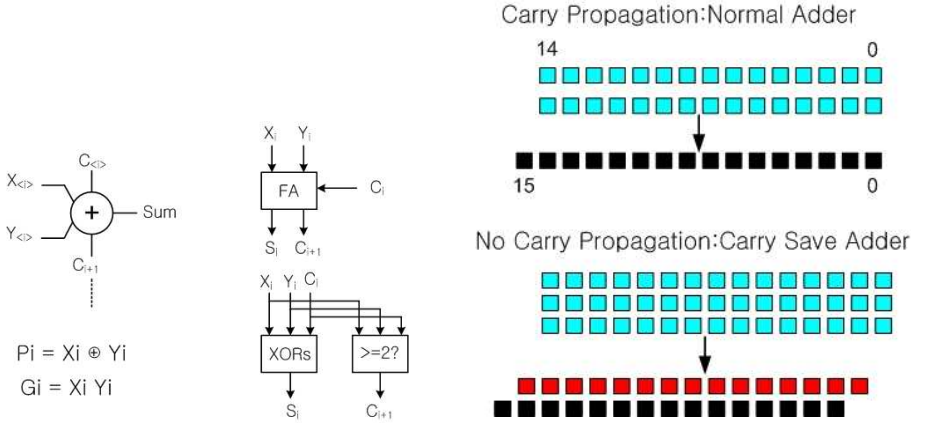
As we discussed, the low power digital logic which included low leakage currents and high-threshold voltage circuits will be validated as a result of formal

verification. Therefore, the design of various thereshold voltage circuit strengthens all other advantages of the circuit, such as strong logic correctness, sensitivity on noise margin, and static power dissipation.

3 Design of Low Power Adder

3.1 Low Power Dissipation in Adder Design

Figure 2 shows a one-bit full adder cell as a carry save addition which is commonly used in VLSI design. Carry propagate bit (P_i) and carry generate bit (G_i) can be defined as $X_i \oplus Y_i$ and $X_i \cdot Y_i$, respectively. Therefore, when a row of full adders is applied in parallel, 3 numbers (X_i, Y_i and C_i) can be reduced to 2 numbers (S_i, C_{i+1}), each of a carry bit and a save bit.



(a) Carry propagate/Carry generate and Carry save addition

(b) Normal adder and Carry save addition

Fig. 2. One-bit full adder and Propagate/Generate addition

For complex VLSI chips and systems, these 3 power reduction steps are dominant in terms of delay, power consumption and silicon area. The output, sum and carry are finally converted to one number using a fast carry-propagating adder such as a carry lookahead adder (CLA) using low power CMOS digital logic which included various thereshold voltage logic discussed in Section 2. A detail of the lookahead stage and integrated linear and non-linear logic is shown in Figure 3.

The core array occupies most of the silicon area of a large multiplier but has regularity in the design. In many cases, the core array is designed to have a fixed bit pitch in one direction since it is advantageous to have a common bit pitch for data-path operators such as multipliers, adders and register arrays. The height in the other direction has a reliability in the size depending on the need of the

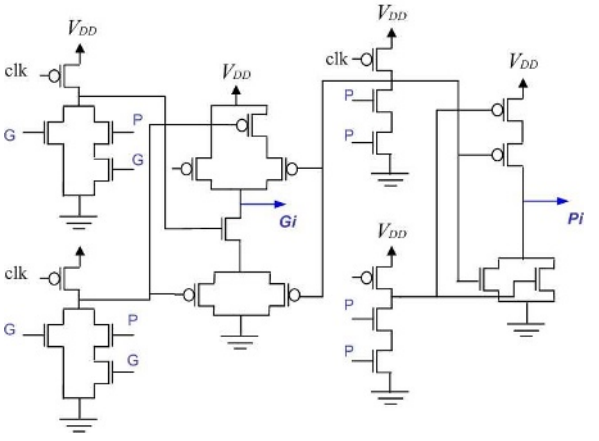


Fig. 3. Schematic view of low power adder lookahead stage

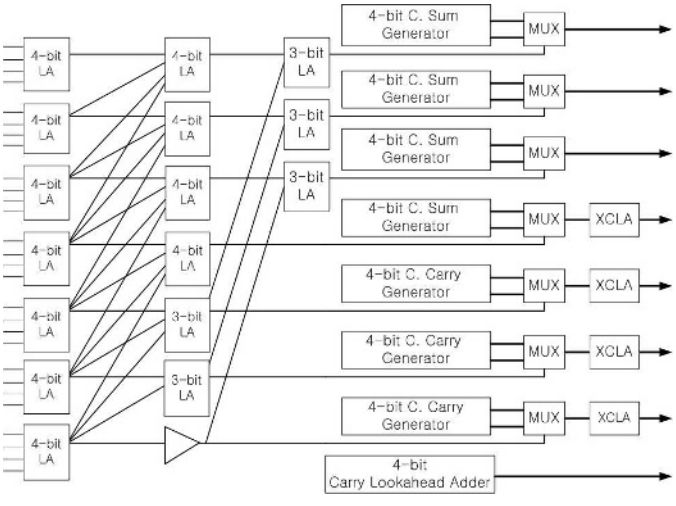


Fig. 4. Block diagram of 32-bit multiplexer core implementation based on 4-bit lookahead adder

specific operator design. Therefore, the core cells such as full adders and Booth multiplexors are stacked vertically and connected together with the same cell width. Figure 4 shows 32-bit slice constructed in this way.

3.2 Hierarchical Power Efficiency System (HPES) Design Approach

High performance design with low power adders is one of the most frequent applications encountered in microprocessor operations and signal processing

applications. Due to its inherent latency and the required large power, we consider a new design and verification method, HPES approach, for this special purpose design which is one of the crucial factors to determine system performance.

We consider a hierarchical design step: Once the power reduction is generated, formal verification can be validated with the multiple number of energy savings. This process is divided into three steps which are (1) low power reduction, (2) formal verification, and (3) dynamic integration of HPES design. The overall design as shown in Figure 5 will be composed of a low power adder design and verification by LAMBDA. In the first step, the product matrix is reduced to the bottom hardware part based on linear circuit modeling. Then, static power is minimized and forms a design product matrix. Dynamic integration and bottom hardware are propagated at the final HPES design stage.

The HPES design, design and formal verification method during synthesis ensure a correct implementation and are employed to provide high coverage of other faults and 100% stuck at fault coverage. In addition, test circuitry is mathematically checked and formally proven not to interfere with the functionality of the IC. Exhaustive simulations and tests are employed using multiple simulations.

Table 2 shows the simulation results on a low power adder from a benchmark suite, ITC99 [6]. For example, the b14 circuit has 245 flip-flops and the test

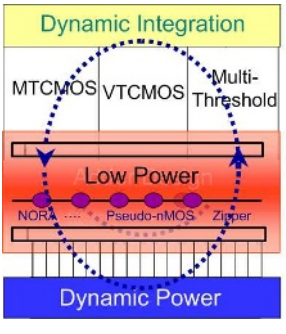


Fig. 5. Hierarchical three steps design with HPES techniques

Table 2. Simulation results of the benchmark suite on low power adder at $1.0V$ V_{DD}

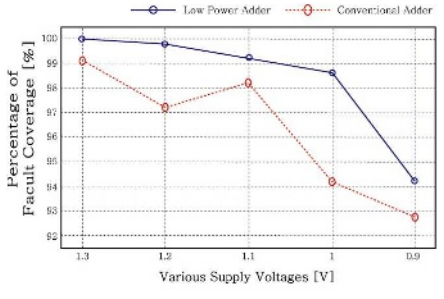
Circuit	Conventional adder		Low power adder		Characteristics of Low power adder	
	no. of FFs	Fault coverage	no. of FFs	Fault coverage	high-V_t usage	Power reduction
b14	245	94.23%	295	99.65%	1,172	17.3%
b15	449	90.12%	499	92.76%	2,148	32.9%
b17	415	87.01%	465	87.11%	1,985	17.6%
$b20_1$	490	92.23%	540	94.92%	2,344	20.2%
b22	735	85.35%	785	87.53%	3,516	19.4%

results have been verified with a set of 160 stimulus vectors and the complete set of benchmark circuits. The first and second column shows a number of FFs and fault coverage from the conventional adder and low power adder, respectively. The last column represents different high-V_t that were a threshold below ground and above V_{DD}. Also, the last column implemented a power reduction rate using a low power adder for comparison. The results confirm that test length and low power adder are significantly reduced while achieving high fault coverage and energy efficiency compared to a conventional adder, with a slight increase in gate length, given that the supply voltage was scaled by at least 10% per technology generation from $0.25\mu m$ to $0.13\mu m$.

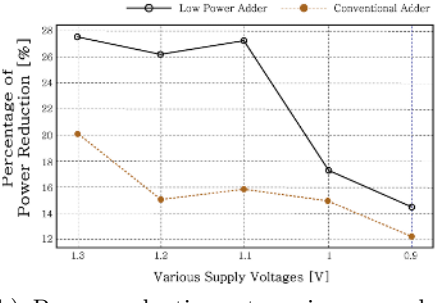
This design was verified by the hardware with functional verification at the chip-level while satisfying the design specification by formal verification tool LAMBDA. The comparison of fault coverage and power reduction rate with a benchmark circuit (i.e., $b14$) at various supply voltages range, from $1.3V$ to $0.9V$, is shown in Figure 6(a). It should be noted that the low power adder design should be determined according to the channel length of the MOS transistor and other design parameters.

In order to achieve comparable results of the chosen power adder and conventional adder, applied to the carry lookahead function, there must be a gradual descent of speed and power metrics. The conventional adder function with high fault coverage applied to the experimental setup is very similar in shape, but with low fault coverage percent. Additionally, Figure 6(b) shows comparison results of conventional and low power adder with power reduction rate.

Despite the different supply voltage scales, a very good comparison of both fault coverage and power reduction can be concluded. HPES design with low power adders is a proven design example that overcome energy limitations and will satisfy the ultimate goal of reliable system impact on minimal power usage.



(a) Fault coverage rate at various supply voltage scales



(b) Power reduction at various supply voltage ranges

Fig. 6. Simulation results of benchmark circuit ($b14$) at various supply voltages, from $1.3V$ to $0.9V$

4 Conclusions and Future Work

The aim of the paper is to model nonlinear circuits using reliable HPES modeling options, which could be a better substitute of a vulnerable design option without losing the system performance. Moreover, the proposed design will save static power consumption and yield benefits for saving overall power dissipation. Finally, this work attempts to solve energy limitation problems using the HPES integration method that would fit within existing design specifications.

In summary, low power CMOS digital circuit power dissipation methodologies in special purpose computer architectures and its HPES design are compared with a view to both design integration and its reliability. New architectures are derived for power reduction methodologies associated with a new design of low power circuit. The better understanding of the effects of power efficiency can be used to develop accurate HPES models that can be applied into the future design technology.

References

1. R. E. Bryant, K. -T. Cheng, A. B. Kahng, K. Keutzer, W. Lamy, R. Newton, L. Pileggi, J. M. Rabaey and A. Sangiovanni-Vincetelli, "Limitations and challenges of computer-aided design tehcnology for CMOS VLSI," *Proc. of the IEEE*, vol. 89., no.3., Mar 2001
2. A. P. Chandrakasan and R. W. Brodersen, "Low power digital CMOS design," *Kluwer Academic Publishers* 1995 USA.
3. P. Pant, R. K. Roy and A Chatterjee, "Dual-threshold voltage assignement with transistor sizing for low power CMOS circuits," *IEEE Trans. on VLSI System*, vol. 9, no. 2, pp. 390-394, Apr. 2001
4. T. Jeong and A. Ambler., "Design trade-offs and power reduction techniques for high performance circuits and system," *Springer-Verlag,* ISSN: 0302-9743, 2006
5. D. Liu and C. Svensson, "Trading speed for low power by choice of supply and thershold voltages," *IEEE J. of Solid-State Circutis*, vol. 28, pp. 10-17, Jan 1993.
6. F. Corno and M. S. Reorda, "RT-level ITC 99 benchmarks and first ATPG results," *IEEE Design and Test of Computers*, pp. 44-53, July-August 2000