COMPUTER TECHNOLOGY

A "hand-shaking" multiplexer for the IBM 1800*

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An instrument is described which is used to multiplex the "ready" and "external sync" lines of an IBM 1800's data channel to 15 external devices. Used with the digital output registers of the computer, the device facilitates the interfacing of non-IBM peripheral devices to the 1800. The multiplexer can be used in any application in which a pair of lines needs to be shared among several devices.

One of the attractive features of the IBM 1800 computer is the availability of digital input and output registers which can be operated under "data channel" control. Each register consists of 16 parallel input or output lines. Bit configurations can be loaded from the computer's memory into the output registers; bit configurations supplied by external devices can be loaded from the input registers into the computer's memory. A variety of registers is available for handling either voltage level changes or contact closures; however, the distinctions between the registers are immaterial for the present report and will, therefore, be ignored.

The input or output from the registers can be controlled either by the central processing unit's accumulator or by the direct-memory-access data channels. In the later mode, data are streamed in and out of core memory without the direct supervision of the on-going program. This mode thus enables the computer to handle multiple tasks in parallel and provides for rapid input or output of large masses of data. Under data channel control, data can be transferred in or out of core at the rate of 500,000 16-bit words/sec.

When data are transmitted between two devices, it is often important to assure that the two devices are operating in concert. It would not do for the external device to transmit a new word to the computer while the computer was fetching and depositing the previous word. Similarly, it would be useless for the computer to fetch words from an input register before these were properly loaded into the output register of the external device. Means are, therefore, required for the computer and the external device to inform each other of their states. In the IBM 1800, these functions are exercised by two "synchronization" lines. When the data channel is "ready" to accept or transmit data, a "ready" signal is generated on a distinct line which is unique to that data channel. The line is normally maintained at −12 V. "Grounding" this line signifies that the computer is "ready." The line will remain "grounded" until the external device responds with an acknowledging signal on a line called the "external synchronization" line, in IBM parlance. This, again, is the grounding of a −12-V line. Upon receipt of the "external sync" signal, the data channel hardware returns the "ready" line to its "off" (−12 V) state, and data are either fetched from or loaded into the computer's memory. If the transmission is to continue, the "ready" line is again grounded and the cycle is continued until the prespecified number of words has been transferred between the computer and the external device.

Several input or output registers can be attached to a single data channel, though all registers on one channel must be either input or output registers. Each of the registers is assigned a unique address, and the hardware can easily and flexibly transmit data via any register at any time by specifying its address at "object" time. Each data channel, however, is equipped with only one pair of synchronization lines, which must be shared by all the registers. The selection of a given register by a program does *not* selectively specify a connection between the synchronization lines and the external devices.

The nature of the problem may be understood in the context of our specific system requirements. We have, over the last several years, found it expedient to purchase a number of non-IBM peripherals for our IBM 1800. We found the analog-to-digital converter manufactured by Datawest Inc. to be superior to the standard A/D system supplied by IBM. We attached to the computer an electrostatic printer-plotter (Versatec's Matrix 1000), which provides high-speed line printing for about one-fifth the cost of the IBM 1443 line printer (admittedly at a higher paper cost). We are now implementing a system of CRT display terminals (the ADDS Consul 880) for use in social psychology and math modeling experiments. All of these devices are interfaced with the 1800 via the digital I/O registers.

Given the usual difficulties of interfacing non-IBM equipment to IBM devices, the use of the digital registers provides an unusually simple and inexpensive interfacing mode. The external device's operation must ordinarily be synchronized with the IBM 1800 via the synchronization lines. It is impractical to tie all the devices to the sync lines "in parallel," for the simple reason that each was designed to respond in a specific way to the arrival of a "ready" signal from the IBM 1800. Sending this signal to any single device would have activated all the others.

While a device addressing network could have been installed so that each of the devices associated with the data channel would respond to its own address, the design and implementation of such a system would have been far more complex, we felt, than the approach we have taken. We have chosen to build a synchronization-line multiplexer. The

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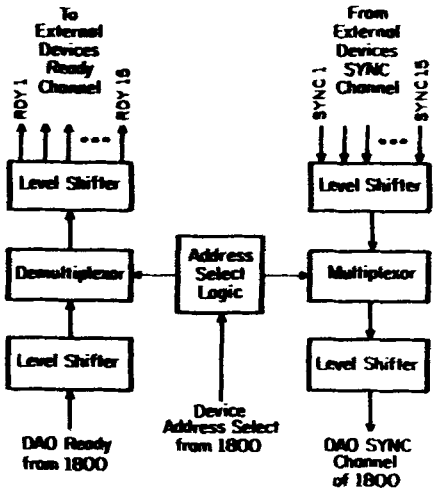

Fig. 1. Block diagram of multiplexer. Signals to and from TTL devices are passed through level shifters to a multiplexing-demultiplexing system. Address selection logic latches the demultiplexer and multiplexer to one of the external devices. Signals to and from these multiplexers are passed through level shifters compatible with the IBM 1800 logic levels.

multiplexer enables the computer to select to which of 15 devices the "ready" and "sync" lines are to be connected at any time. This selection can be achieved either through the transmission of information to the multiplexer from the computer or via a set of toggle switches on the front panel of the multiplexer. This multiplexer has been operating very satisfactorily for several months. In this report, we describe its logical and functional design.

LOGICAL DESIGN

A block diagram of the multiplexer is presented in Fig. 1. All input and output lines pass through a "level-shifting" network. The level-shifting network is required because the logic level used by the IBM 1800's synchronization lines (−12 to 0 V) is not compatible with the logic level common in contemporary TTL logic devices (0 to +3 V).

Sync signals from up to 15 devices arrive at a multiplexer circuit. An address selection network in the multiplexer connects one of its 15 input lines to the output line which is led to the IBM 1800 external sync line via a level shifter. At the same time, the "ready" line from the IBM 1800 is led to a demultiplexer which has 1 input line and 15 output lines. The address selector connects the input line to one of the output lines. Both the multiplexer and the demultiplexer are single-chip integrated circuit (IC) packages (see below). The switching time is specified to be 60 nsec. The address selection signals are supplied to the chips from an address selection network which receives a 4-bit address code either from the IBM 1800 electronic contact-operate (ECO) register or from front panel switches.

ELECTRONICS AND CONSTRUCTION

Our ability to design and build this multiplexer simply and inexpensively derived from the availability of two IC chips which perform the essential multiplexing and demultiplexing functions. The SN74150N is a multiplexer and the SN74154N is a demultiplexer. The manner in which these are utilized in this circuit is illustrated in the detailed circuit diagram in Fig. 2. Four of the multiplexer pins are used for address selections; given a unique bit

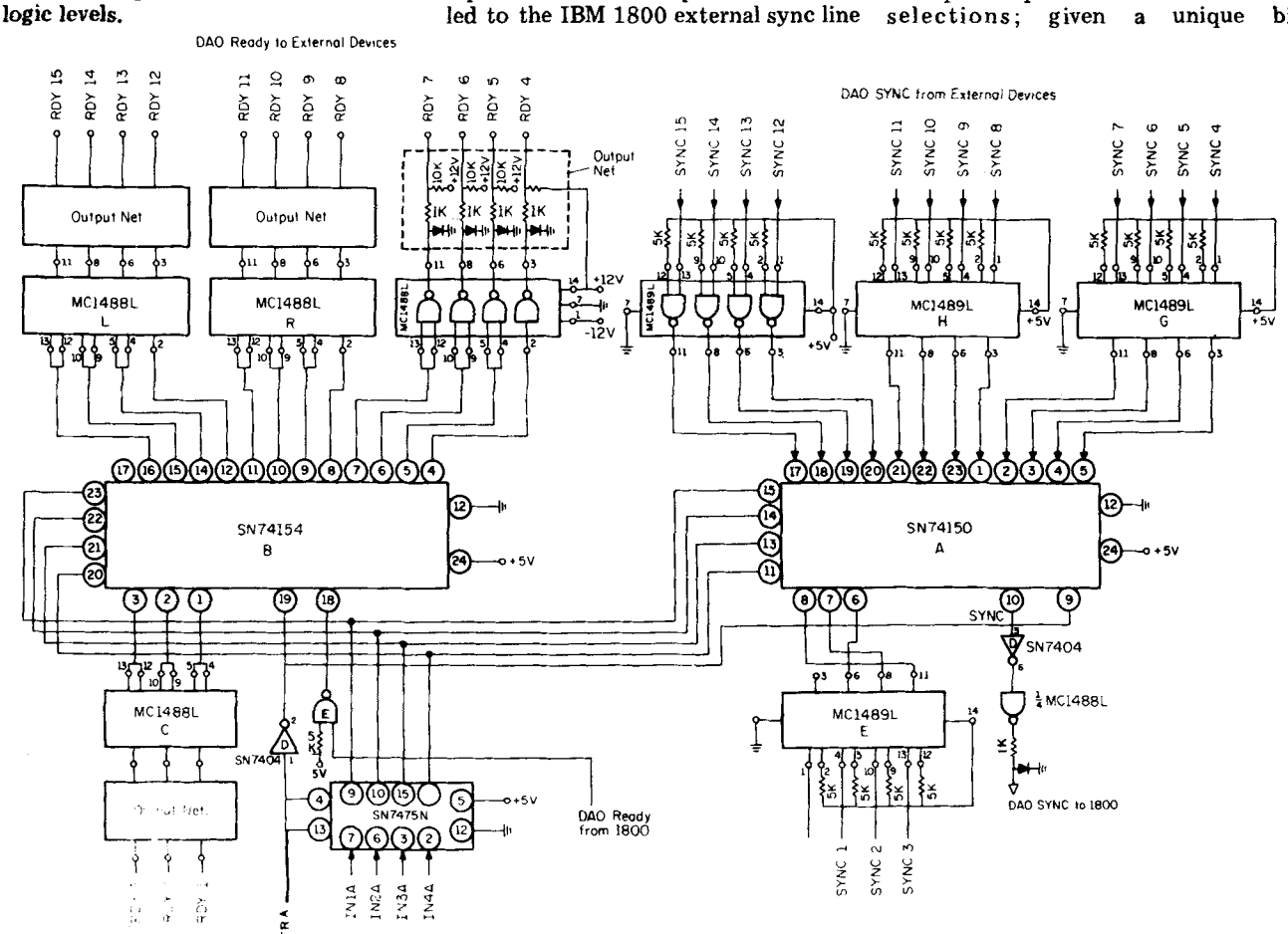

Fig. 2. Circuit diagram of the instrument. The SYNC and RDY lines are to and from external devices. Lines labeled IN1A through IN4A carry the address selection information and are derived either from the 1800 electronic contact operate lines or from front panel switches, as shown in Fig. 3.

onfiguration on these lines, one of he 15 "input" lines is "connected" to he "output" lines. Integrated circuits re also used for level shifting: the MC1489L shifts IBM 1800 levels (−12 o 0 V) to TTL levels (0 to +5 V). The MC1488L shifts TTL levels to 1800 evels.

As shown in Fig. 2, the "ready" ignal from the IBM 1800 is converted o TTL levels by the MC1489L chip. This signal is applied as input to the demultiplexer (SN74154). The demultiplexer passes the "ready" signal o the output line whose address is oaded in quadruple latch (SN7475). This output is level-shifted to TTL level by MC1488L before it is sent as a "ready" signal to the device whose address is loaded in the SN7475. The "sync" signal generated by the selected device is level-shifted by the MC1489L chip before it is applied at the input of the multiplexer (SN74150). The multiplexer passes this input to its output line, where it is level-shifted to IBM 1800 logic level and sent to the computer as a "sync" signal.

Address selection logic is implemented using the SN7400 IC chips. A front panel switch selects between "manual" and "automatic" operation. In the manual mode, the address bits are derived from four front panel switches; in the automatic mode, address bits are supplied by the 1800's ECØ register. Figure 3 presents the details of this logic. The inputs at the A or B gates appear at the outputs of the C gate, depending upon the signal on the "test and normal mode line." In the test (manual) mode, the channel address selected by the switches (IN1S, IN2S, IN3S, IN4S) appears at the output, whereas in the normal (automatic) mode, the channel address is selected by the computer-controlled switches (i.e., IN1, IN2, IN3, IN4) and appears at the output. These addresses are loaded into the quadruple latch (SN7475) of Fig. 2 by XFRA signal of device address select logic, which is generated by XFRS or the XFR inputs of test and manual mode select gates.

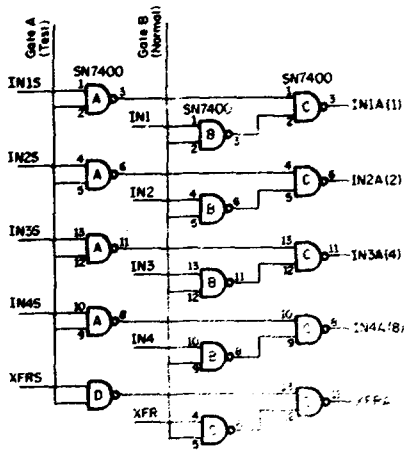

Fig. 3. Address selection logic network. The four address selection lines to the multiplexers can be derived either from front panel switches (IN1S through IN4S) or from the electronic contact operate lines of the 1800 (IN1 through IN4). At any one time, either the Gate A or the Gate B lines are "active," thus enabling the selection of the address from either the switches or the computer. The address selection network is latched on by the XFRA signal, which also can be obtained either from a front panel switch or the computer.

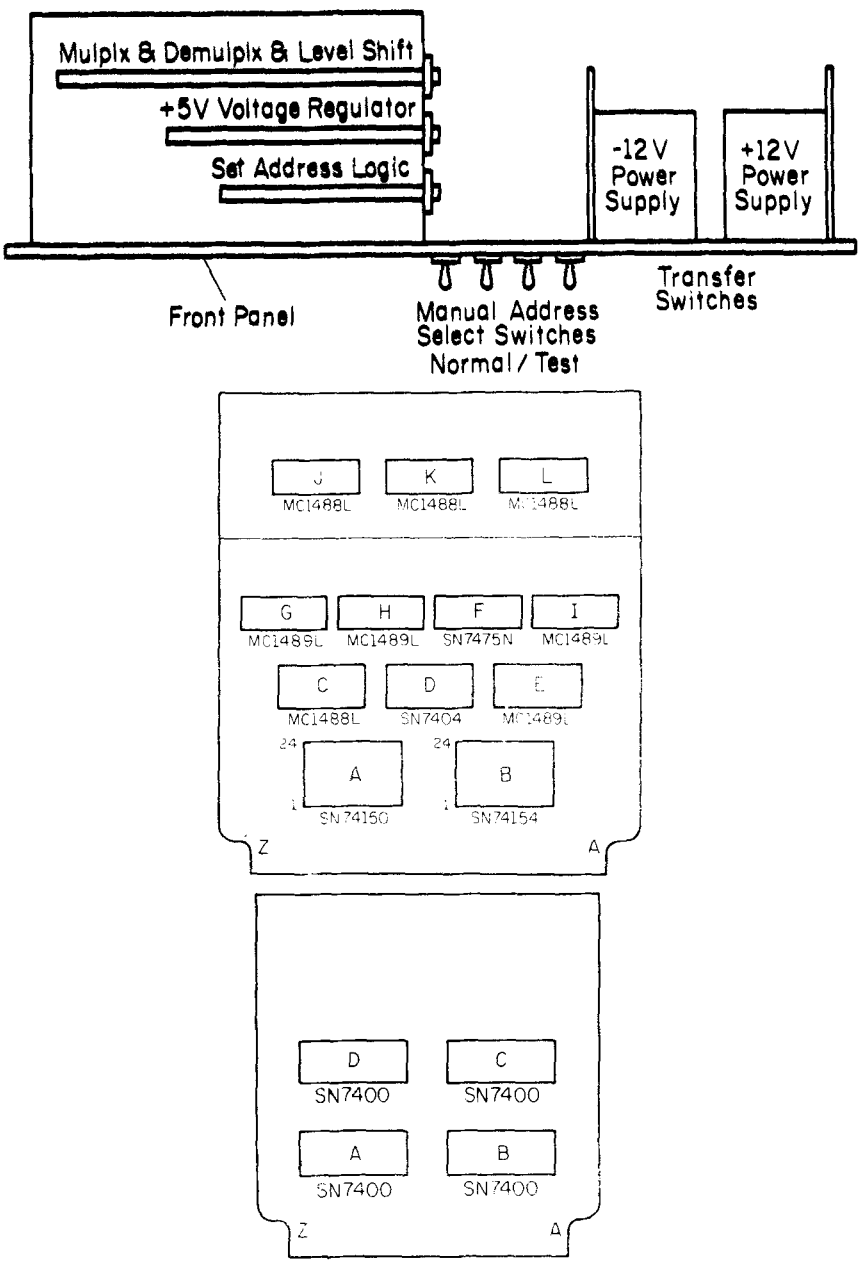

Fig. 4. (a) Top view of unit representing the physical location of power supplies and function switches. (b and c) The card layout of the multiplexer and demultiplexer cards as well as the address selection logic.

The entire circuit is mounted on three cards, as shown in Fig. 4a. The cards are functionally separated to facilitate service. One card implements the multiplexing and demultiplexing logic, one card the address selection logic, and the third serves as a +5-V voltage regulator. Figures 4b and 4c present the layout of the IC chips on the cards.

Power is derived from two supplies, −12 and +12 V (Elexon Inc. Type OLV 15). An integrated voltage regulator with "pass" transistor is used

to obtain the +5 V required for the TTL circuits.

Various sync and ready lines are available on the rear panel as screw-down terminals.

COSTS

Integrated circuit prices vary considerably with the quantity purchased. Most large organizations have (or can have) arrangements that allow them to pool all their purchases so that the individual investigator can obtain large-quantity discounts when buying individual IC chips. Table 1 lists the individual chip prices (as of summer 1971).

Construction of the unit is quite simple and involves little more than careful wiring of the IC pins according to instructions and the preparation of the mounting box. In our case, it took a fairly inexperienced technician 2 days to complete the job.

DISCUSSION

The unit discussed above is now in operation and is functioning in a satisfactory manner. At the present time, its primary function is to allow both the Datawest digitizer and the Versatec printer to be connected to the computer. In jobs in which only one or the other is required, the operator selects the appropriate device on the front panel of the multiplexer. When the two devices are required within a job, the program can select the appropriate device by setting the appropriate bit configuration in the ECO bits allocated to the purpose. (Note that the cost of dedicating four ECO bits to the purpose should be included in the cost estimate of the multiplexer.)

Table 1

	Item	Price
4 Each	MN1488L	$ 22.00
4	MC1489L	16.00
1	SN74150	2.70
1	SN74154	2.23
1	SN7475N	.74
1	SN7404	.24
4	SN7400	.20
1	−12V Power Supply	25.00
1	+12V Power Supply	25.00
Assorted Components (resistors, capacitors, etc.)		10.00
Assorted Hardware (3 circuit cards, mounting plugs, switches, etc.)		25.00
	Total	$129.11

As presented above, the multiplexer will operate with a single data channel only. Thus, when operating with the digital output channel, it is not available for the digital input channel. It is, in fact, trivial to add a multiplexing stage that would multiplex between pairs of synchronization lines to allow several data channels to use the same device. We did not find this necessary, simply because the external devices require only a single pair of synchronization signals that are shared between the input and the output. The multiplexer is, therefore, associated with the *output* channels.

While this communication is addressed primarily to IBM 1800 users, we feel it might have a more general interest. First, the need to share the unique lines of an expensive device among a series of satellite devices is not uncommon, and this multiplexer can be utilized for other purposes (with the possible elimination of the level shifting networks). It is also, we feel, useful to bring to the attention of the behavioral researcher, or at least to underline for these researchers, the immense flexibility currently available in integrated circuits logic. Psychologists have for some time been adept at the use of logic modules. Relay switching networks have given place to major families of RTL logic modules. The standard logic modules used in the psychology laboratory (BRS, Massey Dickinson, Iconix, etc.) are all characterized by the −12 V to ground logic levels. They usually provide reliable operation at a relatively low cost. It is, therefore, unlikely that these will be completely displaced in the near future. However, these units have two major disadvantages. First, they are incompatible with the widely used TTL logic levels. As more and more devices on the market are TTL devices, one is faced with an ever-increasing demand for level shifting and other compatibility maneuvers.

A more serious drawback of the discrete logic approach is that whenever logic circuits of even modest complexity are required, the networks become cumbersome, difficult to program, and expensive. It is the case that integrated circuits are currently available which can implement complicated circuit and logic functions on an individual chip.