Correction to: A novel FPGA-based test-bench framework for SDI stream verification

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The original article can be found online at https://doi.org/10.1186/s13640-020-00515-5.

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Following publication of the original article [1], the authors identified a few errors in the published article.

1. Body text contains incorrect sentence - in a simulation, it is possible to analyze the different frequency rates, but it is missing a test generator able to communicate with transceiver. It should be corrected to - in a simulation, it is possible to analyze the different frequency rates, but it is missing a test generator able to communicate with the DUT through the transceiver

2. The Figs. 11 and 12 had been inverted. Correct Figs. 11 and 12 with captions should look as per below:

The original article [1] has been corrected.

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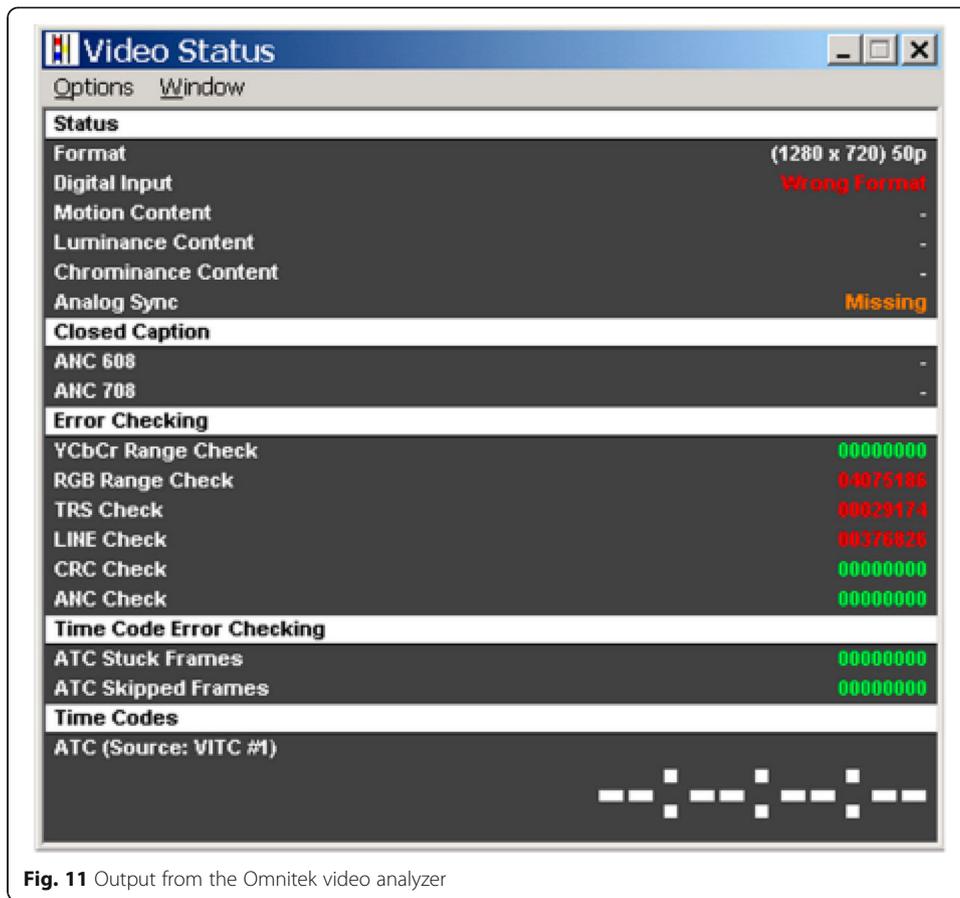
Fig. 11 Output from the Omnitek video analyzer
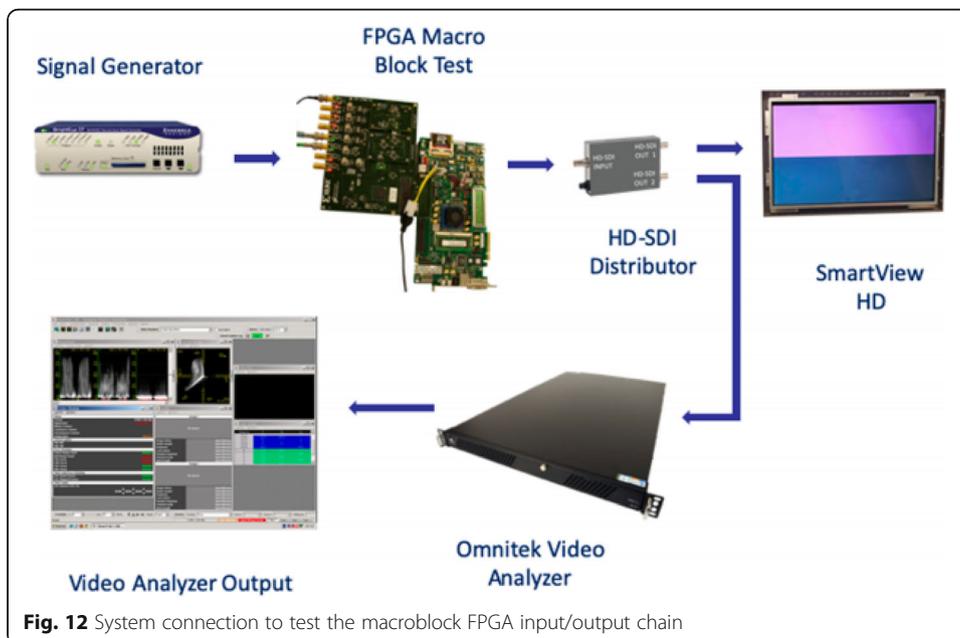
Fig. 12 System connection to test the macroblock FPGA input/output chain

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Reference
1.   G. Conti et al., A novel FPGA-based test-bench framework for SDI stream verification. J. Image Video Proc. **2020**, 31 (2020). https://doi.org/10.1186/s13640-020-00515-5