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Nanoelectronic COupled problems solutions - nanoCOPS: modelling, multirate, model order reduction, uncertainty quantification, fast fault simulation

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Abstract

The FP7 project nanoCOPS derives new methods for simulation during development of designs of integrated products. It covers advanced simulation techniques for electromagnetics with feedback couplings to electronic circuits, heat and stress. It is inspired by interest from semiconductor industry and by a simulation tool vendor in electronic design automation. The project is on-going and the paper presents the outcomes achieved after the first half of the project duration.

Keywords: multirate; model order reduction; co-simulation; uncertainty quantification; power-MOS devices; RF-circuitry; bond wires; coupled problems; multiphysics; fault simulation

1 Introduction

Designs in nanoelectronics often lead to large-size simulation problems and include strong feedback couplings. Industry demands the provisions of variability to guarantee quality and yield. It also requires the incorporation of higher abstraction levels to allow for system simulation in order to shorten the design cycles, while at the same time preserving accuracy. The nanoCOPS FP7 project addresses the simulation of two technically and commercially important problem classes identified by our industrial partners (NXP Semiconductors, ON Semiconductor, ACCO Semiconductor, and MAGWEL):

- **Power-MOS devices**, with applications in energy harvesting, that involve couplings between electromagnetics (EM), heat and stress, and
- **RF-circuitry** in wireless communication, which involves EM-circuit-heat coupling and multirate behaviour, together with analogue-digital signals.

To meet market demands, the **scientific challenges** are to:

- create efficient and robust simulation techniques for strongly coupled systems, that exploit the different dynamics of sub-systems within multiphysics problems and that allow designers to predict reliability and ageing;
- include a variability capability such that robust design and optimization, worst case analysis, and yield estimation with tiny failure probabilities are possible (including large deviations like 6-sigma);
- reduce the complexity of the sub-systems while ensuring that the operational and coupling parameters can still be varied and that the reduced models offer higher abstraction models that are efficient to simulate.

Achieving solutions to these challenges has considerable **industrial impact**. The overall **objective** of nanoCOPS is to advance a methodology for circuit-and-system-level modelling and simulation based on best practice rules to deal with **coupled electromagnetic field-circuit-heat problems** as well as **coupled electro-thermal-stress problems that emerge in nanoelectronic designs**. The new methods developed are robust and allow for **strong feedback coupling** when integrating systems to increase the performance of both existing devices and when integrating systems to produce new devices.

First outcomes have been reported in [1, 2]. The project is on-going and the paper presents the outcomes achieved after the first half of the project duration. Recently, at the DATE-2016 conference in Dresden, Germany, we gave dedicated presentations to designers and to engineers with backgrounds in mathematics and in electronics [3–7]. On the project website http://www.fp7-nanocops.eu/ special videos have been made available. Here also more publications can be found. The current paper addresses mathematicians and points out how mathematics as essential ingredient for innovation is transfered for successful use in industry.

With the new techniques it is possible to efficiently analyze the effects due to **variability**. Our methods are designed to solve **reliability** questions resulting from **manufacturability**. They facilitate robust design as well as enable worst case analysis. They can also be used to study effects due to ageing. **Ageing** causes variations in parameters over a long-term period, which cannot be predicted exactly and thus are typically uncertain. The challenges for an Integrated Circuit (IC) are that each device has its own electrical and thermal conditions, which are changing over time (due to ageing, for example). Here, each device has its own required life-time.

Novel **Model Order Reduction** techniques, developed here for the fast repeated simulation of the coupled problems under consideration, are applicable to both coupled systems and parameterized sub-systems. As such they are an essential ingredient for the Uncertainty Quantification.

In summary, our **solutions** are

- advanced co-simulation/multirate/monolithic techniques, combined with envelope/wavelet approaches;
- new generalized techniques in Uncertainty Quantification (UQ) for coupled problems, tuned to the statistical demands from manufacturability;
- enhanced, parametric Model Order Reduction techniques for coupled problems and for UQ.

All the new algorithms produced are **implemented and transferred** to the SME partner MAGWEL. **Validation** is conducted on industrial designs provided by our industrial partners. These industrial end-users give feedback during the project life-time, contribute to

Table 1 Partners in nanoCOPS

Abbr.	Partner
BUW	Bergische Universität Wuppertal, Germany (coordinator)
HUB	Humboldt Unversität zu Berlin, Germany
TUD	Technische Universität Darmstadt, Germany
UGW	Ernst-Moritz-Arndt-Universität Greifswald, Germany
FHO	FH OÖ Forschungs- und Entwicklungs GmbH, Hagenberg im Mühlkreis, Upper Austria, Austria
KUL	Katholieke Universiteit Leuven, Belgium
BUT	Vysoké učení technické v Brně, Brno University of Technology, Czech Republic
MPG	Max Planck Institute for Dynamics of Complex Technical Systems, Magdeburg, Germany
NXP	NXP Semiconductors Netherland B.V., Eindhoven, The Netherlands
ONN	ON Semiconductor Belgium, Oudenaarde, Belgium
MAG	MAGWEL NV, Leuven, Belgium
ACC	ACCO Semiconductor, Louveciennes, France

measurements and supply material data as well as process data. A thorough comparison to **measurements** on real devices is being made to demonstrate the industrial applicability.

Our consortium brings together extensive R&D experience in nanoelectronic IC simulation and complementary areas of expertise. It includes seven universities, one research institute, two large-scale semiconductor companies, and two SMEs, see Table 1.

2 Progress and results

In this section we give an impression of outcomes achieved in the first half of the project duration. We refer with the abbreviations in Table 1 to the various project partners.

2.1 Simulation environment

Electronic devices consist of a large number of components. Many parts are accurately described by a circuit model, whereas semiconductor parts and configurations suffering from electromagnetic interference necessitate the use of field models. The overall behaviour of the device needs to be simulated by a field-circuit coupled method. Improvements on such coupled techniques indirectly lead to more reliable and better integrated devices. In order to be able to incorporate the mutual electromagnetic influence of neighboring elements (e.g., cross talking), one needs refined models based on a sufficiently exact discretization of the full Maxwell equations. An interface model for such refined models was derived that can be used for lumped circuit net lists.

A main result, through joint effort by **MAG**, **HUB**, **FHO**, **TUD**, was the development of a simulation environment, which both enables the co-simulation [8, 9] and monolithic/holistic simulation of a circuit/device system [6] or electrical-thermal systems [10], see Figure 1 and Figure 2. The interface, both linear and nonlinear, couples software modules from academia to the device and electromagnetic field simulator from MAGWEL, offering flexibility in adapting modules and allowing for different time integration procedures. In this way, coupling of electronic circuits with electromagnetics and with semiconductor material is achieved. It also allows for state-space formulations of subparts to which Model Order Reduction can be applied. The interface treats the space discretization in the field simulator and generates a system of Differential-Algebraic Equations (DAEs). Especially, when including semiconductor material, large differences of magnitude made careful scaling during the assembly essential to guarantee that the overall system was stable [11, 12].

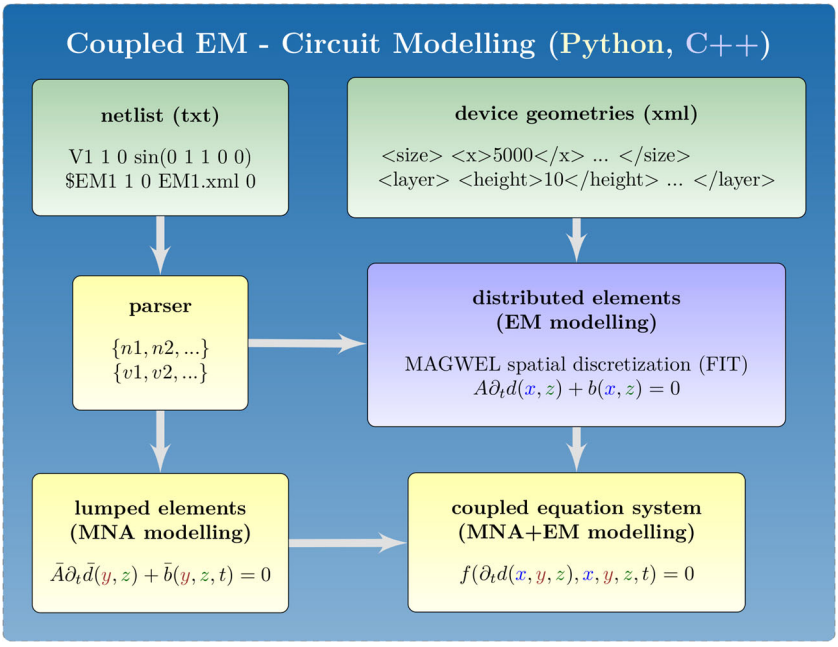


Figure 1 Coupled modelling. Set up for modelling coupled problems involving electromagnetics and circuit equations. Emphasis was made to cast outcomes in terms of Differential-Algebraic Equations.

2.2 Bondwire modelling and simulation

Nowadays integrated circuits (ICs) are important components of daily life. Moreover, the ever tightening specifications imposed on modern integrated circuits (ICs) by the semiconductor roadmap demand more energy-efficient chips which become smaller and smaller in size. Bond-wires are commonly used to connect the chip and the pins during device assembling. These wires are heated up due to Joule effects and their temperature. Figure 3 shows a diagram of a classic IC lead-frame package. **TUD** and **ONN** have focused an improved electro-thermal formula that is the basis for a bondwire calculator for **ONN** [13]. Bondwire temperature can increase substantially since the electric power is supplied through the wires. If the wires cannot properly dissipate this power, then permanent damage will occur to the wires and surrounding material. A mathematical formula has been developed that improves the prediction of this heating compared to known models from literature [14].

Figure 4 depicts a simplified thermal problem upon which the model is built. The rectangular shape of the package compound is retained and suitable boundary conditions (BCs) are used; (1) adiabatic on the rightmost wall except on the wire portion. This facilitates the inclusion of the lead into the model; (2) iso-thermal on the leftmost and bottom walls amounting to the chip and die-attach temperatures; (3) convective on lateral and upper walls; (4) thermal radiation on the wire surface. The temperature dependence of the wire's thermal and electrical conductivities is also included. The heat equation is solved by means of an *ad-hoc* linearization which involves the compound heat equation and its heat kernel [15], viz.

$$T_{\mathrm{w}}(y,t) \cong T_{\mathrm{o}} + \frac{\sqrt{2\alpha_\kappa \widetilde{\theta}_{\mathrm{w}}(y,t) + 1}}{\alpha_\kappa} - \frac{1}{\alpha_\kappa}. \tag{1}$$

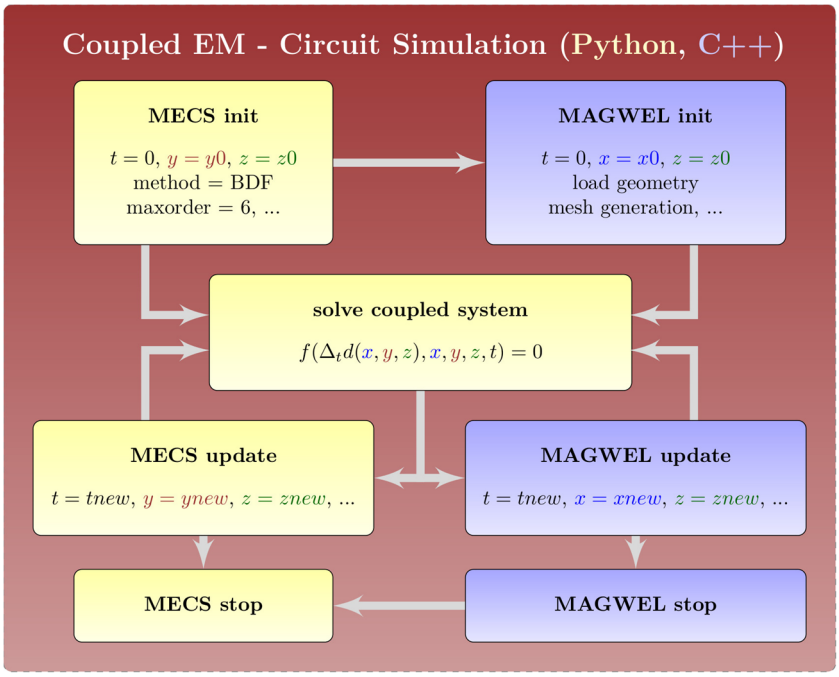
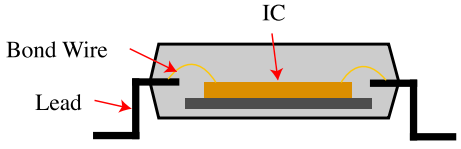


Figure 2 Coupled simulation. Set up for simulating coupled problems involving electromagnetics and circuit equations. Here there is integration between a circuit simulator (MECS) and an EM-solver. Note that the MAGWEL software provides contributions to specific equations as well as associated Jacobian values.

Figure 3 Bond wire. Classic IC lead-frame package.



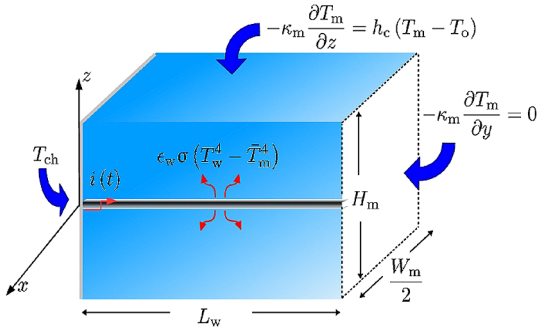


Figure 4 Bond wire. Bond-wire heat transfer problem.

Above, T_w is the wire temperature, T_o is the reference (ambient) temperature, α_κ is the temperature coefficient of the wire thermal conductivity, and $\widetilde{\theta}_w$ is an auxiliary variable.

Several numerical tests for wires of gold, copper, and aluminium have been performed with data provided by **ONN**. Numerical verification has been carried out with CST Multiphysics Studio™, and a good agreement has been corroborated. Figure 5 shows the esti-

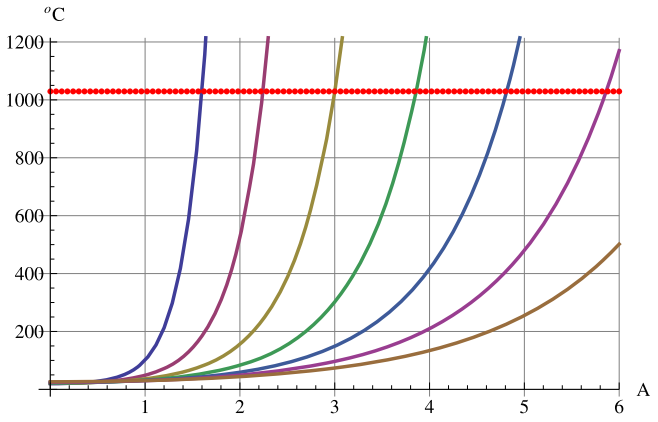


Figure 5 Bond wire. Au-wire current capacities for several diameters and a fixed length. The plotted temperature is at the wire mid-point, where the hottest point is expected.

mated current capacity (temperature vs current amplitude) for a gold wire after 50 ms. The formula retains important geometrical parameters defining the package, which adds high flexibility. This reduces the over-design of the wires during fabrication. The evaluation of this formula is computationally inexpensive such that time-consuming 3D simulation can be avoided. However, a coupling of the bondwire model to a 3D simulator is necessary if the integration in the overall system behaviour should be simulated. Thus, **TUD** also implemented a nonlinear in-house simulation code based on the Finite Integration Technique (FIT) to analyze the coupling before transferring the concept to partner **MAG** [4]. **ONN** aims to use the algorithm within a GUI (Graphical User Interface).

ONN and **BUT** made measurements of DC and dynamical fusing of bondwires [16]. **ONN** fabricated test chips (SOIC package so far), where the individual bondwires with different lengths, diameters and materials have been encapsulated. **BUT** prepared a complete methodology and experimental setup to do such investigations.

The setup (hardware tester and MATLAB GUI) allows measurements of all six bondwires in one IC package. The tester consists of the 6 independent channels, the 6 driving stages, the 6 Kelvin probe sensing stages, the demultiplexing core for the driving stages (specification of address of the bondwire) and the multiplexing core for the Kelvin probe sensing stages.

The block structure, the single channel operation and photographs of the final hardware solution are shown in Figure 6, Figure 7 and Figure 8. The frequency limitation of the measurement setup is about 500 kHz (limits of the used MOS power-switches and PCI card). The software part of the project consists of two executable MATLAB scripts with a GUI. MATLAB software is also used for the generation of testing sequences and signals that drive the tester. Finally, the measurements have been used to validate the bondwire formula.

2.3 Electro-thermal coupled simulation

MAG and **ONN** co-operated on electro-thermal simulation in order to guarantee industrial acceptance. A highlight of this work is that the electro-thermal simulation tool is very flexible concerning the various device technologies since the nanoscale transistor architecture is incorporated via compact models. Therefore, it is possible to couple the large-

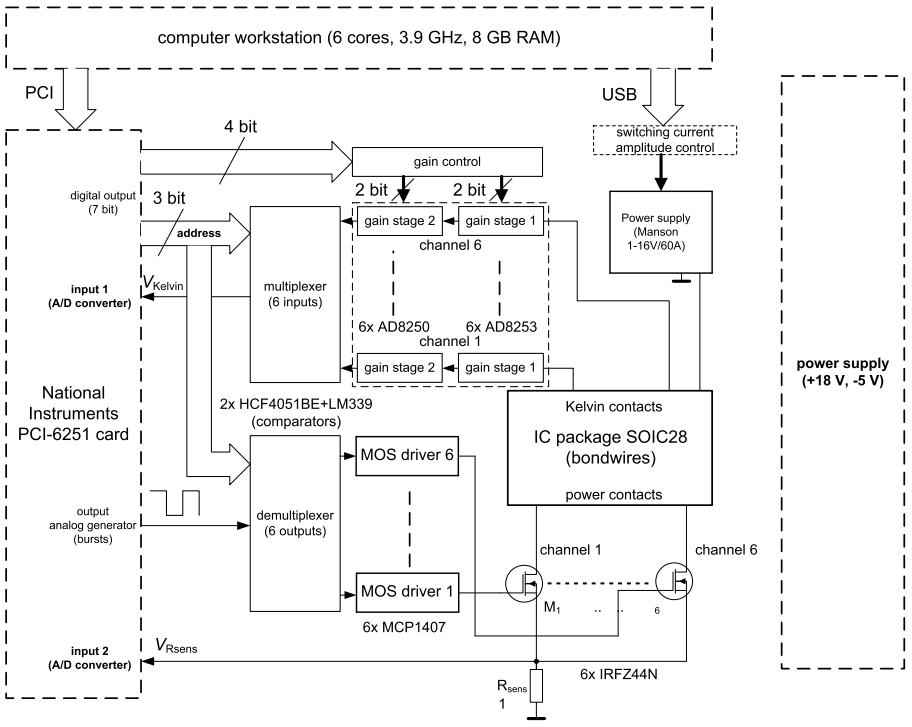


Figure 6 Bond wire. Final hardware solution of the bondwire tester prototype: overall block structure.

scale (millimeter) structures and the small-scale (sub-micron) of the finger architecture in a single simulation. The computation deals with the coupling of the electrical response and with the thermal response in first-principle field solving. Figure 9 illustrates today's capabilities [10].

2.4 Multirate simulations

In coupled problems one often encounters multiscale differences (in space) and large variations in dynamics in time-domain: multirate effects [17]. In this book especially partitions in space with different dynamics lead to couplings between subsets of DAEs. A careful formulation of the coupling is key in being able to guarantee convergent dynamical iterations in a co-simulation. In [9] the partition between physical quantities (electromagnetics, heat) was exploited to study this convergence.

A different kind of multirate occurs in electronic circuits involving oscillators, where a large difference between frequency components can be observed. In the time domain we see a high-frequency carrier signal that is moduled by an envelope signal (in case of amplitude modulation), or where the frequency is modulated (frequency modulation). An additional effect is the occurrence of sudden steep rises and fall of signals. **FHO** developed a multirate envelope time-integration technique, which combines decompositions along two time scales, using nonuniform biorthogonal spline wavelets [18]. Emphasis is on performance optimization, including adaptive grids, iterative linear solvers for huge problems (e.g. preconditioned GMRES), optimization of the evaluation of lumped devices (e.g. BSIM3 and BSIM4, MEXTRAM, etc.). Figure 10 shows the divider block diagram for a PLL in the 5.6 GHz ISM band, employing the silicon germanium technology of IHP (a research center funded by the German government). The simulation of frequency dividers

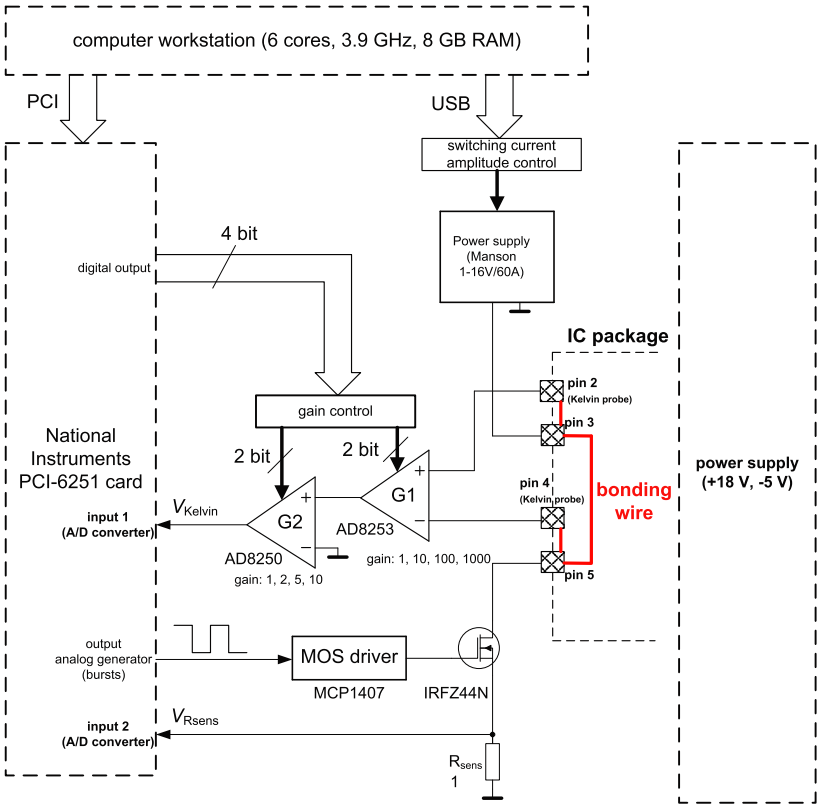


Figure 7 Bond wire. Final hardware solution of the bondwire tester prototype: single channel principle.

is a severe bottleneck for PLL simulation and for the multirate technique in general. In deriving Figure 11, adaptive methods were employed for the different stages of the divider. Table 2 shows the drastic improvement of the run time using adaptivity. No commercial circuit simulator provides this facility yet.

2.5 Parametric model order reduction

MPG and **MAG** developed efficient parametric/parameterized Model Order Reduction (pMOR) methods and techniques for fast simulation of electro-thermal coupled models [19, 20] and for fast Uncertainty Quantification [21] of nanoelectronic, electro-thermal models with random variables or stochastic processes. Given the system matrices at different values of the parameters or realizations of random variables, we extract system matrices which are independent of the parameters (random variables), so that parametric models can be constructed, and the parameters (random variables) symbolically appear in the model. Reduced-order models of the large-scale parametric models are obtained using parametric model order reduction techniques. For general complex geometries, like in Figure 12, an accurate, physical model in the form of heat transfer partial differential equations is required. The electrical transport is controlled by Ohm's law and the current continuity equation in conductive material

$$\nabla \cdot J = 0, \qquad J = \sigma(T)E. \tag{2}$$

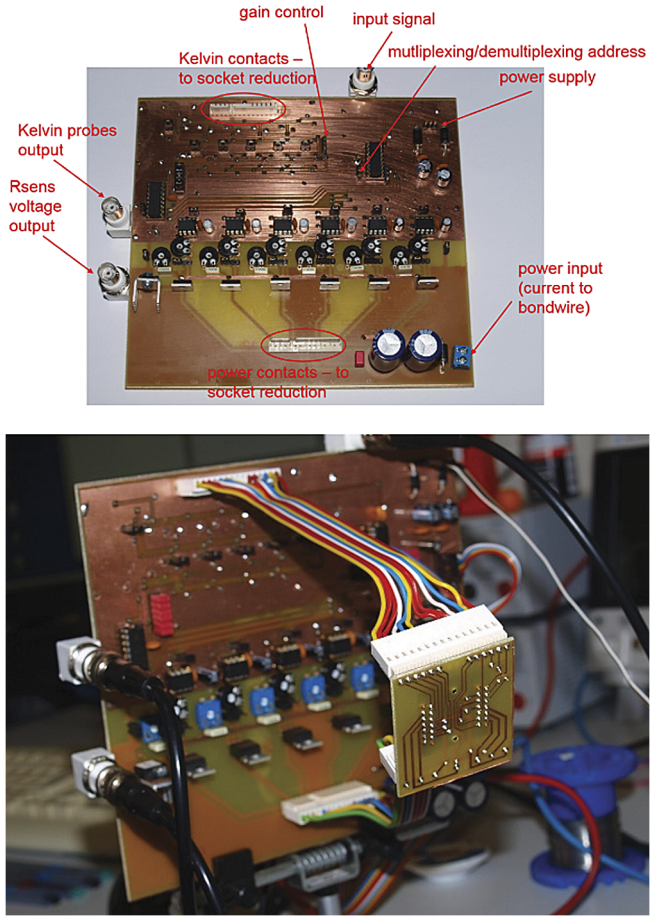


Figure 8 Bond wire. Final hardware solution of the bondwire tester prototype: final version of the PCB.

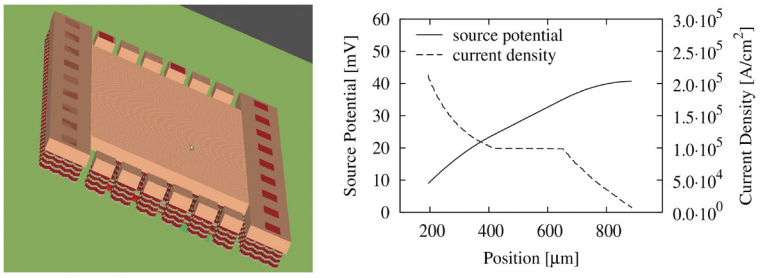


Figure 9 Power MOS transistor. Analysis of a power MOS (left figure) resulting into an asymmetric current density due to thermally induced conductance variations in the metallic interconnect (right figure).

The generated-energy transport is controlled by Joule's law

$$\frac{\partial U}{\partial t} = -\nabla \cdot Q + \Sigma, \qquad Q = -\kappa(T)\nabla T, \qquad U = C_V\big(T - T^*\big). \tag{3}$$

Of particular interest is the local heat generation, which is given by

$$\Sigma = E \cdot J = \sigma(T)(\nabla V)^2. \tag{4}$$

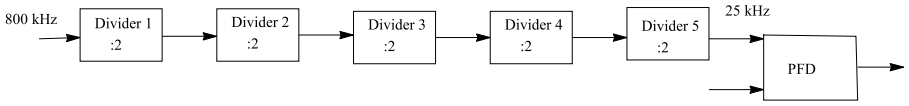


Figure 10 Divider block diagram. A divider block diagram for a PLL (phase lock loop) in the 5.6GHz ISM band (industrial, scientific and medical (ISM) radio band).

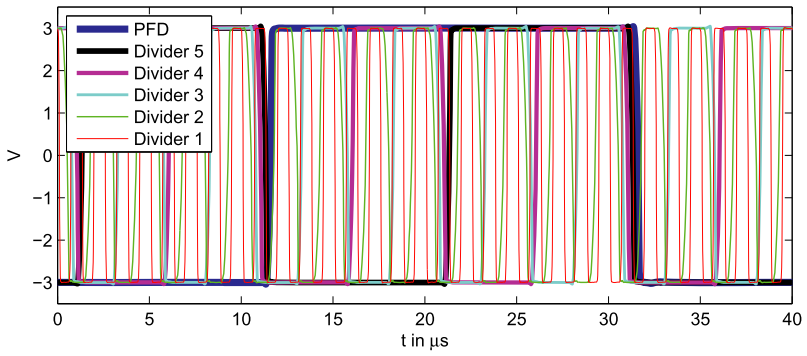
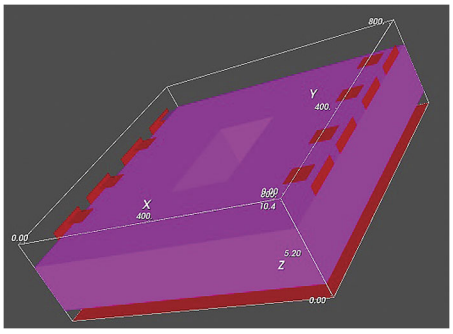


Figure 11 Multirate solution. The solutions show time-varying multirate behaviour, which was efficiently solved by the implementation of FHO.

Table 2 Performance summary multirate simulation

	Single grid	Multiple grids
Number of equations	130,000	85,000
Nonzeros in Jacobian	5×10^6	2.5×10^6
Assembly of linear system	4 s	2 s
Linear solve	8 s	4 s
Envelope analysis	5 h	37 min

Figure 12 A thermal package model (provided by MAG).



Here $\kappa(T)$ is the heat diffusion, C_V is the constant-volume heat capacitance of the material, which is also T-dependent and T^* is a reference or ambient temperature. The latter expression results in a non-linear relation (coupling) between the variables V, the electrical voltages, and the temperature variables, T. Spatial discretization (using the finite-element method, or finite volume method, like finite integration) of (2) and (3) results in a large-

scale system of ODEs in the form of

$$E\frac{dx(t)}{dt} = Ax(t) + x(t)^T \mathcal{F}x(t) + Bu(t), \tag{5}$$

where x is the state vector including the nodal voltages and nodal temperatures varying with time. The tensor $\mathcal{F} \in \mathbb{R}^{n\times n\times n}$ represents the non-linear character of the heat source Σ. Roughly speaking, $\mathcal{F}$ can be considered as a 3D array of n matrices. Each matrix is in $\mathbb{R}^{n\times n}$. The matrix $E \in \mathbb{R}^{n\times n}$ is a capacity matrix for both the electrical and the thermal part, and the matrix $A \in \mathbb{R}^{n\times n}$ is the conductivity matrix for both the electrical and the thermal part. Linear parametric models in state-space-form were constructed based on the discrete data provided by **MAG**, resulting from a finite-integration technique (FIT). As an example we consider a parametric thermal package model, see Figure 12. When considering meshes that are topologically equivalent for different package thicknesses p, the parametric dependence of the matrices as well as the matrices in the tensor $\mathcal{F}$ will take the form as

$$M(p) = M_0 + pM_1 + \frac{1}{p}M_2. \tag{6}$$

The second term in (6) originates from the linear dependence of dual areas corresponding to the cell edges perpendicular to the thickness, whereas the third term originates from dual areas associated to cell edges tangential to the thickness orientation.

If the parameter p symbolically appears in the model, the system in (5) becomes a parametric model,

$$E(p)\frac{dx(t,p)}{dt} = A(p)x(t,p) + x(t,p)^T \mathcal{F}(p)x(t,p) + B(p)u(t), \tag{7}$$

where the matrix $E(p)$, $A(p)$, $B(p)$ and each matrix in $\mathcal{F}(p)$ are in the form of $M(p)$. Some mathematical calculations are needed to extract the parametric system from the system in (5). However, the calculations are independent of the dimension of the matrices in (5), which makes the calculation very cheap and flexible [22].

Using a robust parametric model order reduction algorithm in [23], a reduced parametric model (8) with the same parametric structure as the full parametric model, in (7), but with much fewer equations, has been derived

$$\hat{E}(p)\frac{dz(t,p)}{dt} = \hat{A}(p)z(t,p) + z(t,p)^T \hat{\mathcal{F}}(p)z(t,p) + \hat{B}(p)u(t). \tag{8}$$

By replacing the full parametric system in (7) with the reduced model (8), much simulation time could be saved. Accurate reduced-order models (ROM) were derived for these linear parametric models. Structure preserving models with sufficient accuracy are obtained for nonlinear parametric coupled problems as well. We refer to Figure 13 for the results of the ROM. The relative error of the output produced by the ROM is of the order 10^{-11}. Furthermore, we have constructed a ROM for a Powercell electro-thermal model with size n = 925,286, and m = 408 inputs, l = 816 outputs. Simulation of such a large-scale system with numerous terminals is a hard task for commercial simulation software, e.g., Spectre. The simulation immediately breaks down due to out of memory. We proposed

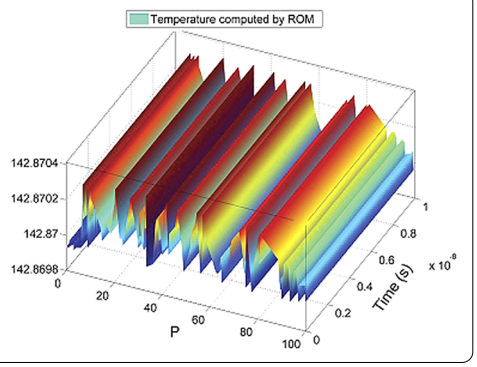


Figure 13 Simulation results after Model Order Reduction. Full order model state space $n = 8549$, ROM state space $r = 58$, amount of inputs 34 and outputs 68. Temperature as computed by the ROM.

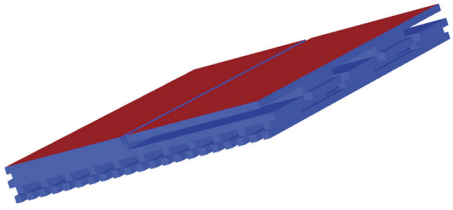


Figure 14 Power-MOS device (the back contact is not shown).

an efficient method: BDSM-ET [3], which uses the superposition principle to construct a ROM with block-wise sparsity. The size of the ROM is $r = 11{,}519$ and thus almost two orders of magnitude smaller than the Full Order Model (FOM). A most important feature is that the ROM is also much sparser than the ROM obtained using the standard method. With an error less than 10^{-5}, the thermal part of the ROM has been used together with Spectre, and validated to be efficient.

In developing pMOR methods for fast UQ of nanoelectronic, electro-thermal models with random variables or stochastic processes, we applied pMOR techniques to a Power-MOS device (Figure 14), provided by MAG, and obtained a parametric reduced order model (pROM) that is of high accuracy over a very large parameter range. We have embedded the parametric reduced model into the Stochastic Collocation Method [24], which proved to be both efficient and accurate.

Figure 14 displays the Power-MOS chip. Figure 15 shows the heating of the chip. We built an order-2 pROM for the order-1660 FOM of the electrical part, and an order-50 pROM for the order-11556 FOM of the thermal part. Figure 16 and Figure 17 depict the evolution of the 'maximal relative error at the outputs', which is defined as the maximal relative error at all outputs. When the system starts, the maximal relative error is high because the system is hardly heated up (exact values close to zero) and the thermal parts are dominated by modelling error and numerical error. However, as time elapses, the maximal relative error goes down to the order of 10^{-4} and therefore, the dominant physical properties are accurately captured over a large parameter range.

2.6 Uncertainty quantification

UGW, **BUW**, **MAG**, **TUD** worked on methods for Uncertainty Quantification and applied the approaches to address variations of material properties as well as in the geometry [25]. Apart from in-house software of **UGW** and **BUW**, interfacing with libraries from Sandia National Laboratories [26] was achieved. In order to demonstrate robustness of an

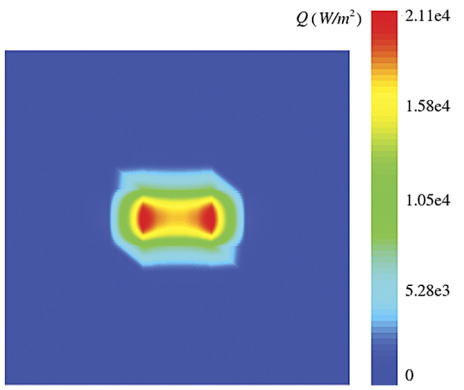


Figure 15 Power-MOS device. Heat flux density on the back contact at time $t = 10^{-6}$ s.

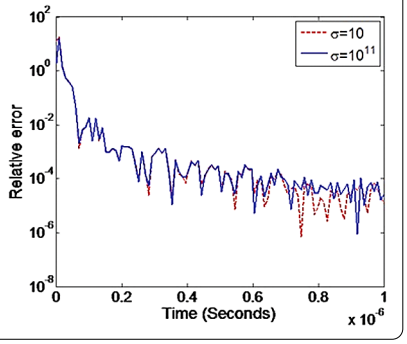


Figure 16 Rel. error at source. The evolution of the maximal relative error of the outputs for different values of the electrical conductivity $\sigma = 10, 10^{11}$ S/cm.

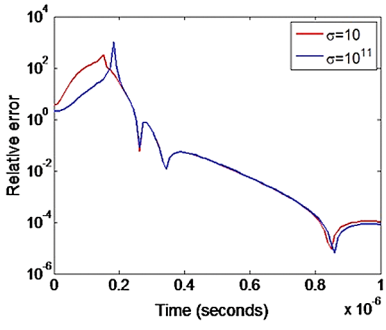


Figure 17 Rel. error at back contact. The evolution of the maximal relative error of the outputs for different values of the electrical conductivity $\sigma = 10, 10^{11}$ S/cm.

optimization algorithm under uncertainties, a Power Transistor Model was considered as a test example. We reduced the thermal instability by optimizing the geometry within the device layout, while taking both the conductive power losses and shape variations of source/drain into account. In [5] we focused on a shape/topology optimization problem of a power MOS device with three metal layers under geometrical and material uncertainties to reduce the current density overshoot. This problem, occurring in the automotive industry, yields a stochastic electro-thermal coupled problem. It is a multi-finger MOSFET power transistor with a stripe cell structure, which consist of several thousands of parallel channel devices. The source and drain contacts are located on the top metal finger of the design, as shown in Figure 18. A series of metal stripes and complex via patterns transport the current to drain and away from the sources of the individual channels. Consequently, the multi-dimensional current flow is governed by a coupled time-dependent system of

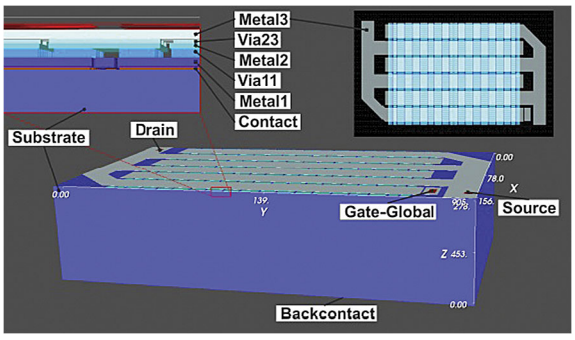


Figure 18 Power transistor. Power Transistor optimized to reduce power hotspots while taking geometrical variations into account.

stochastic Partial Differential Equations (PDEs). Its solution enables to investigate the propagation of uncertainties through a 3-D model, which affect yield and performance of a power transistor. In particular as parameters $p(\omega) = [\sigma_3(\omega), W_2(\omega), C_\upsilon(\omega), V_\mathrm{D}(\omega), V_\mathrm{S}(\omega)]$ are taken, in which the conductivity of the Metal3 layer, σ_3, the thickness of the Metal2, W_2, and the thermal capacitance of the Via12, C_υ, and the drain and source contacts are considered, see also Figure 18. Here ω varies over some event space and the probability distributions of the parameters are predetermined. The PDEs are equipped with random Dirichlet boundary conditions that describe the potentials at the drain and source pads.

To reduce the current density overshoots in the area of the contact layer of the power device, as basic random-dependent cost functional

$$F(\upsilon) = w_1 \int_\mathrm{D} Q_\mathrm{e}\big[\upsilon, V(\upsilon)\big]\,\mathrm{d}x + w_2 \int_\Gamma h\big[V(\upsilon)\big]\,\mathrm{d}\gamma, \tag{9}$$

was taken, where the dissipation power Q_e is analyzed in the area of Metal3 layer $\mathrm{D} \subset \mathbb{R}^3$, and the source voltage term h is represented by the random Dirichlet boundary condition in the area of the source and drain pads $\Gamma \subset \mathbb{R}^2$. The variable υ is defined as $\upsilon = (x, p(\omega))$, whereas the weights w_1 and w_2 refer to known a priori information about objectives.

For the robust optimization one considers a PDE-constrained minimization problem

$$\min_\upsilon \mathbb{E}\big[F(\upsilon)\big] + \eta\sqrt{\mathrm{Var}\big[F(\upsilon)\big]}, \tag{10}$$

where $\eta = 3$ was taken. The Stochastic Collocation Method, based on Polynomial Chaos Expansion (PCE) [24, 27], provided a response surface model to estimate the expectation $\mathbb{E}[F(\upsilon)]$ and the standard deviation $\sqrt{\mathrm{Var}[F(\upsilon)]}$. Combining with a Topological Derivative Method, we could reduce hot spot phenomena in a robust sense, see Figure 19. The optimization results for a relevant nanoelectronics problem demonstrate that the proposed method is robust and efficient [5].

We finally remark that our implementations are also able to identify dominant parameter contributions to the variance when varying parameters [28].

As a separate action, **TUD** developed a GUI (Graphical User Interface) for Uncertainty Quantification to easily compare our UQ methods with Monte Carlo simulations and Worst Case Corner Analysis [29]. The last approach is very popular in the semiconductor

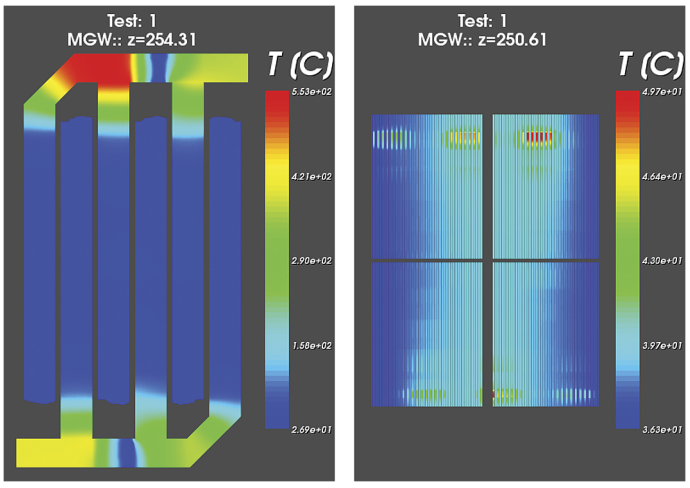
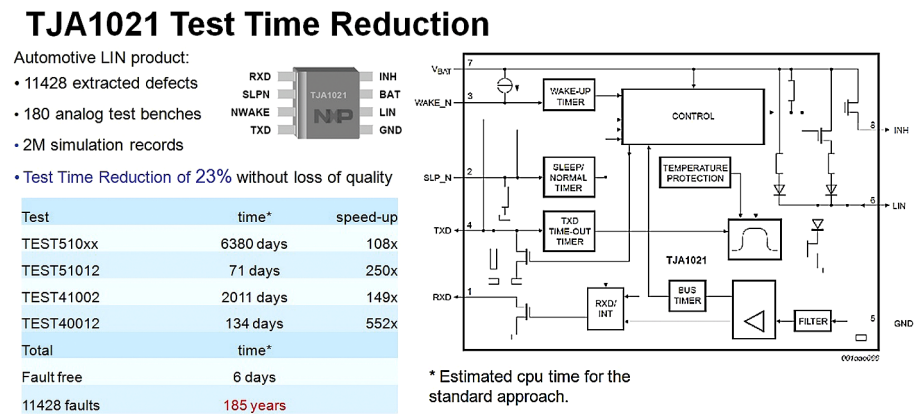


Figure 19 Power transistor. The pictures give a temperature distribution in the Metal3 layer and the Contact Layer for the structure after optimization (joint work by UGW, BUW, MAG).

industry because it is much faster than Monte Carlo. Our UQ implementation exploits sparse grid techniques and can easily deal with up to 20 independent parameters.

2.7 Fast fault simulation

NXP, **BUW** and TU Eindhoven developed a special algorithm for fast fault simulation in NXP's in-house circuit simulator Pstar. NXP's simulator is the best in the world for this functionality [7, 30]. Imperfections in manufacturing processes may cause unwanted connections (faults) that are added to the nominal, 'golden' design of an electronic circuit. When considering faults from the point of view of parameter variations this is well in the range of large deviations. In [30] the faulty elements are represented by adding linear conductivities to the circuit. The approach also works for analyzing the effect of additional linear capacitors. However, the main interest is in adding linear conductivities: thus $puv^T x(t,p)$, where $p = 1/R$, with resistance R, and given vectors u, v, to the system of circuit equations of which the solution becomes $x(t,p)$. By fault simulation we simulate all situations: a huge number of new connections of pairs of vectors (u,v) and each with many different values of p, up to the regime of large deviations, for the newly added element and comparing the result $x(t,p)$ at specific time points with the 'golden' solution $\tilde{x}(t) = x(t,0)$ of the fault-free circuit, corresponding with $p = 0$. If the deviation between $x(t,p)$ and $\tilde{x}(t)$ exceeds some threshold, the fault triple (u,v,p), is marked as detectable and is taken out of the list. We also consider 'opens' (broken connections). A strategy is developed to efficiently simulate the faulty solutions until their moment of detection. The hierarchical structure was enhanced, such that the hierarchical solver could deal with all new elements: note that some new connections may violate the original hierarchical structure of the golden circuit. A clever software solution was developed and is reported in [30]. By this, also the faulty problems could benefit from an enhanced form of hierarchical bypassing. Because each candidate fault is a low-rank modification of the designed circuit an hierarchical variant of the Sherman-Morrison formula was exploited. Fast fault simulation is achieved in which the golden solution and all faulty solutions are calculated over the same time step.



Test	time*	speed-up
TEST510xx	6380 days	108x
TEST51012	71 days	250x
TEST41002	2011 days	149x
TEST40012	134 days	552x
Total	time*	
Fault free	6 days	
11428 faults	185 years	

Figure 20 Fast fault imulation. Speed up in fast fault simulation for the TJA1021 chip.

The results are stored in a database. This database is of help to first externally diagnose a faulty IC and to identify the candidate circuit submodels where the fault may have happened. After that the IC can be studied further internally. This can help to improve next productions. Moreover, the collection of simulations can also be helpful as a priori check before layouting. **NXP** can identify locations on a chip that are probably affected by tiny manufacturing accuracies, which case faulty behaviour at predefined time points for measurements.

Inclusion of sensitivity analysis brought speeds up in CPU time of a factor 20 or more. See Figure 20 for an indicative result. Later invoking of faults gave an additional order of magnitude in speed up. By this reduction of simulation time candidate faults could be detected that would have been impossible otherwise because of excessive CPU time [7].

Note that essentially one is looking to the weak spots in the circuit. In our approach the manufacturing process is the immediate cause of the problem. However it can also show up later, due to effects of ageing of the design, or by stress effects due to heating. It is also related to other network problems, e.g., in analyzing traffic behaviour in a city when suddenly a road is blocked, or when a new connection pops up. Our approach can be extended to energy distribution networks, sewage systems, and even to networks that are not constant of size in time.

This algorithm also offers interesting ingredients to combine with Uncertainty Quantification.

2.8 Test examples, measurements

The industrial partners **NXP**, **ONN**, and **ACC** did provide various test examples. The test cases cover realistic-size power MOS devices at constant temperature and in ET coupling mode; a driver chip with multiple heat-sources; a smart power driver test chip with thermal sensor; an 8-shaped inductor with surrounding circuitry; a fast and reliable model for bondwire heating; RF and electro-thermal simulations; reliable RFIC isolation under uncertainty (for floor planning and grounding strategies; this involves on-chip coupling effects, chip-package interaction, substrate coupling and the so-called co-habitation factor); multirate circuit examples; silicon test chips for step-by-step testing and validation; transmission line and baluns. All these are found in our industrial problem classes described in the introduction. **ACC** has prepared several designs, made simulations and realized test

boards. They served for step by step study, for comparison to measurements and for validation of the enhanced MAGWEL software, in close cooperation with **BUT**, **NXP** and **ONN**.

As simple example, we mention here test chips that include passive structures (inductances, capacitances, baluns, resonators). These structures, that are easily measurable, are used to validate further EM extraction and model reduction. Simulated results are compared to measurements, EM solver extraction and then with extraction plus netlist reduction in terms of accuracy, memory usage and time simulation.

3 Conclusion

The unique combination of the nanoCOPS consortium allows to already report the following intermediate, innovative highlights halfway the project, to which all partners have contributed.

- The coupling interface with the MAGWEL software has been improved, tested and is operational.
- Successful large-scale EM-heat simulation was achieved.
- Grid-adaptive multirate circuit simulation was established.
- Model Order Reduction was successfully applied to coupled EM-heat problems.
- Accurate bond wire modelling for fast usage at industry was demonstrated and was validated by measurements.
- Uncertainty Quantification was applied to variations of material parameters and geometry and was used in robust topology optimization. Apart from the topics, this at best demonstrates the robustness of the integrated software - to achieve optimization one addresses all parts of the codes.
- Innovative methods for improving yield as well as to identify faults were derived.
- Advanced measurements environments have been set up both at academia and at industry.
- Outcomes have been presented at conferences. Joint papers have been published in various journals.
- Interaction between academia and industrial partners addressed a broad range: test examples, new algorithms, implementations, practical use of new methods, ways to improve measurements.

The focus in the second half of the project is on further validation and demonstration of the methods by applying them to the broad range of IC building blocks. Together with the industry partners methodologies are defined how best to use the methods. All three industrial partners started work on reliability and the impact of ageing. Also steps to yield optimization have been developed. Techniques with adjoint approaches are currently introduced. Also inverse problems are addressed. Presentations will be given at SCEE-2016, Scientific Computing in Electrical Engineering, http://wwwdev.ricam.oeaw.ac.at/events/conferences/scee2016/.

Competing interests
The authors declare that they have no competing interests.

Authors' contributions
Sections 1 and 3 are joint responsibility for all authors. In Section 2 the partners' contributions are clearly identified in each subsection.

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