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Low-power memristors based on layered 2D SnSe/graphene materials

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ABSTRACT **The emerging two-terminal memristor with a conductance-adjustable function under external stimulation is considered a strong candidate for use in artificial memory and electronic synapses. However, the stability, uniformity, and power consumption of memristors are still challenging in neuromorphic computing. Here an Au/SnSe/graphene/SiO_2/Si memristor was fabricated, incorporating two-dimensional graphene with high thermal conductivity. The device not only exhibits excellent electrical characteristics (e.g., high stability, good uniformity and a high R_{OFF}/R_{ON} ratio), but also can implement biological synaptic functions such as paired-pulse facilitation, short-term plasticity and long-term plasticity. Its set and reset power values can be as low as 16.7 and 2.3 nW, respectively. Meanwhile, the resistance switching mechanism for the device, which might be associated with the formation and rupture of a filamentary conducting path consisting of Sn vacancies, was confirmed by high-resolution transmission electron microscopy observations. The proposed device is an excellent candidate for use in high-density storage and low-power neuromorphic computing applications.**

Keywords: graphene, SnSe, memristor, electronic synapse

INTRODUCTION

With the rapid development of science and technology, researchers have begun to pursue electronic products with efficient information processing and memory behavior similar to the human brain. The two-terminal memristor, which not only has a simple structure, adjustable size, fast switching speed, and low energy consumption but also is a single device with data storage and processing functions, is considered one of the most promising electronic devices for use in neuromorphic electronic systems that can simulate the neural network of the human brain [1–3]. The first step in building a neuromorphic system is to develop artificial synaptic devices that can simulate multiple functions (e.g., short-term plasticity, long-term plasticity and controllability) of biological synapses. Artificial synapses based on oxides, sulfides or organic materials have been widely studied [4–6]. Despite recent advances in memristors, the development of new materials and synaptic structures is needed to achieve high learning and computing capabilities.

Layered materials are combined through weak van der Waals forces between atomic layers, providing an invaluable foundation for the preparation and research of two-dimensional (2D) materials. Since its development in 2004 [7], graphene has been the leader in 2D material systems. Because of its unique properties (e.g., high mobility, good conductivity and high mechanical stability), graphene has broad potential applications [7–10]. Notably, among 2D materials (Table S1), graphene exhibits the highest thermal conductivity (as high as 1250 W m^{-1} K^{-1}). Moreover, graphene-based electrodes, which have a high contact resistance and weak van der Waals forces, can reduce the running current compared with some metal electrodes [8]. 2D tin selenide (SnSe) materials, which feature a high resistance and a low density of intrinsic defects [10], are potential memristive materials. Chemical vapor deposition (CVD) has been mainly used to fabricate memristors based on 2D large-area materials. However, the high temperature associated with CVD makes it incompatible with industrial manufacturing processes. Thus, 2D SnSe materials fabricated at low temperature warrant greater attention.

In the present work, a two-terminal memristor with an Au/SnSe/graphene/SiO_2/Si structure was fabricated and its electrical properties were measured. The device ex-

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hibits stable and uniform resistive switching performance and a high R_{OFF}/R_{ON} ratio, and its set and reset power are 16.7 and 2.3 nW, respectively. Meanwhile, it might simulate biological synaptic functions, including paired-pulse facilitation (PPF), short-term plasticity (STP), and long-term plasticity (LTP). Its switching behavior from STP to LTP can be regulated by applying various continuous pulses. The results reveal that the Au/SnSe/graphene/SiO_2/Si device is a candidate for use in high-density storage and neuromorphic computing applications.

EXPERIMENTAL SECTION

First, a anisole solution of polymethyl methacrylate was spin-coated onto the surface of a graphene film grown on a Cu foil substrate and heated at 45°C for 10 min. The coated substrate was etched using a solution of $CuSO_4$: H_2O:HCl (1 g/5 mL/5 mL) for ~12 h. Deionized water was then used to clean the remaining etching solution. The graphene was picked up using the SiO_2/Si substrate, and the coated substrate was heated at a low temperature (45°C, 10 min). The sample was soaked in acetone solvent for 6 h, during which the solution was replaced three times, and was allowed to dry naturally, resulting in graphene/SiO_2/Si. The SnSe film was deposited using pulsed laser deposition onto the graphene/SiO_2/Si substrate (1.5 J cm^{-2}, 5 Hz, 300°C). Details of the preparation of the Au electrode are provided elsewhere [11].

RESULTS AND DISCUSSION

Fig. 1a displays the X-ray diffraction (XRD, Bruker AXS D8 Advance) 2θ-scan pattern of the SnSe thin film deposited onto the graphene/SiO_2/Si substrate. XRD peaks are observed at 15.6° (200) and 31.3° (400), consistent with orthorhombic SnSe (PDF#97-005-2425, *Pnma* (No. 62)). The peaks correspond to *d*-spacings of 5.7 and 2.8 Å, respectively. Fig. 1b shows the Raman spectra of the SnSe and graphene. The SnSe material with D^{16}_{2h} symmetry has 12 active vibration modes, including $4A_g$, $2B_{1g}$, $4B_{2g}$, and $2B_{3g}$ modes [12]. In the present experiment, the peaks observed at approximately 68.2, 100.6, 151.2, and 181.7 cm^{-1} are assigned to the A^1_g, B^1_{3g}, A^2_g, and A^3_g modes of the SnSe film, respectively. However, the Raman B^1_{3g} and A^2_g peaks differ from the previously reported data, likely because of structural defects [13]. The Raman spectrum of graphene shows peaks at 1348.02 (D band), 1579.75 (G band), and 2687.75 cm^{-1} (2D band). The G band originates from an in-plane stretching vi-

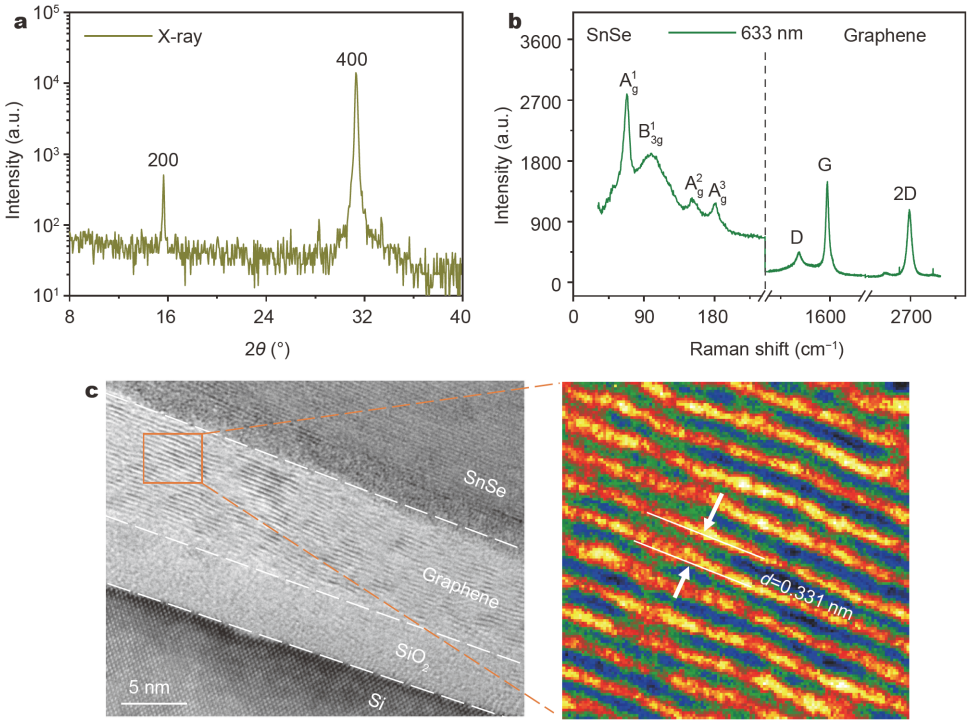

Figure 1 (a) XRD pattern of an SnSe film and (b) Raman spectra of SnSe and graphene deposited onto a SiO_2/Si substrate. (c) Cross-sectional HRTEM image of an Au/SnSe/graphene/SiO_2/Si device; the right image is a magnified image corresponding to the rectangular area drawn on the graphene electrode.

bration of C atoms with sp^2 hybridization. The intensity ratio (I_D/I_G) between the disordered band (D) and crystalline band (G) was ~0.29, confirming that few defects existed in the multilayer graphene [14]. Cross-sectional images of the Au/SnSe/graphene/SiO_2/Si devices (Fig. 1c) were recorded using a high-resolution transmission electron microscope (HRTEM, JEOL JEM2100F). The thicknesses of the SnSe, graphene, and SiO_2 layers of the naturally grown three-layer film are approximately 40, 8.2, and 5.6 nm, respectively. The inset shows magnified images corresponding to the rectangular area indicated in the image of the graphene electrode. The atomic layer spacing of the graphene is ~0.33 nm. The thermal conductivity of graphene is well known to be higher than that of most other 2D materials [15,16]. Here, we attempted to introduce 2D graphene into a memristor to improve its heat dissipation.

To further explore the memristive behaviors of the devices, we recorded their hysteresis current–voltage (*I*–*V*) curves using a Keithley 4200 SCS parameter analyzer. Here, Au and graphene were used as the device electrodes, and SnSe was used as a functional layer. A thin insulating SiO_2 layer was used to reduce the device leakage current. Fig. 2a shows a typical *I*–*V* curve for the first cycle of the Au/SnSe/graphene/SiO_2/Si device under a sweeping voltage (0 V → 5.0 V → 0 V → −4.0 V → 0 V). As the direct current bias voltage was increased from 0 to 2.0 V (1st stage), the conductance of the memristor slowly increased. However, as the voltage was increased from 2.0 to 5.0 V (2nd stage), the conductance increased rapidly. The memristor transformed from a high-resistance state (HRS) to a low-resistance state (LRS) immediately, maintained the LRS (3rd and 4th stages) from 5.0 to −2.3 V, and finally returned to the HRS (5th stage). When a second-cycle scan voltage was applied to the Au top electrode, unlike the conductance in the first scan, the conductance abruptly transformed at ~3.5 V (Fig. 2b). The *I*–*V* curves in Fig. 2c were obtained as the current compliance values were modulated (i.e., 0.4, 1.0, 5.0, 10.0, and 50.0 μA). The retentions of different resistance states of devices were measured under different current compliance values (0.4, 1, 5, and 10 μA), as shown in Fig. S1. A single memory cell might realize multilevel LRS between 1.0 and 10.0 μA current compliances, which is expected to be useful in the high-density memory field. In addition, the *I*–*V* curves for 200 cycles with the same and continuous sweeping voltage (0 V → 3 V → 0 V → −2 V → 0 V) (Fig. 2d) show excellent reproducibility and uniformity. Meanwhile, the threshold voltage of the device was determined from the results in Fig. 2e, f. Ac-

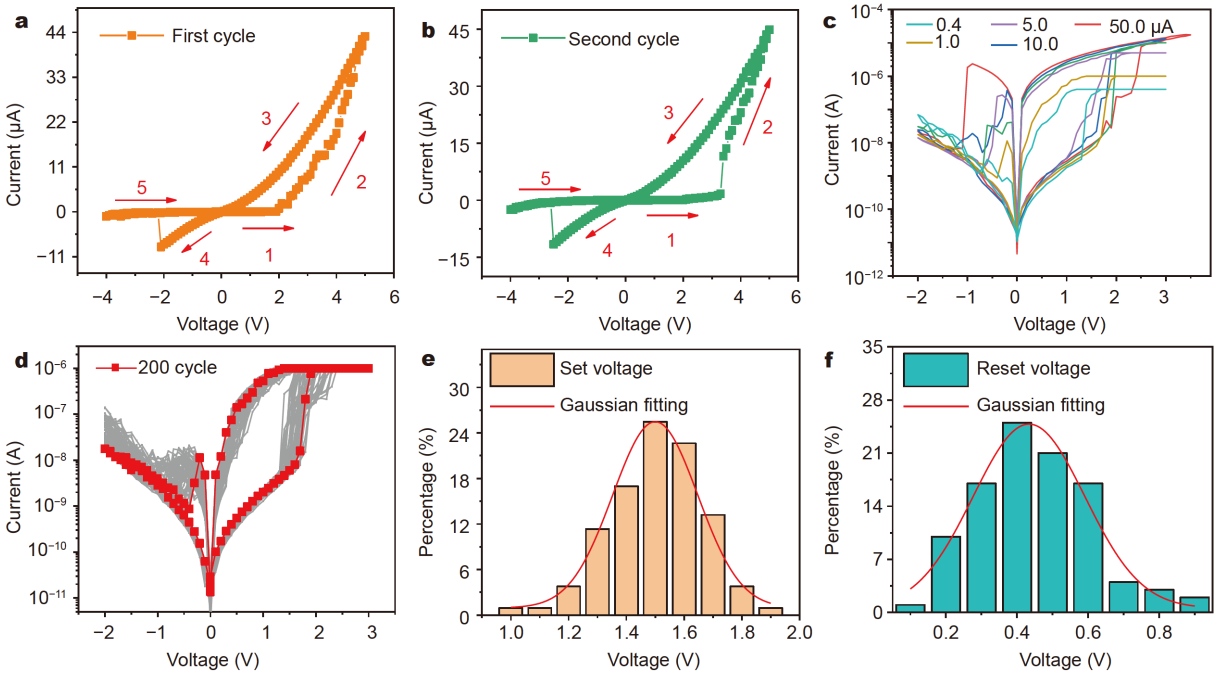

Figure 2 (a) The first and (b) second *I*–*V* curves under a sweeping voltage (0 V → 5 V → 0 V → −4 V → 0 V). (c) *I*–*V* curves of the Au/SnSe/graphene/SiO_2/Si device with modulating current compliance. (d) *I*–*V* curves of 200 continuous sweeping cycles with the same sweeping voltage (0 V → 3 V → 0 V → −2 V → 0 V). The distribution of the (e) set and (f) reset voltages for the device.

cording to the Gaussian fitting results, the set/reset voltage is separately concentrated at approximately 1.5 and −0.4 V; both voltages show a small discrete distribution. The device's set and reset powers are 16.7 and 2.3 nW, respectively. Compared with set and reset powers of the reported devices [17–24], those of our device are substantial (Table 1).

The cumulative probability of the high/low-resistance illustrates that the distribution for the HRS and LRS of the devices is centralized (Fig. S2a). We also collected statistics on the HRS and LRS of the devices for 200 cycles and found that they all have obvious HRS and LRS distributions, which indicates that the proposed devices exhibit good endurance characteristics (Fig. S2b). Graphene, which exhibits high thermal conductivity, was introduced into the device, where it might improve the dissipation of heat generated during device operation, thereby increasing the device's stability and service life.

Fig. 3a shows that the electronic transport mechanism for the device includes the Poole–Frenkel (PF) and trap-assisted tunneling (TAT) models, as further confirmed by the fitting results for the I–V characteristics. First, the relation between $\ln(I/V)$ and $V^{1/2}$ corresponding to the positive I–V curve of the Au/SnSe/graphene/SiO_2/Si de-

Table 1 Statistics for the set and reset power of the proposed device

Device structure	Set power (W)	Reset power (W)	Ref.
Au/SnSe/graphene/SiO_2/Si	10^{-8}	10^{-9}	This work
TiN/AlN/graphene/Pd	10^{-8}	10^{-4}	[17]
Ag/SiGe/*p*-Si	10^{-7}	10^{-4}	[18]
Ag/SiO_2/Pt	10^{-6}	10^{-2}	[19]
Cu/AlN/Pt	10^{-5}	10^{-3}	[20]
Ag/TiO_2/Pt	10^{-5}	10^{-4}	[21]
Ag/LSMO/Pt	10^{-3}	10^{0}	[22]
Cu/AlN/TiN	10^{-5}	10^{-4}	[23]
Ag/AgInSnTe/Ta	10^{-5}	10^{-4}	[24]

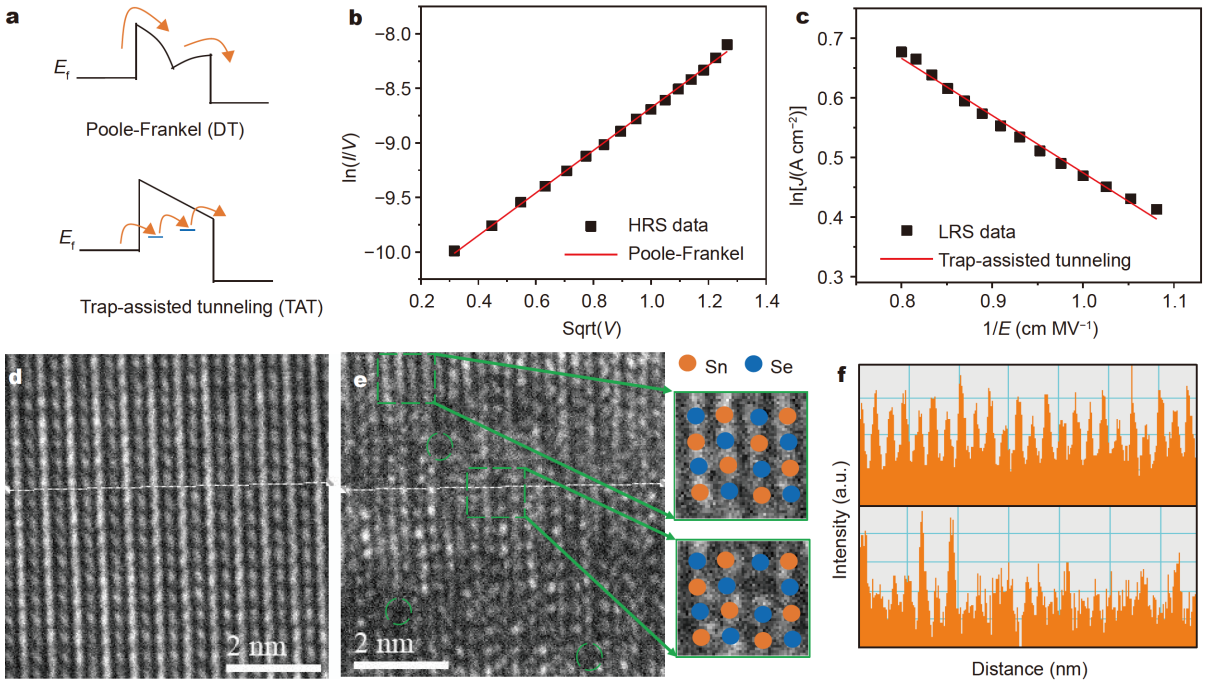

Figure 3 (a) Schematics of two possible transport mechanisms: the PF and TAT models. (b) PF and (c) TAT mechanism fitting for the Au/SnSe/graphene/SiO_2/Si device. HRTEM images of SnSe films in the (d) initial state and (e) low-resistance state. (f) Line profiles for line areas with (top) and without (bottom) atomic vacancies in SnSe materials.

vice in the HRS (Fig. 2a) can be fitted linearly (Fig. 3b). The results show that the fitted data are coincident with the PF model [25]. Under the PF mechanism, a Coulomb potential barrier under the charge interaction limits electron movement. However, the barrier is lowered under a high electric field; thus, the electrons are more likely to break free. Next, the positive *I*–*V* curve of this device in the LRS (Fig. 2a) was fitted as ln(*J*) *vs.* E^{-1}, where *J* is the current density and *E* is the electric field (Fig. 3c). The fitting results indicate linear behavior, meaning that the electronic transport behavior can be well described by the TAT model [26]. The switching behavior of the device's switching resistance could be better fitted because of the large number of defect states introduced into the SnSe material during the manufacturing process [12].

To further investigate the resistance switching mechanism, the microscopic properties of the device were characterized using HRTEM. Fig. 3d, e show the HRTEM images of SnSe materials before and after application of electric fields. Obviously, the HRTEM image of SnSe in the LRS shows more defects than the image of SnSe in its initial state. The areas within the green dashed boxes in Fig. 3e are enlarged in the right illustration, which show the standard zigzag-oriented quadrilateral units and units with vacancies. The absence of Sn atoms is apparent in Fig. 3e. Moreover, the line profiles (Fig. 3f) for Sn and Se atoms were collected from the white-lined area. Sn vacancy defects are observed in the films of devices in the LRS. Based on the aforementioned analysis, the resistance switching mechanism for the device is attributable to the formation and rupture of filamentary conducting paths consisting of Sn vacancies.

Fig. 4 shows the schematics of the initial state, LRS, and HRS of the device during the setting and resetting processes. Numerous Sn vacancies are observed inside the initial-state device under an electric field. These vacancies form Sn vacancy filament paths between the Au electrode and the graphene electrode, and the device is in the LRS. When a negative voltage is applied to the device in the LRS, the filament conducting path is ruptured and the device is in the HRS. Sn vacancies have the greatest possibility of playing a leading role in the resistive switching process; however, the existence and influence of other defects cannot be completely excluded.

The neurotransmitter dopamine ($C_8H_{11}NO_2$) is generally believed to govern learning and memory behaviors in the human neural network. In particular, $C_8H_{11}NO_2$ regulates synaptic plasticity [20,27]. Here, the synaptic plasticity of the electronic synapse was tested. When an excitation pulse was applied to the device, its conductance value changed significantly with a short-term modulation of ~0.5 mS because of ionic currents; it gradually stabilized at a higher-than-initial state (Fig. 5a). To further verify the adjustable characteristics, a continuous excitation with a different duty cycle (0.25 and 0.70) was applied to the device (Fig. 5b, c). The results illustrate that a sequence pulse with a large ratio leads to a conductivity greater than that of the device in its initial state; that is, the device can be switched from short-term to long-term memory. The effect of voltage amplitude on the conductance was also studied. The width and interval of the pulse were both 1 ms, the step voltage was 0.1 V, and the voltage amplitude sequence was 1.5–3.5 V. As the voltage was increased linearly, the rate of change of the current gradually decreased, indicating a change in the resistance state of the device (Fig. 5d).

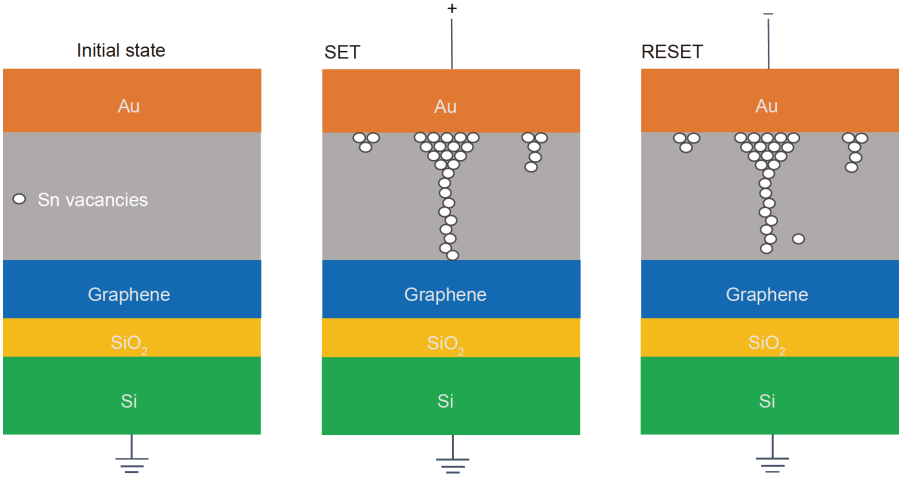

Figure 4 Schematics of the resistance switching mechanism for the device in its initial, high-resistance, and low-resistance states.

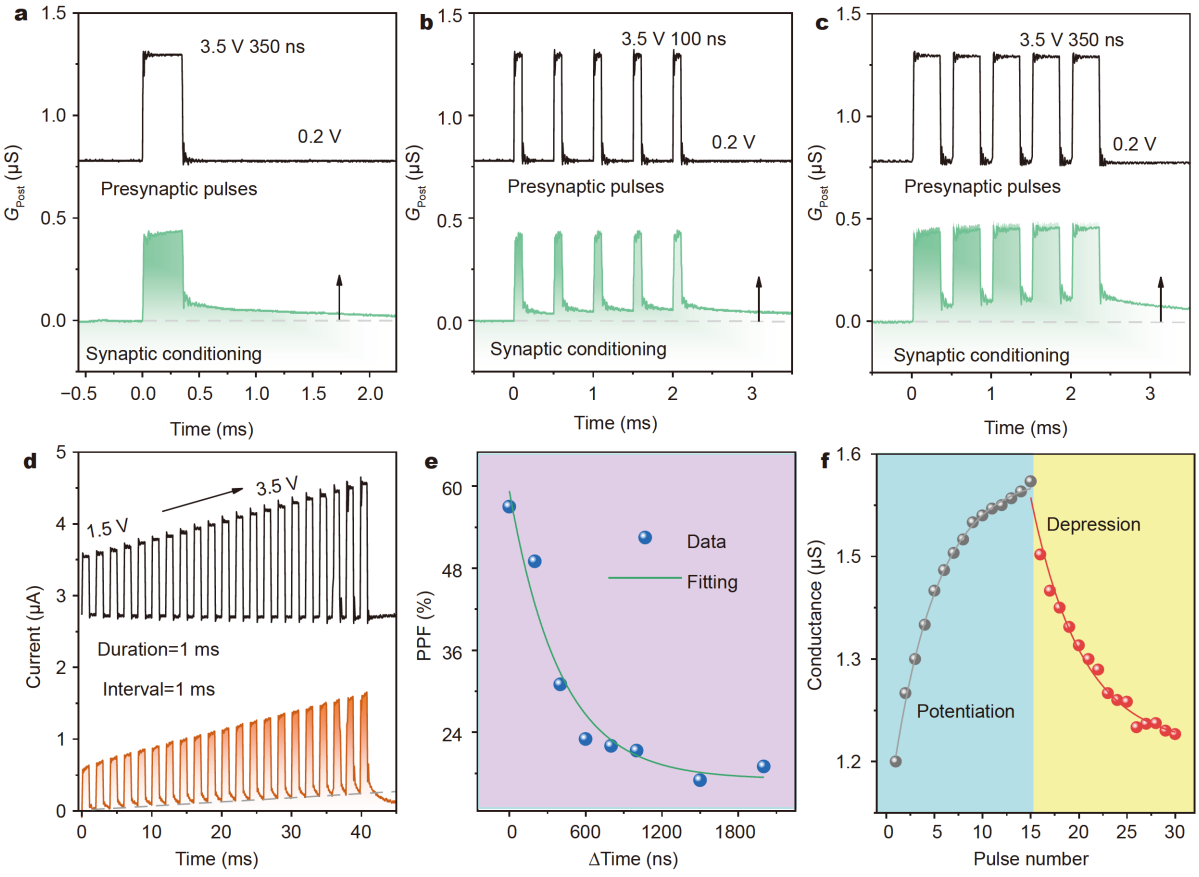

Figure 5 Neurobehaviors for a neuromorphic device. (a) Postsynaptic current remains higher than the initial level after one presynaptic pulse (3.5 V, 350 ns). (b, c) Pulsing curves for the device after application of a sequence of presynaptic pulses with different ratios (duration:interval = 0.25 and 0.70). (d) Pulsing curves for the device after a pulse with a different amplitude (1.5 V → 3.5 V). (e) PPF characteristics. (f) Relationship between the conductance and pulse number under the consecutive application of potentiation and depression pulses.

The PPF characteristics of the device were also tested. PPF is an important learning rule that simulates the forgetting process in biological synapses (Fig. 5e). The pulse waveform for driving PPF was set as follows (Fig. S3a): the duration and amplitude of the read pulse were 500 ns and 0.5 V, respectively, the duration of the write pulse was 250 ns, and the voltage amplitude was 3.5 V. The formula for PPF is

$$\mathrm{PPF} = (G_2 - G_1)/G_1 \times 100\% = C_1\exp(-t/\tau_1) + C_1\exp(-t/\tau_2), \quad (1)$$

where G_1 and G_2 are the conductance values after the first and second pulse, respectively, and τ is a time constant [5]. The fitting parameters are $C_1 = 20.87$, $C_2 = 21.30$, $\tau_1 = 401.00$ ns, and $\tau_2 = 402.00$ ns. The results show that a smaller interval leads to high conductance, whereas a larger interval leads to low conductance. When the time interval was sufficiently large, no further change was observed in the device conductance.

Fig. 5f shows the STP and LTD behaviors of the proposed device subjected to the pulse sequence. Here, we set the driving pulse as follows (Fig. S3b): for the positive-pulse part, we set 15 pulse waveforms with a duration of 200 ns and a voltage amplitude of 0.9 V; for the negative pulse part, we set 15 pulse waveforms with a duration of 200 ns and a voltage amplitude of −0.5 V. The results indicate that the proposed device exhibits bidirectional gradual conductance changes which can be regulated by positive or negative pulse sequences. The developed bidirectional analog memristor is suitable for application in more complex deep neural networks.

CONCLUSION

Graphene with high thermal conductivity was incorporated into Au/SnSe/graphene/SiO_2/Si memristors to improve their performance. The set/reset power for the memristor could be as low as 16.7 and 2.3 nW, respec-

tively—far lower than those of most current devices. The device not only exhibited excellent stability and uniformity and a high R_{OFF}/R_{ON} ratio but also could simulate biosynaptic functions such as PPF, STP, and LTP. Such excellent performance is attributed to the incorporation of graphene, which exhibits high heat dissipation, and a SiO_2 insulation layer. The proposed device is an excellent candidate for use in high-density storage and neuromorphic computing applications.

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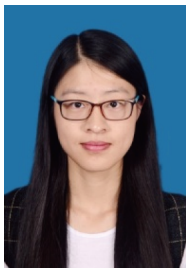
Author contributions Yan X designed the samples and revised the paper. Wang H conducted the performance test of the device and prepared the manuscript. Yu T analyzed the data. Zhao J assisted in writing the response. All authors contributed to the general discussion of the manuscript.

Conflict of interest The authors declare no conflict of interest.

Supplementary information Supporting data are available in the online version of the paper.



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基于层状硒化锡/石墨烯材料的低功耗忆阻器件

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摘要 在外部刺激下具有电导可调功能的新兴两端忆阻器被认为在记忆和电子突触功能方面颇具潜力. 但是, 目前忆阻器的稳定性、均匀性和功耗在神经形态计算中仍然具有一定挑战性. 本文中, 我们利用具有高导热性的层状二维石墨烯制造了Au/SnSe/石墨烯/SiO_2/Si忆阻器. 该器件不仅具有压倒性的电性能(高稳定性、均匀性和R_{OFF}/R_{ON}比), 而且还可以实现生物突触功能, 例如双脉冲促进、短期可塑性和长期可塑性. 其开关功率值分别可降低至16.7和2.3 nW. 同时, 高分辨透射电子显微镜图证实了该器件的电阻转换机制, 可能归因于由锡空位组成的丝状导电路径的形成和破裂. 该设备有望应用于高密度存储和低功率神经形态计算领域.