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Balance control of grid currents for UPQC under unbalanced loads based on matching-ratio compensation algorithm

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Abstract In three-phase four-wire systems, unbalanced loads can cause grid currents to be unbalanced, and this may cause the neutral point potential on the grid side to shift. The neutral point potential shift will worsen the control precision as well as the performance of the three-phase four-wire unified power quality conditioner (UPQC), and it also leads to unbalanced three-phase output voltage, even causing damage to electric equipment. To deal with unbalanced loads, this paper proposes a matching-ratio compensation algorithm (MCA) for the fundamental active component of load currents, and by employing this MCA, balanced three-phase grid currents can be realized under 100% unbalanced loads. The steady-state fluctuation and the transient drop of the DC bus voltage can also be restrained. This paper establishes the mathematical model of the UPQC, analyzes the mechanism of the DC bus voltage fluctuations, and elaborates the interaction between unbalanced grid currents and DC bus voltage fluctuations; two control strategies of UPQC under three-phase stationary coordinate based on the MCA are given, and finally, the feasibility and effectiveness of the proposed control strategy are verified by experiment results.

Keywords Unified power quality conditioner (UPQC), Unbalanced loads, Matching-ratio compensation, Balance control, DC bus voltage fluctuations

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1 Introduction

At present, the three-phase four-wire power supply network has been widely used in the 380 V low-voltage power supply system [1, 2], in which each phase can operate independently. If there is no effective compensation, unbalanced grid currents will emerge because of a single-phase load or unbalanced loads, and these will cause a zero sequence current flow in the neutral line of the grid side. The more unbalanced the loads are, the greater neutral line current is. Usually, the neutral line of the grid side is selected as a reference ground for both the power and control circuit in a three-phase four-wire system. The neutral potential is not zero when a larger current flows through the neutral line, and this will lead to an offset over the reference ground. As a result of this ground offset, the control precision and performance of the overall UPQC will be deteriorated, and then three-phase load voltages become unbalanced. Each phase voltage may be above or below the rated voltage to a different extent, and this will tend to cause damage to the electrical equipment [3].

To overcome the influence of unbalanced loads on the grid side neutral potential shift, it is necessary to control the three-phase grid currents to keep them in a sinusoidal and balanced state under unbalanced loads. The unified power quality conditioner (UPQC) [4–13] has the ability to compensate for unbalanced load currents and to realize the balance control of the grid currents.

In terms of grid current control, three independent H-bridges are used to form a parallel active power filter, and the single-phase *p-q* theory is employed to control the grid currents, so as to keep them in a balanced state [4, 5]. However, in this structure six more IGBTs are needed compared with a three-phase half-bridge inverter, and this will increase the control complexity and the cost. In [6], the grid current and load voltage references in both dq and $\alpha\beta$ coordinates are calculated, and then hysteresis control is used to achieve grid current balance. However, the switching frequency of hysteresis control is not constant, and in [6] the design of appropriate LC filters is not considered. In [7], the grid currents are controlled as balanced sinusoidal currents in the positive and negative sequence double synchronous rotating coordinates under unbalanced loads. However, the implementation of this method requires multiple coordinate transformations, and the number of controllers in the closed-loop control is relatively larger, so control complexity is increased. The reactive power compensation and admittance calculation method are used to realize grid current balance control based on the balanced component method [8, 9]. In using this method, the unbalanced loads need to be decomposed, and the admittance calculation is also necessary. This makes the calculation rather complicated.

In a direct control scheme [10, 11] for UPQC, the DC bus voltage will be involved in the generation process of the grid current reference. The output result of the DC bus voltage loop is directly used as the grid current reference generation in [12, 13]. However, the DC bus voltage will produce a larger fluctuation under unbalanced loads, and this may cause the current reference to be distorted and thus the sine and balance degrees of the grid currents to be poor. Because of the low bandwidth and slow response of the DC bus voltage loop, the DC bus voltage will produce a large transient drop with a load step-up, exacerbating the deterioration of the control effect of the grid currents. To overcome the above shortcomings, a matching-ratio compensation algorithm (MCA) for the fundamental active component of load currents is proposed to calculate the grid current reference, so as to optimize the sine and balance degrees of the grid currents, reduce the steady-state fluctuation of the DC bus voltage, and improve the dynamic response speed of the DC bus loop. At the same time, the mutual influence between DC bus voltage fluctuations and unbalanced grid currents can also be weakened.

When a system is controlled in the three-phase stationary coordinate, the traditional proportional-integral (PI) controller [14] cannot achieve the zero steady-state error control. Therefore, a resonant (R) controller is employed to achieve zero steady-state error in [15]. The nonlinear loads may cause the output voltages of the inverter to be distorted, and thus multi-resonant (MR) controllers are employed to effectively control several low-order harmonics with high content in the nonlinear load currents in [16], so as to improve the waveform quality of the inverter voltage. In this paper, the UPQC is controlled in the three-phase stationary coordinate. The references of both converters are the fundamental sine quantities, considering the influence of the nonlinear loads, the PI + MR control method is employed to improve the waveform qualities of the grid currents and load voltages for the UPQC.

This paper aims to realize the balance control of three-phase grid currents under unbalanced loads. Compared with the aforementioned control strategies in [4–13], the control strategy based on the proposed MCA possesses a better control performance and can be realized more easily.

This paper is organized as follows. After this introduction and in Section 2, the mathematical model of UPQC is established, and the mechanism of DC bus voltage fluctuation is analyzed thoroughly; then the control strategy based on the MCA is given under the three-phase stationary coordinate, and the essence of the mutual influence between the DC bus voltage fluctuations and the unbalanced grid currents is revealed. To reduce the steady-state errors of PI controllers in the three-phase stationary coordinate, the MR controllers are added to the control loop of the two converters. Considering the most serious unbalanced loads (a single-phase load), the operation state of UPQC is thoroughly described and three important conclusions are obtained in Section 3. Finally, experimental results show that three-phase grid currents can be maintained in a sinusoidal and balanced state under the single-phase resistive and nonlinear load by using the proposed MCA strategy. The neutral line current on the grid side fluctuates slightly around zero. The steady-state fluctuation and the transient drop of the DC bus voltage can be reduced. The correctness of the theoretical analysis and the feasibility of the given strategy are verified by experiment results.

2 Theoretical analysis

The three-phase four-wire UPQC mainly consists of two bidirectional converters connected back-to-back sharing a common DC bus, as shown in Fig. 1.

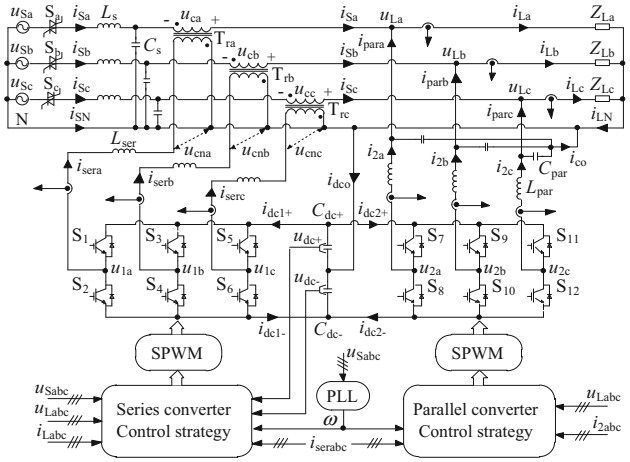

Fig. 1 Three-phase four-wire UPQC topology

It should be noted that S_{abc} are turned on at the positive and negative half cycles of the grid voltage. Once the grid short circuit, S_{abc} can cut off the connection between the UPQC and grid in time, so as to prevent the UPQC from generating a large short circuit current to feed back to the grid. The primary and secondary sides of Tr_{abc} are connected to the grid and series converter, with turn ratio $n = N_1{:}N_2 = 1{:}5$.

The direct control scheme [10, 11] employed is described as follows: (a) The series converter is controlled to operate as a sinusoidal current source. It has the current source characteristic with impedance high enough for harmonic voltages, and thus mutual pollution between the source and load can be avoided [17]. The grid currents are controlled by the series converter to be sinusoidal, balanced and always in phase with the grid voltages, and the DC bus voltage is stabilized at a desired level; (b) The parallel converter is controlled to operate as a sinusoidal voltage source. It has the voltage source characteristic with impedance small enough to harmonic currents, and it provides the reactive power and harmonic currents for loads [11]. The load voltages are controlled by the parallel converter to be sinusoidal, balanced and in phase with the grid voltages.

2.1 Modeling and control of series converter

1) Mathematical model of series converter

The series converter topology is shown in Fig. 2, where i_{dco2} is the zero sequence current generated by the unbalanced loads and load voltages, and i_{so} is the zero sequence current generated by the output currents of the series converter i_{serabc}. Since the grid currents i_{Sabc} are controlled by the currents i_{serabc}, the current i_{so} is equivalent to the neutral current of the grid side i_{SN}.

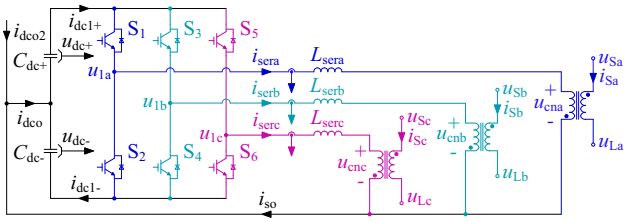

Fig. 2 Series converter topology

The main reason for the unbalanced grid currents is the DC bus voltage fluctuations caused by the unbalanced loads. Therefore, it is necessary to establish the mathematical model of the series converter and analyze the mechanism of DC bus voltage fluctuations.

Let $L_{serabc} = L_{ser}$, and the state space average model of the series converter is as follows:

$$\begin{cases} u_{1a} = L_{ser}\dfrac{\mathrm{d}i_{sera}}{\mathrm{d}t} + R_{ser}i_{sera} + u_{cna} \\ u_{1b} = L_{ser}\dfrac{\mathrm{d}i_{serb}}{\mathrm{d}t} + R_{ser}i_{serb} + u_{cnb} \\ u_{1c} = L_{ser}\dfrac{\mathrm{d}i_{serc}}{\mathrm{d}t} + R_{ser}i_{serc} + u_{cnc} \end{cases} \tag{1}$$

where R_{ser} is the equivalent resistance of L_{ser}.

The relationship among the secondary side voltages of series transformers u_{cnabc}, grid voltages u_{Sabc} and load voltages u_{Labc} is:

$$\begin{cases} u_{cna} = (u_{La} - u_{Sa})/n \\ u_{cnb} = (u_{Lb} - u_{Sb})/n \\ u_{cnc} = (u_{Lc} - u_{Sc})/n \end{cases} \tag{2}$$

If output currents of the series converter i_{serabc} are unbalanced, they can be expressed as:

$$i_{sera} + i_{serb} + i_{serc} = i_{so} \tag{3}$$

The zero sequence current i_{dco2} generated by the unbalanced loads Z_{Labc} and load voltage u_{Lo} can be expressed as:

$$i_{dco2} = i_{LN} + i_{co} = (i_{para} + i_{parb} + i_{parc}) + \frac{3}{C_{par}}\frac{\mathrm{d}u_{Lo}}{\mathrm{d}t} \tag{4}$$

The switching states of the series converter are represented by the switching function S_{1j}: (1) $S_{1j} = 1$ when jth leg upper switch is turned on and jth leg lower switch is turned off, (2) $S_{1j} = -1$ when jth leg lower switch is turned on and jth leg upper switch is turned off.

$$S_{1j} = \begin{cases} 1 \\ -1 \end{cases} \qquad j = \mathrm{a,\ b,\ c} \tag{5}$$

where subscript 1 represents the series converter.

Based on (5), the three-leg voltages of the series converter u_{1abc} can be expressed as:

$$\begin{cases} u_{1a} = u_{dc+}\dfrac{S_{1a}+1}{2} + u_{dc-}\dfrac{S_{1a}-1}{2} \\ u_{1b} = u_{dc+}\dfrac{S_{1b}+1}{2} + u_{dc-}\dfrac{S_{1b}-1}{2} \\ u_{1c} = u_{dc+}\dfrac{S_{1c}+1}{2} + u_{dc-}\dfrac{S_{1c}-1}{2} \end{cases} \tag{6}$$

The positive and negative DC bus currents $i_{dc\pm}$ can be expressed as:

$$\begin{cases} i_{dc1+} = i_{sera}\dfrac{S_{1a}+1}{2} + i_{serb}\dfrac{S_{1b}+1}{2} + i_{serc}\dfrac{S_{1c}+1}{2} \\ i_{dc1-} = i_{sera}\dfrac{S_{1a}-1}{2} + i_{serb}\dfrac{S_{1b}-1}{2} + i_{serc}\dfrac{S_{1c}-1}{2} \\ i_{dc1+} - i_{dc1-} = i_{so} + i_{dco2} = i_{dco} \end{cases} \tag{7}$$

Based on the instantaneous power theory [18], ignoring the inductance resistance R_{ser}, an energy expression is derived from (1) to (7):

$$\begin{aligned} &u_{cna}i_{sera} + u_{cnb}i_{serb} + u_{cnc}i_{serc} \\ &\quad = u_{dc+}i_{dc1+} + u_{dc-}i_{dc1-} - \frac{L_{ser}}{2}\frac{da_1}{dt} \end{aligned} \tag{8}$$

where $a_1 = i_{sera}^2 + i_{serb}^2 + i_{serc}^2$.

The left side of (8) is the instantaneous output power of the series converter p_{ser}, and it can be expressed as:

$$p_{ser} = u_{cna}i_{sera} + u_{cnb}i_{serb} + u_{cnc}i_{serc} \tag{9}$$

The positive and negative DC capacitor currents $i_{dc1\pm}$ can be expressed as:

$$\begin{cases} i_{dc1+} = C_{dc+}\dfrac{du_{dc+}}{dt} \\ i_{dc1-} = C_{dc-}\dfrac{du_{dc-}}{dt} \end{cases} \tag{10}$$

Substituting (9) and (10) into (8), p_{ser} can be further expressed as:

$$p_{ser} = \frac{C_{dc+}}{2}\frac{du_{dc+}^2}{dt} + \frac{C_{dc-}}{2}\frac{du_{dc-}^2}{dt} - \frac{L_{ser}}{2}\frac{da_1}{dt} \tag{11}$$

The expressions of positive and negative DC bus voltages $u_{dc\pm}$ can be derived from (10):

$$\begin{cases} u_{dc+} = \dfrac{1}{C_{dc+}}\displaystyle\int_0^t i_{dc1+}dt + U_{dco+} \\ u_{dc-} = \dfrac{1}{C_{dc-}}\displaystyle\int_0^t i_{dc1-}dt + U_{dco-} \end{cases} \tag{12}$$

where U_{dco+} and U_{dco-} are the initial voltages of capacitors C_{dc+} and C_{dc-} respectively.

Let $C_{dc+} = C_{dc-} = C_{dc}$ and $U_{dco+} = U_{dco-} = U_{dco}$, the difference of u_{dc+} and u_{dc-} can be derived from (12):

$$u_{dc+} - u_{dc-} = \frac{1}{C_{dc}}\int_0^t i_{dco}dt \tag{13}$$

It can be derived from (11) that:

$$u_{dc+}^2 + u_{dc-}^2 = \frac{2}{C_{dc}}\int_0^t p_{ser}dt + \frac{L_{ser}a_1}{C_{dc}} + \frac{W_o}{C_{dc}} \tag{14}$$

where W_o is the initial energy stored on the capacitor C_{dc}.

The total DC bus voltage u_{dc} can be obtained based on (13) and (14):

$$\begin{aligned} u_{dc} &= u_{dc+} + u_{dc-} \\ &= \sqrt{\frac{2W_o}{C_{dc}} + \frac{4}{C_{dc}}\int_0^t p_{ser}dt + \frac{2L_{ser}a_1}{C_{dc}} - \frac{1}{C_{dc}^2}\left(\int_0^t i_{dco}dt\right)^2} \end{aligned} \tag{15}$$

From (13) and (15), the expressions of positive and negative DC bus voltages $u_{dc\pm}$ can be rewritten as:

$$\begin{cases} u_{dc+} = \dfrac{u_{dc}}{2} + \dfrac{1}{2C_{dc}}\displaystyle\int_0^t i_{dco}dt \\ u_{dc-} = \dfrac{u_{dc}}{2} - \dfrac{1}{2C_{dc}}\displaystyle\int_0^t i_{dco}dt \end{cases} \tag{16}$$

The mechanism of DC bus voltage fluctuations can be revealed by (15) and (16). That is, the DC bus voltage u_{dc} and $u_{dc\pm}$ will fluctuate with the changes of the power p_{ser}, currents i_{serabc} and neutral current i_{dco}.

However, u_{dc} will be involved in the generation process of the grid current reference. If the fluctuation of u_{dc} is larger than a certain level, it will deteriorate with the sine and balance degrees of the grid currents, leading to increasing the neutral current i_{SN}, which exacerbates the DC bus voltage fluctuation in turn. Thus, based on the above analysis, it can be clearly seen that there is a mutual influence between the DC bus voltage fluctuation and the neutral currents. In addition, in the topology proposed, the neutral current of the load side flows into the neutral point of the positive and negative DC capacitors, resulting in a larger DC bus voltage fluctuation which is proportional to the load unbalance degree.

2) Control strategy of series converter

To overcome the adverse influence of DC bus voltage fluctuation on the balance control of grid currents, this paper proposes the MCA to calculate the grid current reference. Three ways for improvement are presented: (a) it can suppress influence of the DC bus voltage fluctuation on the sine and balance degrees of the grid currents; (b) it can reduce the steady-state fluctuation of the DC bus voltage; (c) it can improve the response speed of the DC bus voltage loop, so as to reduce a large transient drop of DC bus voltage with a load step-up. Considering (a), (b) and (c), the MCA can finally reduce the mutual influence between the DC bus voltage fluctuation and unbalanced grid currents.

The proposed MCA is described as follows: First the grid voltages u_{Sabc}, load voltages u_{Labc} and load currents i_{Labc} are transformed by dq transformation:

$$u_{Sd} = \bar{u}_{Sd} + \tilde{u}_{Sd} \tag{17}$$

$$u_{Ld} = \bar{u}_{Ld} + \tilde{u}_{Ld} \tag{18}$$

$$i_{Ld} = \bar{i}_{Ld} + \tilde{i}_{Ld} \tag{19}$$

where $\bar{u}_{Sd}$, $\bar{u}_{Ld}$ and $\bar{i}_{Ld}$ are the DC components, and they represent the fundamental active components. $\tilde{u}_{Sd}$, $\tilde{u}_{Ld}$ and $\tilde{i}_{Ld}$ are the AC components, and they represent the harmonic components.

Generally, certain harmonics and imbalance usually exist in the grid voltages, so the AC component $\tilde{u}_{Sd}$ obtained after dq transformation is not zero. In addition, the load voltages and currents after dq transformation must contain the ac components $\tilde{u}_{Ld}$ and $\tilde{i}_{Ld}$ with the nonlinear loads. The above ac components will bring in an error during the grid current reference calculation process, and to solve this problem, low pass filters (LPFs) are employed to eliminate these ac components.

In (17), (18) and (19), $\bar{u}_{Sd}$, $\bar{u}_{Ld}$ and $\bar{i}_{Ld}$ represent the fundamental amplitude of grid voltages, load voltages and load currents, respectively, and they can be obtained by filtering u_{Sd}, u_{Ld} and i_{Ld} with LPFs.

According to the instantaneous power theory, ignoring the system loss, the fundamental active powers on the grid side and load side are equal, as follows:

$$\bar{P}_{Sd} = \bar{P}_{Ld} = \bar{u}_{Sd}\bar{i}_{Sd} = \bar{u}_{Ld}\bar{i}_{Ld} \tag{20}$$

The proposed MCA for load fundamental active current can be expressed as:

$$\bar{i}_{Sd} = \frac{\bar{u}_{Ld}}{\bar{u}_{Sd}}\bar{i}_{Ld} \tag{21}$$

It can be seen from (21) that $\bar{i}_{Sd}$ can adjust the magnitude of the grid current with the changes of the load active power $\bar{u}_{Ld}\bar{i}_{Ld}$ and the grid voltage $\bar{u}_{Sd}$, and thus $\bar{i}_{Sd}$ has adaptability to grid voltages.

Based on the proposed MCA and mathematical model of the series converter, the control block diagram of the series converter in a three-phase stationary coordinate is given, as shown in Fig. 3. It can be seen that there is a mutual influence between the DC bus voltage fluctuation and unbalanced grid currents.

The DC bus voltage loop can compensate for the UPQC internal loss, and is also a link of cooperative work between serial and parallel converters.

The transfer function of PI controller $G_{dc}(s)$ for the DC voltage loop can be expressed as:

$$G_{dc}(s) = k_{dcp} + k_{dci}/s \tag{22}$$

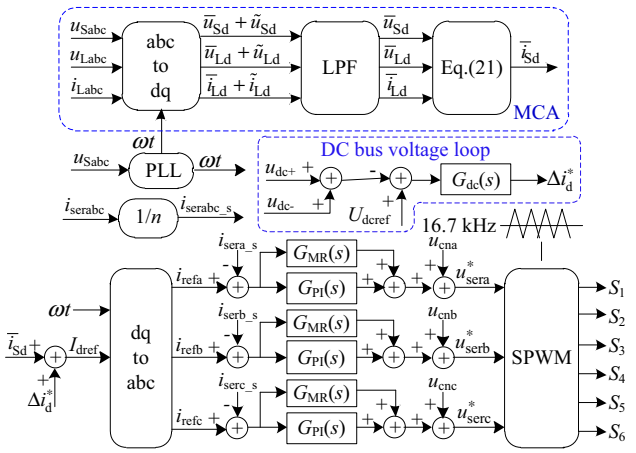

Fig. 3 Control block diagram of the series converter

where k_{dcp} and k_{dci} are the proportional and integral coefficient of $G_{dc}(s)$, respectively.

The output signal of the DC voltage loop Δi_d^* can be expressed as:

$$\Delta i_d^* = (U_{dcref} - u_{dc+} - u_{dc-})G_{dc}(s) \tag{23}$$

The grid current reference amplitude is obtained by adding the value of $\bar{i}_{Sd}$ calculated by the MCA and the output signal Δi_d^*:

$$I_{dref} = \bar{i}_{Sd} + \Delta i_d^* \tag{24}$$

In contrast, there is no the MCA part in [12, 13], and the reference I_{dref} is implemented only by the output signal of the DC bus voltage loop, i.e. $I_{dref} = \Delta i_d^*$. The DC bus voltage u_{dc} with a larger fluctuation will make the grid currents i_{Sabc} unbalanced or even distorted, but after adding the MCA, it can be found that the reference I_{dref} is shared by $\bar{i}_{Sd}$ and Δi_d^*, where $\bar{i}_{Sd}$ takes most of the current reference from (21) and (24), so as to reduce the influence of the DC bus voltage fluctuation on i_{Sabc}.

The a-phase of the series converter is designed as an example. Its control block diagram is shown in Fig. 4, where k_{PWM} is the equivalent gain of the converter, $G_{sam}(s)$ is the current sampling link and i_{sera_s} is the sampling value of the current i_{sera}.

The current sampling link can be equivalent to a first-order inertia link, and its transfer function $G_{sam}(s)$ is:

$$G_{sam}(s) = k_{sam\_ser}/(T_{sam\_ser}s + 1) \tag{25}$$

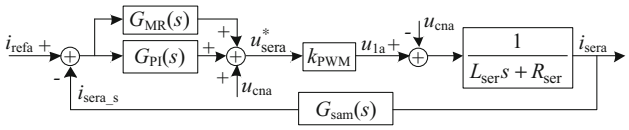

Fig. 4 Control block diagram of current loop

where k_{sam_ser} and T_{sam_ser} are the current i_{sera} sampling coefficient and filter delay time (s), respectively.

The current loop of the series converter is controlled by the PI + MR controllers, where the PI controller can correct the current loop to a type II system to improve the system's anti-jamming performance; the MR controllers are used to control the fundamental and harmonics components to improve the control accuracy of the series converter and the waveform qualities of the grid currents.

With the increase of the harmonic order, the harmonic components will decrease rapidly, and thus the influence of the high harmonic components on the load voltages is limited. Therefore, the MR controllers mainly control for the lower harmonics. Taking into account the cost of digital control computation, the fundamental and 3th, 5th and 7th harmonics are selected in this paper.

The transfer function of PI + MR controllers $G_{PIMR}(s)$ can be expressed as:

$$\begin{aligned} G_{PIMR}(s) &= G_{PI}(s) + G_{MR}(s) \\ &= (k_{serp} + \frac{k_{seri}}{s}) + \sum_{h=1,3,5,7} \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + (h\omega_o)^2} \end{aligned} \tag{26}$$

where k_{serp} and k_{seri} are the proportional and integral coefficient, respectively. k_r is the resonant coefficient, ω_c is the cut-off frequency (rad/s), ω_o is the resonant frequency $\omega_o = 100\pi$ (rad/s), and h is the harmonic order.

The design method of MR controllers can be found in [16]. The parameters of the $G_{MR}(s)$ controller are as follows: $k_r = 50$ and $\omega_c = 5$rad/s.

Figure 5 is the bode plot of $G_{PIMR}(s)$. The gain of the low frequency-band is determined by the gain of the PI controller. The PI controller plays a major role in the overall regulation process. The MR controllers will generate a large gain at the desired resonant points, and the performance of the PI controller is reflected at other frequency-bands outside the resonant points, so the parameters of $G_{PI}(s)$ will be designed accordingly.

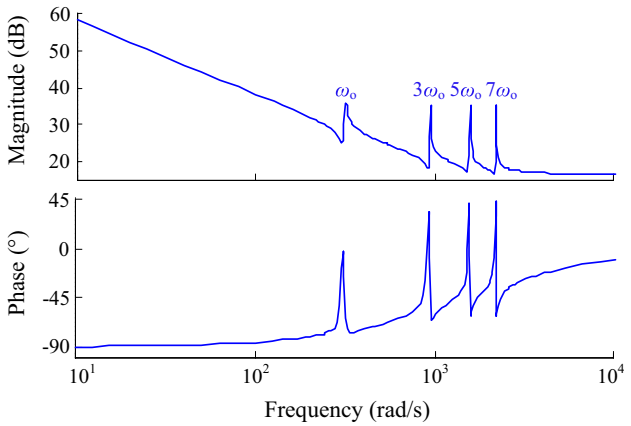

Fig. 5 Bode plot of $G_{PIMR}(s)$

The design process of the PI controller in [14] is now applied. Let the shear frequency of the current loop $\omega_{seri\_cut} = 3340\pi$ rad/s (1/10 of the switching frequency 16.7 kHz), and then the turning frequency R_{ser}/L_{ser} is much smaller than ω_{seri_cut}, so the resistor R_{ser} can be ignored in Fig.4. The current loop is corrected to a type II system, and the transfer function of the current open-loop $G_{op\_seri}(s)$ can be expressed as:

$$\begin{aligned} G_{op\_seri}(s) &= \frac{k_{PWM}}{L_{ser}s} G_{PI}(s) G_{sam}(s) \\ &= k_{op\_ser} \frac{k_{serp}s + k_{seri}}{s^2(T_{sam\_ser}s + 1)} \end{aligned} \tag{27}$$

where the current open-loop gain $k_{op\_seri} = k_{PWM}\, k_{sam\_ser}/L_{ser}$.

The turning frequency of the zero point of $G_{op\_seri}(s)$ is 1/5 of ω_{seri_cut}, and thus the relation between k_{serp} and k_{seri} can be expressed as:

$$k_{seri}/k_{serp} = k_\omega \omega_{seri\_cut} = \omega_{seri\_cut}/5 \tag{28}$$

The modulus of the transfer function $G_{op\_seri}(s)$ at the shear frequency ω_{seri_cut} is equal to 1, and the following equation can be obtained:

$$k_{serp} = \frac{\omega_{seri\_cut} L_{ser}}{k_{sam\_ser} k_{PWM}} \sqrt{\frac{1 + T_{sam\_ser}^2 \omega_{seri\_cut}^2}{1 + k_\omega^2}} \tag{29}$$

According to (28) and (29), the parameters of $G_{PI}(s)$ are as follows: $k_{serp} = 6.43$ and $k_{seri} = 819$.

The modulation signals of the series converter u^*_{serabc} can be expressed as:

$$\begin{cases} u^*_{sera} = (i_{refa} - i_{sera\_s}) G_{PIMR}(s) + u_{cna} \\ u^*_{serb} = (i_{refb} - i_{serb\_s}) G_{PIMR}(s) + u_{cnb} \\ u^*_{serc} = (i_{refc} - i_{serc\_s}) G_{PIMR}(s) + u_{cnc} \end{cases} \tag{30}$$

The three-phase grid current references i_{refabc} can be derived from the grid current reference amplitude using the inverse dq transformation:

$$\begin{cases} i_{refa} = I_{dref} \sin \omega t \\ i_{refb} = I_{dref} \sin(\omega t - 2\pi/3) \\ i_{refc} = I_{dref} \sin(\omega t + 2\pi/3) \end{cases} \tag{31}$$

where ωt is obtained by a phase-locked loop (PLL) [19].

Under the control of the series converter, the neutral current of the grid side i_{SN} is equal to zero.

2.2 Modeling and control of parallel converter

1) Mathematical model of parallel converter

The main task of the parallel converter is to ensure that the load voltages u_{Labc} are sinusoidal and balanced, and also to provide the required harmonic and reactive currents for loads. The parallel converter topology is shown in Fig. 6.

The modeling process of the parallel converter is the similar as that of the series converter, and the mathematical model expressions of the DC bus voltage in the parallel converter are given directly in this section.

The state space average model of the parallel converter is as follows:

$$\begin{cases} u_{2\mathrm{a}} = L_{\mathrm{par}}\dfrac{\mathrm{d}i_{2\mathrm{a}}}{\mathrm{d}t} + R_{\mathrm{par}}i_{2\mathrm{a}} + u_{\mathrm{La}} \\ u_{2\mathrm{b}} = L_{\mathrm{par}}\dfrac{\mathrm{d}i_{2\mathrm{b}}}{\mathrm{d}t} + R_{\mathrm{par}}i_{2\mathrm{b}} + u_{\mathrm{Lb}} \\ u_{2\mathrm{c}} = L_{\mathrm{par}}\dfrac{\mathrm{d}i_{2\mathrm{c}}}{\mathrm{d}t} + R_{\mathrm{par}}i_{2\mathrm{c}} + u_{\mathrm{Lc}} \end{cases} \tag{32}$$

$$\begin{cases} i_{2\mathrm{a}} = i_{\mathrm{ca}} + i_{\mathrm{para}} = C_{\mathrm{par}}\dfrac{\mathrm{d}u_{\mathrm{La}}}{\mathrm{d}t} + i_{\mathrm{La}} - i_{\mathrm{Sa}} \\ i_{2\mathrm{b}} = i_{\mathrm{cb}} + i_{\mathrm{parb}} = C_{\mathrm{par}}\dfrac{\mathrm{d}u_{\mathrm{Lb}}}{\mathrm{d}t} + i_{\mathrm{Lb}} - i_{\mathrm{Sb}} \\ i_{2\mathrm{c}} = i_{\mathrm{cc}} + i_{\mathrm{parc}} = C_{\mathrm{par}}\dfrac{\mathrm{d}u_{\mathrm{Lc}}}{\mathrm{d}t} + i_{\mathrm{Lc}} - i_{\mathrm{Sc}} \end{cases} \tag{33}$$

where R_{par} is the equivalent resistance of inductor L_{par}.

The parallel converter will output a zero sequence current i_{LN} under the unbalanced loads:

$$i_{\mathrm{para}} + i_{\mathrm{parb}} + i_{\mathrm{parc}} = i_{\mathrm{LN}} \tag{34}$$

The total DC bus voltage u_{dc} can be expressed as:

$$\begin{aligned} u_{\mathrm{dc}} &= u_{\mathrm{dc}+} + u_{\mathrm{dc}-} \\ &= \sqrt{\frac{2W_{\mathrm{o}}}{C_{\mathrm{dc}}} + \frac{4}{C_{\mathrm{dc}}}\int_0^t p_{\mathrm{par}}\mathrm{d}t + \frac{2L_{\mathrm{par}}b_1}{C_{\mathrm{dc}}} + \frac{2C_{\mathrm{par}}b_2}{C_{\mathrm{dc}}} - \frac{1}{C_{\mathrm{dc}}^2}\left(\int_0^t i_{\mathrm{dco}}\mathrm{d}t\right)^2} \end{aligned} \tag{35}$$

where $b_1 = i_{2\mathrm{a}}^2 + i_{2\mathrm{b}}^2 + i_{2\mathrm{c}}^2$ and $b_2 = u_{\mathrm{La}}^2 + u_{\mathrm{Lb}}^2 + u_{\mathrm{Lc}}^2$.

The expressions of positive and negative DC bus voltages $u_{\mathrm{dc}\pm}$ can be expressed as:

$$\begin{cases} u_{\mathrm{dc}+} = \dfrac{u_{\mathrm{dc}}}{2} + \dfrac{1}{2C_{\mathrm{dc}}}\displaystyle\int_0^t i_{\mathrm{dco}}\mathrm{d}t \\ u_{\mathrm{dc}-} = \dfrac{u_{\mathrm{dc}}}{2} - \dfrac{1}{2C_{\mathrm{dc}}}\displaystyle\int_0^t i_{\mathrm{dco}}\mathrm{d}t \end{cases} \tag{36}$$

It can be seen from (35) and (36) that the DC bus voltage u_{dc} and $u_{\mathrm{dc}\pm}$ will fluctuate with the changes of the power p_{par}, currents $i_{2\mathrm{abc}}$, voltages u_{Labc} and neutral current i_{dco}.

The unbalanced load voltages will also cause fluctuations in the DC bus voltage, and thus the control objective of the parallel converter is to keep the three-phase load voltages sinusoidal and balanced, so as to minimize the impact of the load voltages on the DC bus voltage.

2) Control strategy of parallel converter

Based on the mathematical model of the parallel converter, a double closed-loop control strategy for the parallel converter under three-phase stationary coordinate is given, as shown in Fig. 7, where $i_{2\mathrm{a\_s}}$ and $u_{\mathrm{La\_s}}$ are the sampling values of $i_{2\mathrm{a}}$ and u_{La}, respectively. To reduce the steady-state errors of PI controllers, MR controllers are added in the voltage outer-loop.

The control block diagram of the current inner-loop is shown in Fig. 8. To eliminate the disturbance of the load voltage to the current loop, the load voltage (u_{La}) feedforward control is added to the current inner-loop.

The transfer function of the current sampling $G_{\mathrm{sami}}(s)$ in the parallel converter can be expressed as:

$$G_{\mathrm{sami}}(s) = k_{\mathrm{sam\_pari}}/(T_{\mathrm{sam\_pari}}s + 1) \tag{37}$$

where $k_{\mathrm{sam\_pari}}$ and $T_{\mathrm{sam\_pari}}$ are the sampling coefficient and filter delay time (s) of the current $i_{2\mathrm{a}}$, respectively.

The current inner-loop represents the tracking performance, so it is designed as a type I system. A PI controller is employed by the current inner-loop, and its transfer function $G_{\mathrm{PIi}}(s)$ can be expressed as:

$$G_{\mathrm{PIi}}(s) = k_{\mathrm{parip}} + k_{\mathrm{parii}}/s \tag{38}$$

where k_{parip} and k_{parii} are the proportional and integral coefficient of $G_{\mathrm{PIi}}(s)$, respectively.

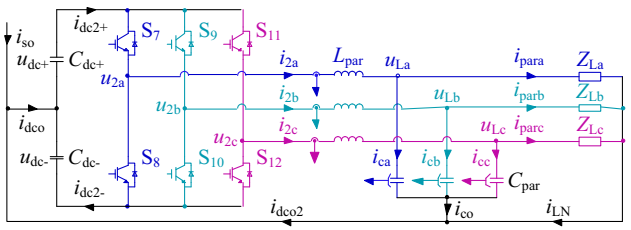

Fig. 6 Parallel converter topology

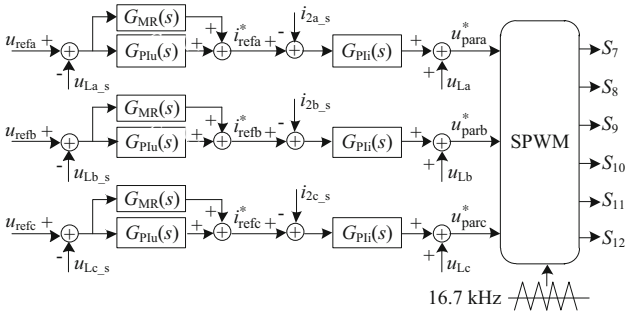

Fig. 7 Control block diagram of the parallel converter

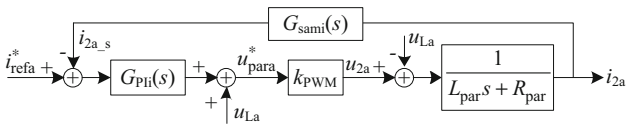

Fig. 8 Control block diagram of the current inner-loop

After the zero point of $G_{\mathrm{PIi}}(s)$ and the pole point of $1/(L_{\mathrm{par}}s + R_{\mathrm{par}})$ cancellation, the transfer function of the current open-loop $G_{\mathrm{op\_pari}}(s)$ can be expressed as:

$$G_{\mathrm{op\_pari}}(s) = \frac{k_{\mathrm{PWM}}}{L_{\mathrm{par}}s + R_{\mathrm{par}}} G_{\mathrm{PIi}}(s) G_{\mathrm{sami}}(s) = \frac{k_{\mathrm{op\_pari}}}{s(T_{\mathrm{sam\_pari}}s + 1)} \tag{39}$$

where the current open-loop gain $k_{\mathrm{op\_pari}} = k_{\mathrm{PWM}}\, k_{\mathrm{sam\_pari}}\, k_{\mathrm{m}}$, and the proportional relationship $k_{\mathrm{m}} = k_{\mathrm{parip}} / L_{\mathrm{par}} = k_{\mathrm{parii}} / R_{\mathrm{par}}$.

The parameter calculation of $G_{\mathrm{PIi}}(s)$ is the same as that of the series converter. Let the shear frequency of the current loop $\omega_{\mathrm{pari\_cut}} = 3340\pi$ rad/s, and the parameters of $G_{\mathrm{PIi}}(s)$ are: $k_{\mathrm{parip}} = 0.96$ and $k_{\mathrm{parii}} = 319$.

The transfer function of the current closed-loop $G_{\mathrm{cl\_pari}}(s)$ can be expressed as:

$$G_{\mathrm{cl\_pari}}(s) = \frac{k_{\mathrm{PWM}} k_{\mathrm{m}}}{T_{\mathrm{sam\_pari}}s^2 + s + k_{\mathrm{op\_pari}}} \tag{40}$$

Ignoring the higher order term $T_{\mathrm{sam\_pari}}s^2$ in (40), $G_{\mathrm{cl\_pari}}(s)$ can be reduced order to:

$$G_{\mathrm{cl\_pari}}(s) = \frac{k_{\mathrm{PWM}} k_{\mathrm{m}}}{s + k_{\mathrm{op-pari}}} \tag{41}$$

The control block diagram of the voltage outer-loop is shown in Fig. 9, where the PI + MR controllers are employed for the load voltages, and their transfer function is shown in (26).

The transfer function of the voltage sampling $G_{\mathrm{samu}}(s)$ can be expressed as:

$$G_{\mathrm{samu}}(s) = k_{\mathrm{sam\_paru}} / (T_{\mathrm{sam\_paru}}s + 1) \tag{42}$$

where $k_{\mathrm{sam\_paru}}$ and $T_{\mathrm{sam\_paru}}$ are the sampling coefficient and filter delay time (s) of the voltage u_{La}, respectively.

The PI controller transfer function of the voltage outer-loop $G_{\mathrm{PIu}}(s)$ can be expressed as:

$$G_{\mathrm{PIu}}(s) = k_{\mathrm{parup}} + k_{\mathrm{parui}}/s \tag{43}$$

where k_{parup} and k_{parui} are the proportional and integral coefficient of $G_{\mathrm{PIu}}(s)$, respectively.

The transfer function of the voltage open-loop $G_{\mathrm{op\_paru}}(s)$ can be expressed as:

$$G_{\mathrm{op\_paru}}(s) = \frac{k_{\mathrm{op\_paru}}(k_{\mathrm{parup}}s + k_{\mathrm{parui}})}{s^2(T_{\sum \mathrm{par}}s + 1)} \tag{44}$$

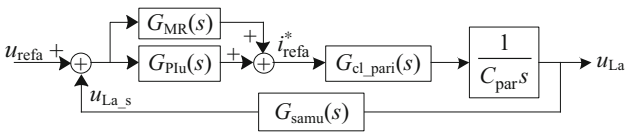

Fig. 9 Control block diagram of the voltage outer-loop

where the voltage open-loop gain $k_{\mathrm{op\_paru}} = k_{\mathrm{sam\_paru}} / (k_{\mathrm{sam\_pari}}\, C_{\mathrm{par}})$, and the sum of the small inertia time constants $T_{\sum \mathrm{paru}} = T_{\mathrm{sam\_paru}} + 1/(k_{\mathrm{op\_pari}})$.

Let the shear frequency of the voltage loop $\omega_{\mathrm{paru\_cut}} = 668\pi$ rad/s (1/5 of $\omega_{\mathrm{pari\_cut}}$), and the parameters of $G_{\mathrm{PIu}}(s)$ are as follows: $k_{\mathrm{parup}} = 0.16$ and $k_{\mathrm{parui}} = 77.6$.

The load voltage references u_{refabc} can be expressed as:

$$\begin{cases} u_{\mathrm{refa}} = U_{\mathrm{ref}} \sin \omega t \\ u_{\mathrm{refb}} = U_{\mathrm{ref}} \sin(\omega t - 2\pi/3) \\ u_{\mathrm{refc}} = U_{\mathrm{ref}} \sin(\omega t + 2\pi/3) \end{cases} \tag{45}$$

where U_{ref} is the desired amplitude of load voltages.

The current loop references i^*_{refabc} can be expressed as:

$$\begin{cases} i^*_{\mathrm{refa}} = (u_{\mathrm{refa}} - u_{\mathrm{La\_s}}) G_{\mathrm{PIMR}}(s) \\ i^*_{\mathrm{refb}} = (u_{\mathrm{refb}} - u_{\mathrm{Lb\_s}}) G_{\mathrm{PIMR}}(s) \\ i^*_{\mathrm{refc}} = (u_{\mathrm{refc}} - u_{\mathrm{Lc\_s}}) G_{\mathrm{PIMR}}(s) \end{cases} \tag{46}$$

The modulation signals of the series converter u^*_{parabc} can be expressed as:

$$\begin{cases} u^*_{\mathrm{para}} = (i^*_{\mathrm{refa}} - i_{\mathrm{2a\_s}}) G_{\mathrm{PIi}}(s) + u_{\mathrm{La}}/k_{\mathrm{PWM}} \\ u^*_{\mathrm{parb}} = (i^*_{\mathrm{refb}} - i_{\mathrm{2b\_s}}) G_{\mathrm{PIi}}(s) + u_{\mathrm{Lb}}/k_{\mathrm{PWM}} \\ u^*_{\mathrm{parc}} = (i^*_{\mathrm{refc}} - i_{\mathrm{2c\_s}}) G_{\mathrm{PIi}}(s) + u_{\mathrm{Lc}}/k_{\mathrm{PWM}} \end{cases} \tag{47}$$

3 Case analysis of single-phase load

By employing the proposed control strategies, UPQC can compensate for unbalanced load currents caused by unbalanced loads, so that the grid currents can be kept in sinusoidal and balanced state. Here we take the most serious unbalanced loads (100% unbalanced load) as an example to do some analysis. To better illustrate the compensation effect of the UPQC for the unbalanced load current, the operation schematic and phasor diagram only with a-phase load are shown in Fig. 10.

Under the control of the series converter, the a-phase load fundamental active current i_{La} can be evenly distributed to each phase on the grid side, so the three-phase grid currents i_{Sabc} are still maintained in a sinusoidal and balanced state. Seen from the grid side, the whole system is in a three-phase balanced state. i_{Sabc} can be expressed as:

$$i_{\mathrm{Sabc}} = i_{\mathrm{La}}/3 \tag{48}$$

From (48), each phase grid current is equal to 1/3 of the load fundamental active current.

Under the control of parallel converter, the a-phase current of the parallel converter i_{para} is in phase with the a-phase grid current i_{Sa}, and provides the 2/3 load current i_{La} for the load. The b- and c-phase grid currents i_{Sb}, i_{Sc} are absorbed by the b- and c-phase of the parallel converter.

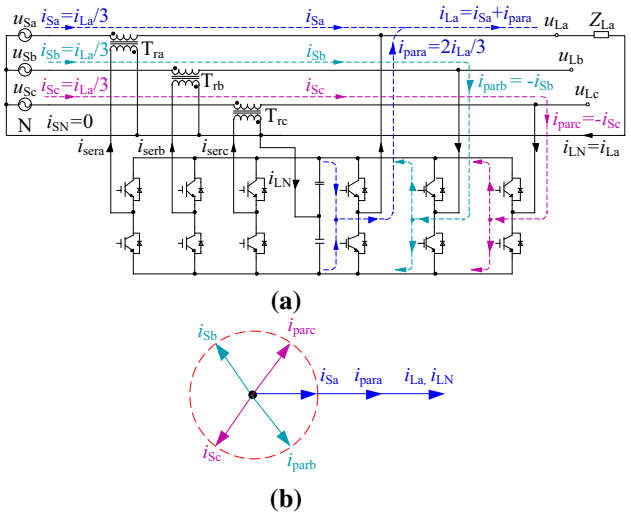

Fig. 10 Operating principle of UPQC with a-phase load

Therefore, the a-phase load current i_{La} is jointly provided by the grid and parallel converter.

The output currents of the parallel converter i_{parabc} can be expressed as:

$$\begin{cases} i_{para} = 2i_{La}/3 \\ i_{parb} = -i_{Sb} \\ i_{parc} = -i_{Sc} \end{cases} \tag{49}$$

The three-phase load currents i_{Labc} can be expressed as:

$$\begin{cases} i_{La} = i_{Sa} + i_{para} \\ i_{Lb} = i_{Lc} = 0 \end{cases} \tag{50}$$

The neutral currents on both the grid and load side i_{SN}, i_{LN} can be obtained as:

$$\begin{cases} i_{SN} = 0 \\ i_{LN} = i_{La} \end{cases} \tag{51}$$

Thus the following conclusions can be drawn on unbalanced loads: (1) Each phase grid current is 1/3 of the sum of three-phase load fundamental active currents; (2) The neutral current on the grid side is zero, whereas the neutral current on the load side is equal to the load unbalanced currents; (3) The parallel converter absorbs and converts the grid currents to ensure the operation of unbalanced loads.

4 Experimental validation

Two DSPs (TMS320F28335) are used as the controllers of the series and parallel converters. Experimental parameters are: the rms values of grid and load voltage are 220 V, their frequencies are 50 Hz; the switching frequencies of the two converters are 16.7 kHz; the positive and negative DC bus voltages are ±400 V; the a-phase rated load power is 9.35 kW; the a-phase rated load is 5.18 Ω.

The experimental results of the a-phase resistance load with the MCA are shown in Fig. 11. To verify the aforementioned important functions of the proposed MCA, the comparative experiments are carried out in terms of the sine and balance degrees of the grid currents, the neutral current of the grid side and the steady-state fluctuation and the transient drop of the DC bus voltage, as shown in Fig. 12.

The grid voltages u_{Sabc}, grid currents i_{Sabc}, load voltages u_{Labc} and load currents i_{Labc} are shown in Fig. 11a–d. The percentage of unbalanced load is 100% only with a-phase rated load. It can be seen from Fig. 11b, c that three-phase grid currents i_{Sabc} and load voltages u_{Labc} remain in a good sinusoidal and balanced state under the proposed control strategies. Moreover, the grid currents i_{Sabc} with the system loss are controlled to be in phase with the grid voltages, and their rms values are 16.9 A, 16.6 A and 16.5 A, respectively, which are approximately 1/3 of the a-phase load current i_{La} (42.6 A rms). Compared with Fig. 12a, because of the influence of the DC bus voltage fluctuations (as described in Section 2.1), the sine and balance degrees of the grid currents i_{Sabc} without the proposed MCA are obviously poorer, and the rms values of the currents i_{Sabc} are 18.6 A, 19.7 A and 20.5 A, respectively.

The output currents of parallel converter i_{parabc} are shown in Fig. 11e. The a-phase current i_{para} is in phase with the a-phase grid voltage u_{Sa}, indicating that the a-phase of the parallel converter supplies 2/3 of the load current for the a-phase load. The b- and c-phase currents i_{parb}, i_{parc} are reversed with the b- and c-phase grid voltage u_{Sb}, u_{Sc}, indicating that the b- and c-phase of the parallel converter absorb 1/3 of load current from the grid side.

The neutral current of the load side i_{SN} is equal to the a-phase load current i_{La} in Fig. 11f. Under the control of series and parallel converters, the neutral current of the grid side i_{SN} is very small, fluctuating in a small range around the zero axis, and its rms value is 2.72 A, which is much smaller than the neutral current of the load side i_{LN} (44.8 A rms). Compared with Fig. 12b, the neutral current of the grid side i_{SN} (4.77 A rms) without MCA is larger than that with MCA.

The steady-state positive and negative DC bus voltages $u_{dc\pm}$ are shown in Fig. 11g. It should be noted that the neutral current of the load side flows into the neutral point of the positive and negative DC capacitors $C_{dc\pm}$, and this will result in the DC bus voltage fluctuations. The fluctuation frequencies of the positive and negative DC bus voltages are 50 Hz, which coincides with the a-phase load current frequency, and the fluctuation frequency of the total

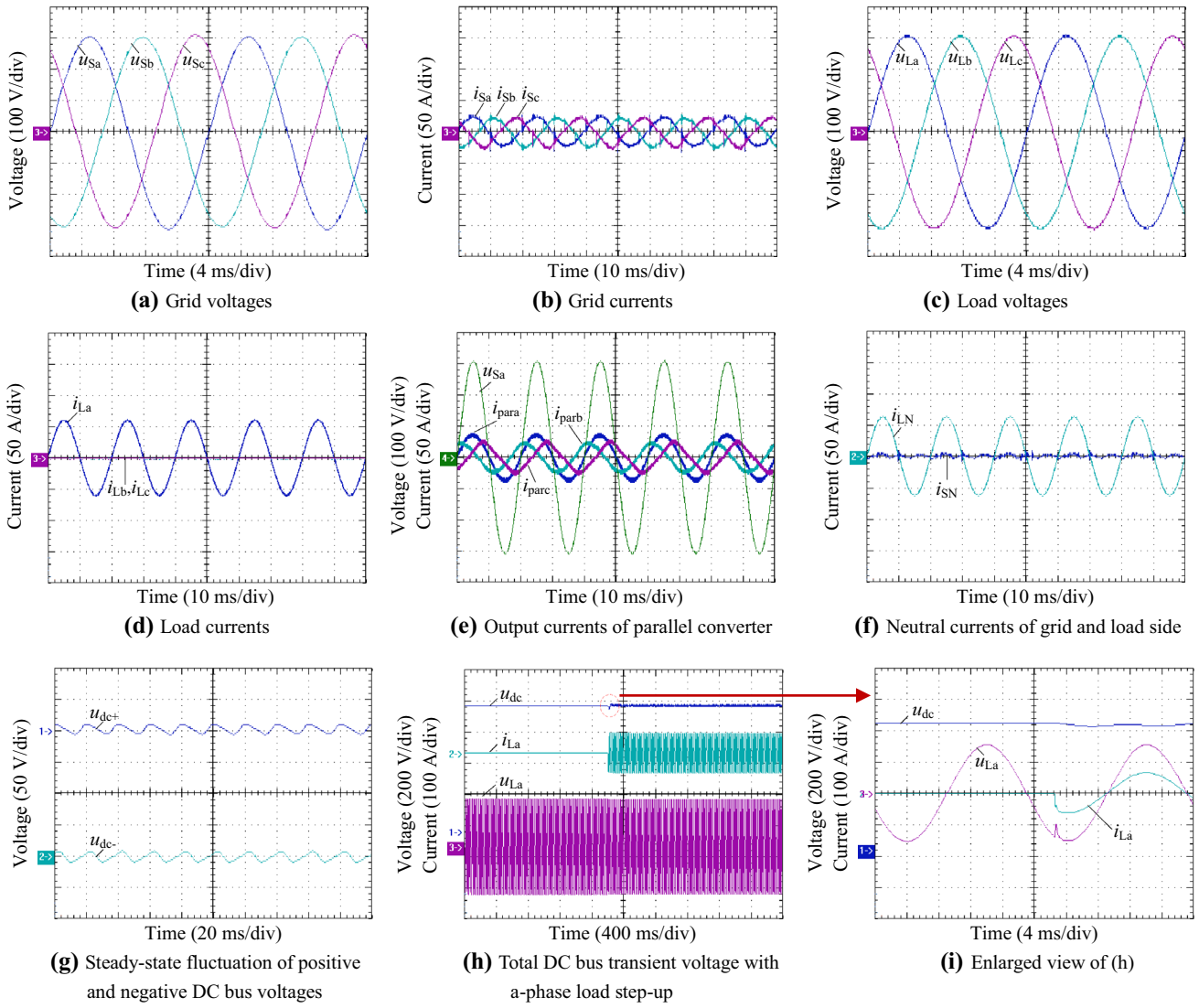

Fig. 11 Experimental results of the a-phase resistance load with MCA

DC bus voltage is twice the fundamental frequency. Compared with Fig. 12c, the positive and negative DC bus voltage fluctuations without the MCA are larger than those with the MCA because of the increased unbalanced degree of the grid currents.

The grid currents i_{Sabc} cannot immediately respond to the sudden change of a-phase load from empty-load to full-load in Fig. 11h, so a certain adjustment time is needed. During this adjustment time, the positive or negative DC bus capacitor provides energy for the a-phase load, and thus the total DC bus voltage u_{dc} experiences a large drop. Fig. 11i is an enlarged view of Fig. 11h. Compared with Fig. 12d, it can be seen that the DC bus voltage transient drop without MCA is much larger.

The experimental results in Fig. 12 also prove that there is a mutual influence between the DC bus voltage fluctuation and the neutral current of the grid side.

To verify the robustness of the UPQC based on the proposed MCA control strategy, the experimental results of the a-phase nonlinear load (diode bridge rectifier with a capacitive load) are added in this section, as shown in Fig. 13. The sine degree of the grid currents i_{Sbac} will be deteriorated, as shown in Fig. 13a, but the UPQC is still able to control i_{Sbac} to be balanced, and the rms values of i_{Sabc} are 7.06 A, 7.27 A and 7.07 A. The a-phase load voltage u_{La} appears to be distorted because of the influence of the a-phase nonlinear load, as shown in Fig. 13b. Figure 13c shows the three-phase load currents i_{Labc}, where the a-phase load current i_{La} has the characteristics of periodic load and no-load. The a-phase of the parallel

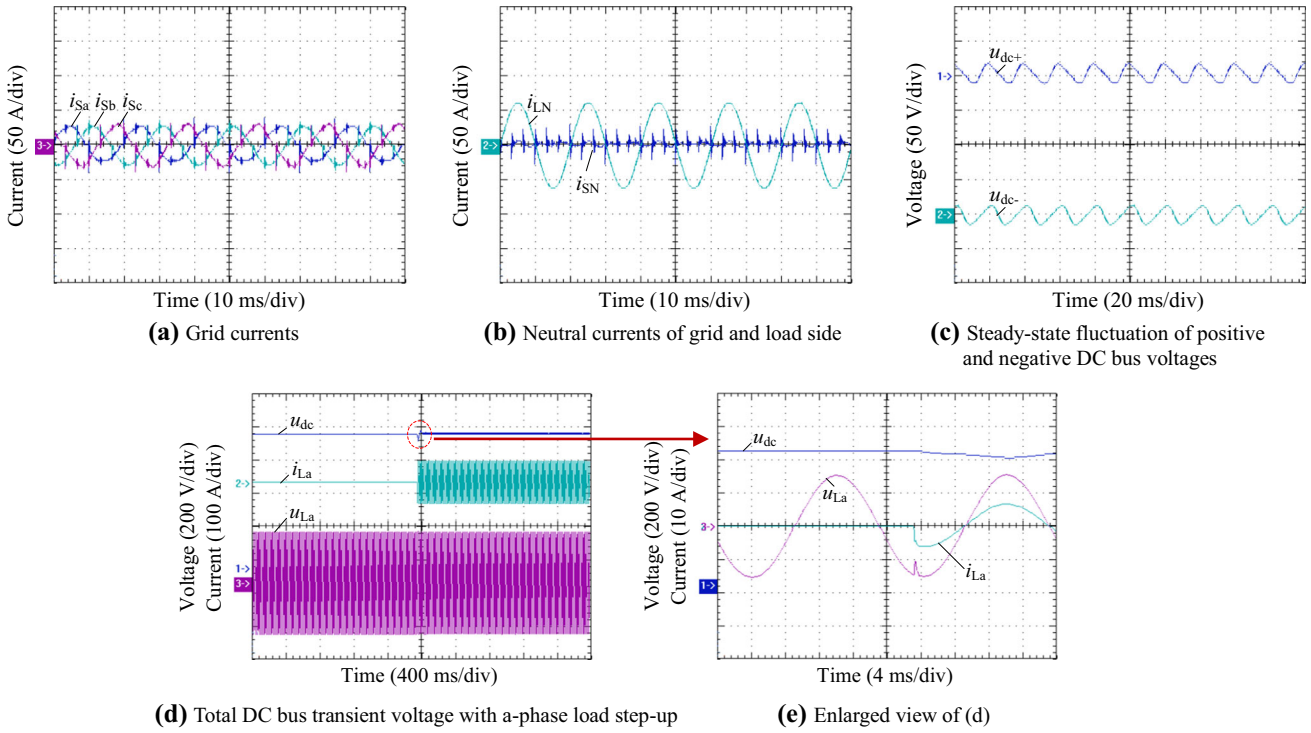

Fig. 12 Experimental results of the a-phase resistance load without MCA

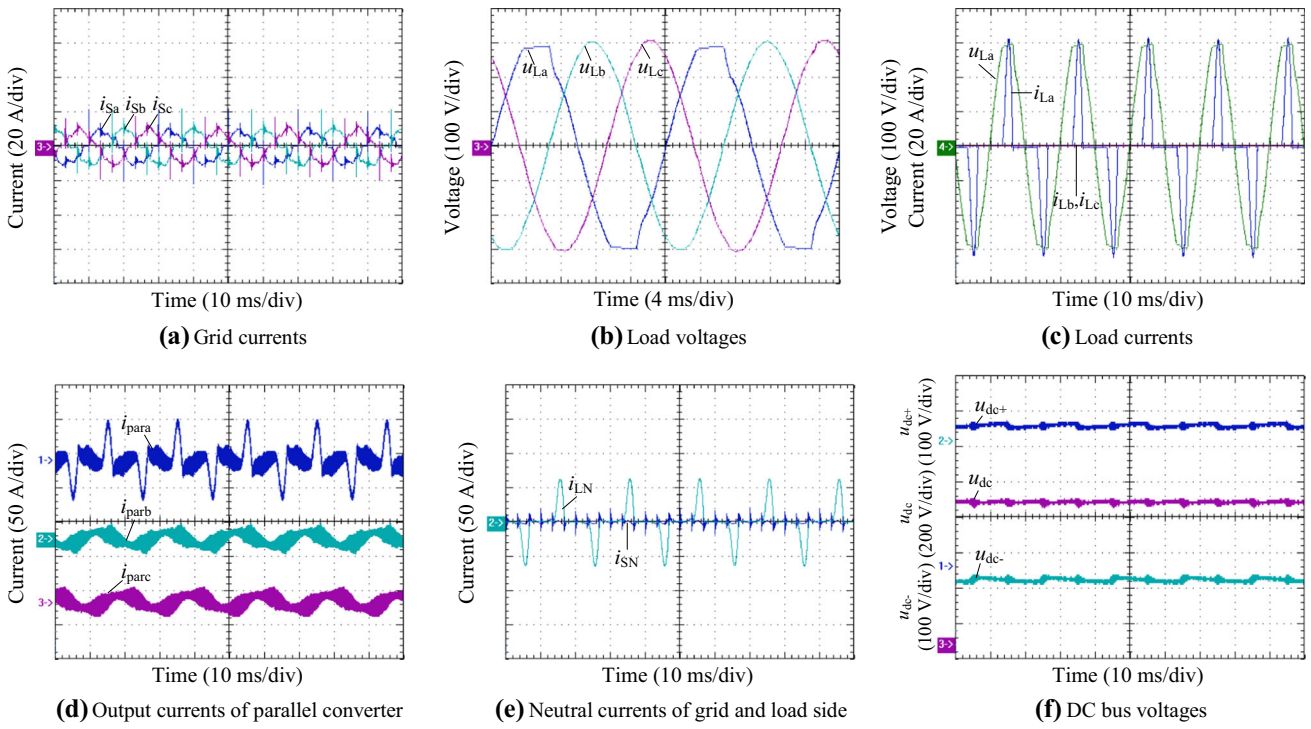

Fig. 13 Experimental results of the a-phase nonlinear load with MCA

converter provides a part of the fundamental active current and all of the harmonic currents i_{para} for the nonlinear load. Meanwhile the b- and c-phase absorb the grid currents, as shown in Fig. 13d. The neutral current i_{SN} is obviously smaller than the current i_{LN}, as shown in Fig. 13e. The unbalanced grid currents and the larger neutral current of the load side will cause the fluctuations in the DC bus voltage, as shown in Fig. 13f.

5 Conclusion

Tackling the problem of three-phase grid currents imbalance caused by three-phase unbalanced loads, first the mathematical model of a three-phase four-wire UPQC is established. The mechanism of DC bus voltage fluctuations is analyzed in detail, and the mutual influence between the DC bus voltage fluctuations and the unbalanced grid currents is described. Then the control strategy based on the MCA is given under a three-phase stationary coordinate. The experimental results show that:

1) The balance control of the grid currents with 100% unbalanced load can be realized by the given control strategy based on the proposed MCA;
2) The neutral current of the grid side fluctuates in a small range around zero;
3) The steady-state fluctuation and the transient drop of the DC bus voltage can also be restrained;
4) The system has a greater robustness under the single-phase nonlinear load.

Therefore, the correctness of the theoretical analysis and the feasibility of the control strategy based on the MCA are verified. On the basis of the theoretical analysis, we believe this paper also draws important conclusions, which are of significance to related academic research as well as engineering.

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