JOM, Vol. 70, No. 10, 2018
https://doi.org/10.1007/s11837-018-3081-z
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NANOPOROUS AND NANOARCHITECTURED MATERIALS

A Review of Nanoporous Metals in Interconnects

KASHYAP MOHAN,[1] NINAD SHAHANE,[1] RAN LIU,[2,3] VANESSA SMET,[1,4] and ANTONIA ANTONIOU[2,5]

1.—3D Systems Packaging Research Center, Georgia Institute of Technology, Atlanta, GA, USA. 2.—The Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, GA, USA. 3.—KLA-Tencor, Milpitas, CA, USA. 4.—e-mail: vanessa.smet@prc.gatech.edu. 5.—e-mail: antonia.antoniou@me.gatech.edu

Interconnections in semiconductor devices need to provide a seamless electrical, thermal, and mechanical link to different parts of the circuit. Since the move away from lead-based solders due to toxicity concerns, the search has been on for materials that can provide desirable attributes before, during, and after bonding. While lead-free solders have been extensively used as a replacement, they are now reaching their limits in terms of pitch scaling, as well as, electrical and thermal properties, forcing the semiconductor industry to look for alternative material systems for the next interconnection node. This review provides an overview of key properties needed in metal interconnections and possible use of nanoporous metals due to ease of fabrication, nanostructured ligaments, and other key physical attributes.

INTRODUCTION

Nanoporous (NP) metals are part of a broader category of porous media or metal–air composites that can extend the range of properties and therefore applications of the parent (solid wall) material.[1] The solid mass fraction (or relative density) for NP metals is typically greater that 30%[2–8] with open-cell structure, formed by a random arrangement of nanosized ligaments and junctions through the volume. Abundant information exists on the physical properties of porous media with ligaments and porosities in the micron or above range,[9] but several modifications are necessary for NP metals due to their higher relative density[3] and the interplay of nanosized ligament properties, which can substantially influence their overall physical properties; For example, NP metals have been reported to have different scalings of strength[4,5,10–13] and stiffness[3] than expected. NP metals, with their open-cell structure, bicontinuous porosity, and resulting high surface-to-volume ratio, have been proposed as catalysts,[14–16] sensors,[17–19] actuators,[18,20] radiation-resistant coatings,[21] and optical[22] or lipid bilayer platforms.[23]

Kashyap Mohan and Ninad Shahane have contributed equally to this work.

This review discusses the favorable attributes of NP metals (and NP copper in particular) that make them promising interconnection materials for power electronics and microelectronics applications.[24–26] In power electronics, nanoporous copper is proposed as a low-cost alternative to Ag sintering for die-attach interconnections, with a drastic reduction in organic volatile content, superior design flexibility for control of bondline thickness and stress management, and improved manufacturability. In microelectronics, NP copper can be used as low-modulus capping on top of a copper pillar to improve manufacturability, of direct Cu-Cu bonding particular tolerance to non-coplanarities and warpage, while still retaining pitch scalability, owing to their solid state.

FUNDAMENTALS OF INTERCONNECTIONS AND ASSEMBLY

Electronic systems are made of multiple interconnected semiconductor devices and passive components to realize their electronic functions. Most leading-edge active components contain billions of transistors or bits, so they need to be connected to other parts of the system, such as other integrated circuits, as in multichip modules for digital systems with high data rates, or to passive components to form functional circuits such as radiofrequency (RF)

 (Published online August 27, 2018)

or power modules. Thus, for the system to function, all 100 or so components need to be interconnected, powered, cooled, and protected. These components are interconnected on package substrates such as printed circuit boards (PCBs) with several copper wiring layers. Interconnections are the physical links that electrically, mechanically, and thermally connect different levels of packaging, such as semiconductor chips to substrates, as shown schematically in Fig. 1. Assembly refers to the process by which these interconnections are formed.

While the primary function of interconnections is electrical, this can only be achieved by using materials and processing techniques that feature appropriate mechanical, electrical, and thermal properties. Thus, three key considerations are: (a) interconnection materials with the required electrical, thermal, and mechanical properties, (b) processing of these materials to form electrical joints (i.e., assembly), and (c) mechanical aspects such as stresses and strains that develop in these joints due to thermal expansion mismatch between active devices, e.g., Si, GaAs, SiGe, GaN or SiC devices with coefficient of thermal expansion (CTE) between 3 ppm/K and 6 ppm/K and package substrates and organic boards with CTEs ranging from 3 ppm/K to 17 ppm/K.

Interconnections have three primary functions: (1) electrical: to provide a path for signal and power distribution in the packaged system; (2) mechanical: to provide mechanical reliability of the interconnected system; and (3) thermal: to provide a heat transfer path to efficiently dissipate the heat generated in the semiconductor devices through the substrate. Interconnections, therefore, play a critical role at chip, package, and board levels for the system's overall performance and have to be carefully designed, taking into account material, geometry, processing, and manufacturability considerations. Ideal properties of an interconnection system can be defined as follows:

- *Electrical*: Resistance, capacitance, and inductance are important properties of any interconnection technology. To achieve the highest signal transmission speed at low loss and low power and maintain signal integrity, the resistance, capacitance, and inductance of the interconnections need to be minimized. The amount of current that can be passed through an interconnection is fundamentally limited by the interconnection material and geometry. Excessive current densities can create failures in interconnections by electromigration.[27,28]
- *Thermal*: Interconnections also serve as thermal interfaces to transfer heat between semiconductor devices and the package substrate. Heat is generated within chips as they operate, due to intrinsic power losses. Efficient removal of this heat through the substrate is critical for maintaining a reasonable temperature in the semiconductor, particularly in analog and power applications. Interconnections provide the necessary heat transfer path between devices and substrate, and high-thermal-conductivity materials are highly desirable. Metals and alloys, with both high electrical and thermal conductivities, therefore represent ideal candidate materials for interconnections.
- *Mechanical*: The mechanical behavior of an interconnection is important because its potential failure can result in electrical failure. The interconnection materials and their temperature dependence are critical parameters as they directly impact on the reliability of the interconnections. Young's modulus and yield strength are two critical properties that affect both themomechanical fatigue and drop performance. Thermomechanical reliability is governed by the ability of the interconnection material to prevent plastic deformation, therefore benefitting from higher modulus and yield strength values. On the contrary, drop performance relies on the ability of the interconnection material to absorb shock energy, necessitating more compliant (lower-modulus) materials.
- *Reliability:* As electronic systems make their way into every part of our lives, from communication and computing systems to self-driving cars and more electric aircrafts, reliability and safety have become of utmost concern. Failures of mobile phones or laptops may be inconvenient, but malfunction of onboard electronic systems, for instance, in high-speed trains, electric cars or planes, can endanger lives. Electronic systems with poor reliability fail to perform their intended function and often require additional maintenance over the product life, which increases cost. Any electronic product is expected to perform reliably, sometimes in harsh environments, for its normal duration of use, which varies greatly from product to product.

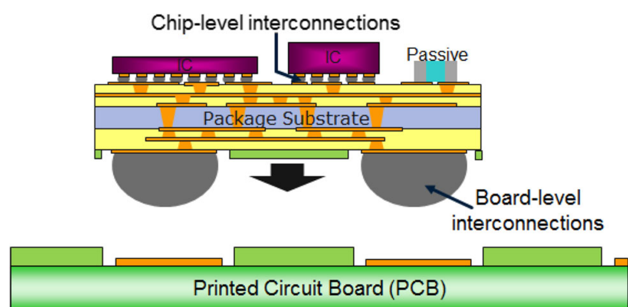

Fig. 1. Anatomy schematic of interconnections between chip and package substrate, and package substrate and mother board.

Electronic systems must satisfy stringent and sometimes conflicting requirements for performance and reliability. Interconnections play a critical role in achieving high reliability. Interconnection

materials and geometries must, therefore, be carefully selected to minimize mechanical stresses and strains induced, for example, by expansion mismatch that can cumulatively lead to catastrophic failure of the product.

Assembly is the process by which interconnections are formed, primarily through a metallurgical bond joining two metal interfaces. Metallurgical or metallic bonding relies on self- or inter- diffusion between metal interfaces. A metallurgical bond is formed between two interfaces made either of the same metal or of two or more different metals. When the two interfaces are made of the same metal, the metallurgical bond is formed through self-diffusion, resulting in a seamless bonded interface. When the two interfaces are made of two or more different metals, the metallurgical bond is formed through interdiffusion, resulting in formation of intermetallic compounds at the bonded interface based on the phase diagram of the reacting metals.

The reaction occurring during metallurgical bonding is enabled by the motion (transport) of atoms of one metal into another, provided external energy is brought into the system to overcome the energy barrier to diffusion, E_a, following an Arrhenius equation: $D = D_0 e^{\left(\frac{-E_a}{RT}\right)}$, where R is the universal gas constant equal to 8.314 J/mol K, T is the temperature in K, and D_0 is the initial diffusivity value of the diffusing metal in the base metal in m^2/s. Atomic contact between the two metal interfaces to be bonded is required to achieve diffusion. While surface roughness, non-coplanarities, and oxidation tend to increase the energy barrier to diffusion, external application of heat, pressure, or ultrasonic energy can be used to reduce it. Diffusivity tends to increase with temperature, reaching its peak as the diffusing metals change phase and become liquid. Heat is typically applied to achieve metallurgical bonding, and metals and alloys with relatively low melting point T_m are preferred to form metallic bonds in the shortest time. The bonding time directly impacts the throughput of the process in units per hour (UPH), which in turn affects cost. Bonding parameters such as time, temperature, and applied pressure are critical factors in the development of a suitable assembly process respecting the thermal budget and throughput required by the product and application. These considerations are summarized in Fig. 2 as guidelines for selection of materials with desired properties during initial, assembly, and operating conditions. As can be seen, any new process should be compatible with existing lithography protocols. During assembly, interconnection materials need to have low to moderate compliance, but the end product needs to have low electrical resistivity, high thermal conductivity, and stability as close as possible to high-melting-point, dense (bulk) metals.

INTERCONNECTION MATERIALS AND TECHNOLOGY OVERVIEW

Based on these considerations, tin-lead solders with a variety of compositions having Pb content from 37% to 95% were used prolifically in industry due to their ease of fabrication, relatively low melting point (in particular, 183°C for the eutectic composition), and outstanding reliability performance during operation.[29–34] However, concerns over the toxicity of lead led to a worldwide ban of its use in electronics packaging. Tin-based lead-free alloys made of mixtures of Sn, Cu, and Ag, e.g., SnCu0.7 or SnAg3.5, were widely adopted as a replacement technology, despite their slightly higher melting points in the range of 220–230°C and slightly worse thermomechanical properties compared with leaded solders.[34–36] Solder-based interconnections using lead-free solders have become a near-universal solution for assembly of a

Before Assembly	During Assembly	After Assembly
• Manufacturable wafer bumping process compatible with standard lithography processes and existing infrastructures • Fine control of interconnection thickness and composition	• High tolerance to non-coplanarities & warpage • Low elastic modulus • High wettability • High diffusivity at <250°C • Controllable oxidation	• Low electrical resistivity • High current carrying capability • High thermal conductivity • Thermodynamical stability • High shear strength • Good fatigue performance • Good resistance to mechanical shocks

Fig. 2. Desired properties of interconnections during initial, assembly, and end product.

wide-range of electronic systems, including digital, analog, and power devices, owing to their: (1) self-alignment capability through surface tension in molten phase, (2) low-temperature assembly at less than 250°C, and (3) corrosion resistance, among other benefits. Two types of interconnections have been pursued in parallel, as described in Fig. 3: bumped interconnections defined by their pitch, i.e., the distance between the centers of interconnections, for (digital, analog, and low-power) microelectronics applications, and large-area interconnections in power electronics.

High-performance computing has been driving advances in interconnection technologies from the digital side, to scale interconnection pitches following the transistor scaling trend governed by Moore's law. Pitch scaling is accompanied by a necessary reduction in solder volume to prevent solder bridging and, subsequently, in the interconnection standoff height. This aggravates mechanical stresses and strains in the solder joints, resulting in reliability concerns and limiting further scaling of traditional solder bump interconnections.[37] The next-generation technology, referred to as Cu pillar interconnection technology, shown in Fig. 4, was introduced in the 1990s for further pitch scaling. In this approach, Cu pillars with high aspect ratio, acting somewhat as compliant interconnections but with solder caps, were developed. The Cu post was introduced to increase the standoff height of the interconnections, thereby reducing strains in solders and, subsequently, improving the joints' reliability. Cu pillar interconnections were first implemented in production in 2005 in RF power amplifiers and front-end modules to improve their electrical and thermal performance, reliability, and cost. Cu pillar technology has been demonstrated at pitches down to 35 μm in production today. However, further pitch scaling is hindered by aggravated risks of bridging, difficulties in controlling interfacial reactions with further reduced solder volumes, and fundamental material limitations, including maximum admissible current densities of 10^4 A/cm^2 and operating temperatures of 150°C or below 0.3–0.5 × T_{m} to prevent catastrophic creep failure.[38–41]

Solid–liquid interdiffusion (SLID) bonding, shown in Fig. 4, also known as transient liquid-phase (TLP) bonding or diffusion soldering, was proposed and developed as the next natural evolution to extend the applicability of solder-based technologies to finer pitches. It has been extensively researched and demonstrated in a wide range of material systems, including Ag-Sn, Ag-In, Au-Sn, Au-In, and Ni-Sn.[42–44] Intermetallic compounds have higher melting points and provide higher thermal stability and greater current-carrying capability than solders by an order of magnitude or more.[45]

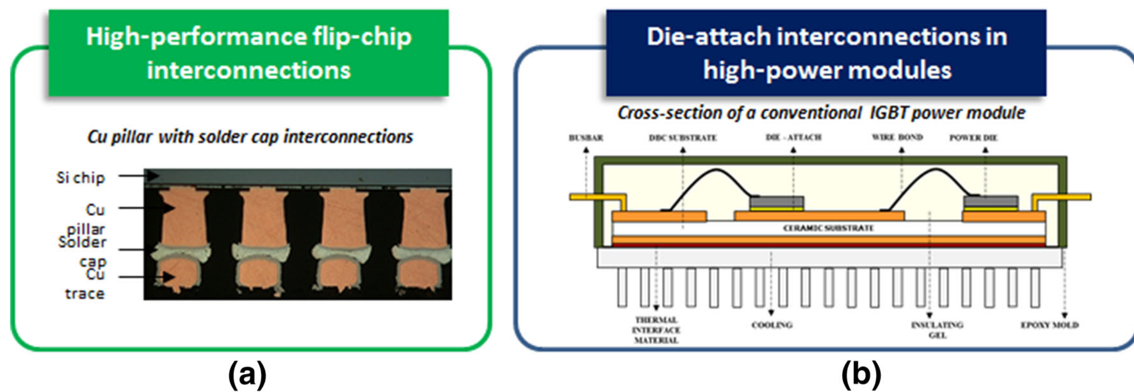

Fig. 3. Two types of solder-based interconnections: (a) Cu pillar with solder caps used in high-performance computing, and (b) die-attach interconnections used in power electronic modules.

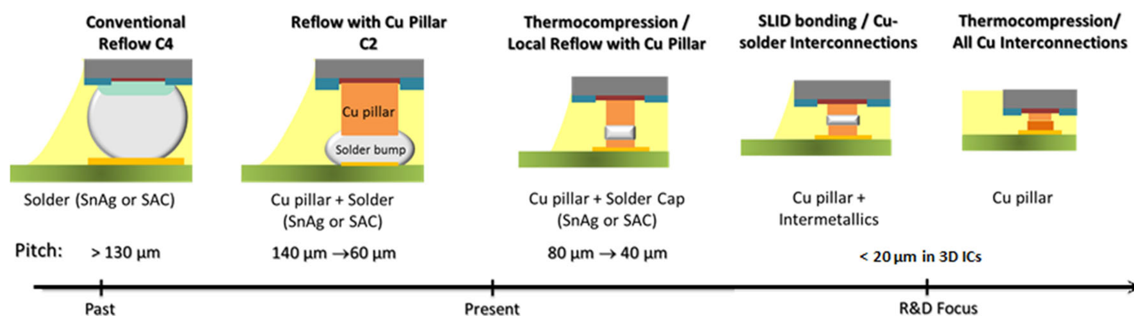

Fig. 4. Evolution of interconnection technologies in high-performance computing.

SLID bonding retains the ease of processability of solders while enabling finer pitches and performance improvements. However, intermetallics are typically stiff and brittle, which results in thermomechanical stresses in active devices that must be managed to achieve reliability.[46–49]

Beyond solder-based systems, all-Cu interconnections have been extensively pursued by the semiconductor industry as the ultimate interconnection node. Copper has outstanding electrical and thermal conductivities, thermal stability at temperatures exceeding 300°C, as well as excellent power-handling capability, two orders of magnitude higher than that of traditional solders. In addition, copper is relatively inexpensive and compatible with back-end-of-line processes and infrastructures, making it an ideal candidate interconnection material.[50,51] As a solid-state interconnection and assembly (no molten phase in assembly) technology, all-Cu interconnections can be viewed to scale to ultrafine pitches of 5 μm and below. Direct Cu-Cu bonding faces many fundamental material and process challenges that have hindered technology development, including: (1) room-temperature oxidation, (2) low diffusivity at temperatures below 300°C, and (3) low tolerance to non-coplanarities and warpage due to relatively high elastic modulus. For standard Cu pillar technology, these fundamental challenges can be addressed through: (a) fluxing under assembly to prevent oxidation, (b) high diffusivity of solder in molten form at 250°C, and (c) high compliance and fatigue life due to the low elastic modulus of solders, respectively. However, such solutions cannot be applied to direct Cu-Cu bonding because: (a) of the incompatibility of fluxing with typical direct Cu-Cu bonding conditions, (b) Cu has a melting point of 1081°C and undergoes comparatively slower kinetics under solid-state diffusion, and (c) Cu has a relatively high modulus of $\sim$ 121 GPa compared with that of solders.

Consequently, existing technologies rely heavily on selective activation of the bonding surface to ensure perfect contact and high diffusivity across the Cu-Cu interface for metallurgical bonding, as well as involving expensive planarization steps to eliminate non-coplanarities. Essentially, current state-of-the-art technologies in direct Cu-Cu bonding require high bonding forces, assembly in vacuum, inert or reducing environments with temperatures far greater ($>$ 300°C) than that used for solder-based reflow, and long annealing times with expensive chemical–mechanical polishing steps.[52–59] This limits their adoption to wafer-level packaging (WLP). Direct Cu-Cu bonding using capillary bridging of nano-Cu inks under evaporation was recently proposed by IBM Zurich.[60] This technology reintroduces a low-modulus viscous phase, playing a similar role to the solder caps in Cu pillar technology, to enhance wettability and compliance, two critical properties in assembly that are lost when shifting from solders to solid-state systems. Nanomaterials such as pastes and inks benefit from high surface area and can, therefore, sinter at low temperatures to achieve strong joints with high electrical and thermal performance after densification.[61–65]

A similar technology evolution was observed for die-attach interconnections in high-power modules, as shown in Fig. 5, primarily motivated by the need for increased operating temperatures and increased reliability concerns. The rise of wide-bandgap semiconductors has accelerated development of alternative technological solutions to traditional solders with improved heat removal capability while still providing robust electrical connection. While high-temperature solder alloys such as Au-Ge and Au-Sn eutectic have been considered, the prohibitive cost of Au has limited their wide adoption. Like in digital applications, use of TLP/SLID bonding technologies has been proposed but faces many manufacturability and reliability challenges and has, therefore, only met with limited adoption in high-volume manufacturing by Infineon.[66–68] Sintering of nanosilver pastes has also gained momentum in the last decade as an alternative to high-lead solders in high-temperature applications,[69–71] as shown in Fig. 5.[69] The resulting sintered joints have outstanding thermal and electrical conductivities as well as thermal stability at temperatures exceeding 200°C, outshining the performance of lead-free solders.[69] Despite early adoption by key industry players such as Semikron, ABB, and Infineon, Ag sintering has only achieved, so far, limited production, as it faces manufacturability and cost challenges that have yet to be fully addressed.[72] Silver sintering pastes typically require noble interfaces such as Au or Ag to form a strong bond, which increases the overall cost.[73–75] In addition, sintered joints suffer from retained porosity due to incomplete densification and voids caused by evaporation of organic volatiles, present to prevent agglomeration of the particles prior to sintering.[76] Pores and voids degrade the mechanical, thermal, and electrical properties of the sintered joints. Furthermore, they are found to coalesce and grow during temperature cycling in operation, and can act as precracks and, ultimately, lead to early failure of the joints.[74] Therefore, sintered joints with over 90% densification are highly desirable. However, higher densification also translates into high modulus, which can induce severe mechanical stresses in thin active power devices and limit scalability at large die sizes. Sintering of Cu nanoparticles has also received attention as a lower-cost alternative, with comparable electrical and thermal properties to Ag. However, it inherently faces the same limitations as Ag sintering. Moreover, oxidation of copper nanoparticles before, during, and after sintering is an additional challenge that is typically addressed through expensive surface treatments at nanoscale, possibly offsetting the cost advantage.[77,78] To address the aforementioned challenges, a new class of Cu-based

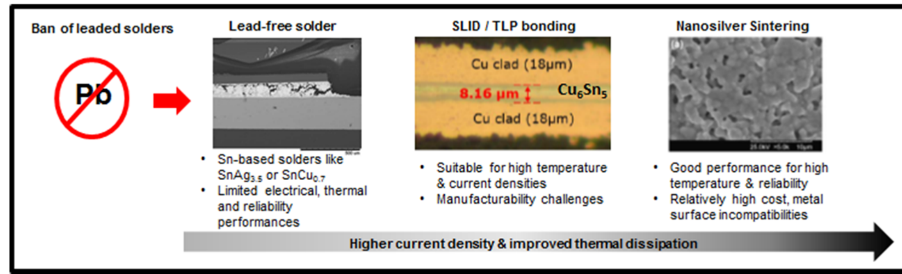

Fig. 5. Evolution of interconnection materials after ban of lead solders. Image of metastable SLID die-attach in the Cu-Sn system. Image of nanosilver sintering shows the free surface of silver nanoparticle paste after sintering at 300°C. Nanosilver sintering image reprinted with permission from Ref. 69.

die-attach technologies is, therefore, required with the processability, compliance, and cost of solders, but electrical and thermal properties matching those of Ag sintering.

WHY NANOPOROUS METALS ARE GOOD CANDIDATES

As previously mentioned, Cu is an ideal candidate that has the potential to provide a low-cost universal solution for many electronic applications. However, Cu lacks the compliance required in assembly (Fig. 2) to accommodate unavoidable non-coplanarities, making it difficult to achieve intimate atomic contact of the bonding interfaces, and ultimately, form a metallic joint through interdiffusion. The most intuitive way to lower the elastic modulus of a bulk material is to introduce porosity to form a sponge-like solid. Porosity is, however, undesirable in electronic materials as it degrades the electrical, thermal, and reliability performance and should, therefore, be eliminated during the assembly step. To that effect, porous metals have been demonstrated to sinter and densify to approach the properties of dense solids with bulk-like properties. In a similar manner to nanoparticle systems, NP metals with nanoscale feature sizes benefit from high surface area, making them more reactive and enabling sintering at temperatures below that of the melting point of the bulk material. Lastly, NP metals can be formed through chemical dealloying (etching) of a baseline alloy, which can be deposited by electrodeposition, sputtering, or through powder processing. Their fabrication process is, therefore, not only compatible with standard photolithography processes commonly used in wafer bumping, but also highly versatile with options for manufacturing of standalone die-attach films by arc or furnace melting. This opens the door for establishment of a modular supply chain, which is highly desirable for fabless end users. This makes nanoporous Cu an ideal candidate interconnection material with respect to the requirements of Fig. 2. During assembly, it will have high tolerance to non-coplanarities and warpage due to low elastic modulus, and bonding at temperatures below 250°C. After assembly, NP copper will sinter to form a strong metallic

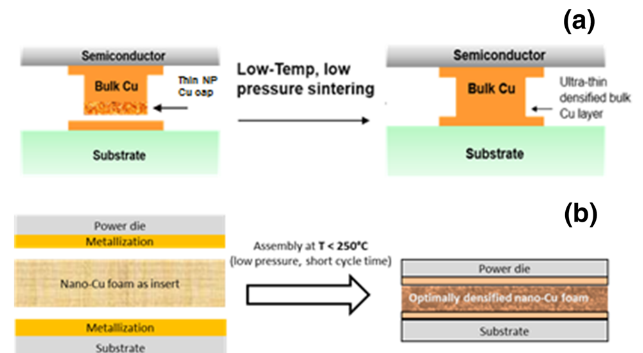

Fig. 6. Schematics demonstrating how NP Cu can be incorporated into existing microelectronics systems as: (a) a cap of NP Cu on top of Cu pillars or (b) an insert of NP Cu for die-attach film sintering.

Cu joint with over 90% density, achieving bulk-like properties such as high shear strength, high electrical and thermal conductivities, thermal stability at temperatures exceeding 300°C, and outstanding electromigration and fatigue performance.

A demonstration of the high compliance of NP Cu before sintering is shown on the tilt scanning electron microscopy (SEM) images in Fig. 6a and b, before and after frustum indentation. The resulting normalized pressure versus normalized indent depth curve is shown in Fig. 6c.[79] This particular NP copper has ligaments with size of 35 nm and modulus of 25 GPa. More information on this type of experiment and results can be found in Ref. 79. Similar properties were also reported for NP gold,[3,80,81] confirming that, compared with other solid-state interconnection materials, NP metals, and in particular NP Cu, offer sub-40 GPa modulus as-fabricated, which can compensate for the lack of wettability compared with liquid-phase bonding materials.[5,79,82] In addition, NP Cu offers the following advantages over paste approaches: (1) low-cost synthesis, (2) scalability in pitch due to solid state, (3) high design flexibility with fine control over bondline thickness and high scalability in feature sizes and aspect ratios, (4) absence of organic additives, minimizing risks of voiding due to volatiles, and subsequent corrosion and electromigration issues, and (5) better control over the

densification process and associated stresses, as well as the final properties of the joints through the initial morphology. These key attributes are detailed in the following sections. Concept schematics of implementation of this technology in digital, analog, and low-to medium-power applications is shown in Fig. 7a, with Cu pillars with NP Cu caps proposed as the next node beyond standard Cu pillars. Implementation in power electronics as high-temperature, high-performance die-attach interconnections is illustrated in Fig. 7b as a low-cost alternative to Ag sintering.

SYNTHESIS AND COMPATIBILITY WITH EXISTING INFRASTRUCTURE

NP metals are typically fabricated by dealloying, i.e., controlled etching of one (or more) elements in an alloy while the remnant self-assembles into an interconnected network of nanosized ligaments with random spatial arrangement. Pore and ligament size distributions tend to be well defined. Table I lists precursor alloys and other conditions for synthesizing NP copper as reported in literature. Table I also highlights key parameters that can impact the ligament structure, such as the precursor alloy composition, etchant type (see, for example, Fig. 2 in Ref. 83), electrolyte bath temperature,[84] free or electrochemical etching, and duration.

After etching, NP metal may retain the grain orientation and structure of the precursor, so that for the case of NP gold obtained from polycrystalline Au-Ag alloy, micron-sized grains will remain after etching.[95] For the case of amorphous alloy precursors, after etching, nanocrystalline grains and even nanosized twins may form within the ligaments.[4,5,15,96,97] The precursor alloy may be fabricated in a variety of ways from arc melting, melt-spinning to sputter or electrodeposition. For the case of deposition on wafers, precursor films that are either sputter-or electrodeposited are preferred, with the dealloying adding one additional step to the process. Depending on the precursor alloy used, it is possible that some of the alloy will remain behind. For example, in the case of Au-Ag for assembly of NP Au, up to 5 at.% of Ag may remain.[98–100] For NP copper, for the case of Cu-Si, there is no traceable amount of Si left in the NP copper,[5] but there can be remnant Zn from etching Cu-Zn or other alloys.

CONCEPT DEMONSTRATIONS

Figure 8 shows some of the earliest demonstrations of the promise of NP metals in alleviating some of the non-coplanarities. Figure 8a and b shows 100-μm NP Ag, dealloyed from Ag-Al alloys, which have also been demonstrated as standalone large-area die-attach materials.[101] These sheets were bonded under pressure of 20 MPa at 200–400°C to form metallic joints with shear strength close to that of solder alloys (30 MPa).[76] Figure 8c shows bonding of an NP Au bump at low pressure (10 MPa) and bond temperature of 200°C. The bump was formed by dealloying Au-Ag alloy that was electroplated on a silicon wafer.[102] More recently, Cu-Cu bonding of a nanoporous Cu insert, dealloyed from $Cu_{40}Al_{60}$ alloy, was demonstrated at 260°C and pressure of 10 MPa, giving a shear strength of 22 MPa.[103]

Figure 9 shows an example of an amorphous silicide alloy that was sputter deposited through a mask onto a ~ 100-mm silicon wafer. The mask was removed, then the alloy was etched in 3% HF for ~ 2 min. The resulting NP metal is shown in Fig. 9d. An additional example of a copper bump fabricated from amorphous alloy using a focused ion beam is shown in Fig. 9e and f, with the NP copper ligaments being clearly visible in Fig. 5f. Sputter deposition through a mask carries inherent complications, with the height of the overall amorphous film not achieving the same height as that of a blanket film for the same sputtering parameters

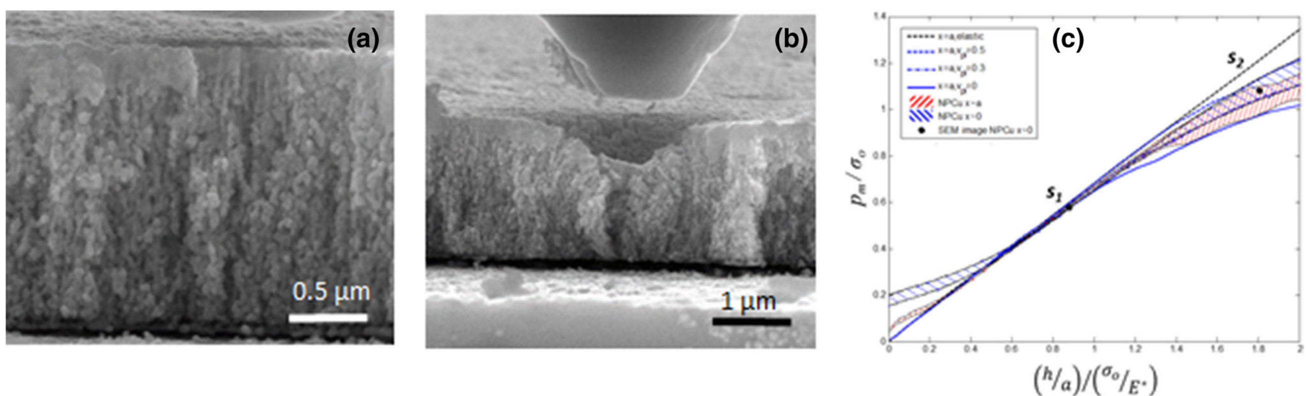

Fig. 7. Tilt SEM view of NP copper (a) before and (b) after frustum indentation. (c) Normalized pressure and normalized indent depth of the frustum indentation is shown in the early part of the deformation. The slope in the linear regime shows that the modulus is 25 GPa for the 35-nm ligament NP copper tested. Figure (c) reproduced with permission from Ref. 79.

Table I. Nanoporous (NP) copper synthesis: precursor alloy, etchant, and resulting ligament size

System	Alloy composition	Fabrication route	Etchant chemistry	Dealloying time/ temperature	Ligament size (nm)	Material properties
Cu-Mn[83,85]	$Mn_{70}Cu_{30}$	Arc melting	HCl, citric acid, $(NH_4)_2SO_4$	Passive: 2–10 days RT	45–120	Relative density: 30%
			H_2SO_4	Active: 14 h ($0.11V_{MSE}$) RT	16 ± 4	Hardness: 128 ± 37 MPa (120-nm ligaments)
Cu-Zn[86,87]	$Cu_{50}Zn_{50}$, $Cu_{40}Zn_{60}$, $Cu_{30}Zn_{70}$, $Cu_{20}Zn_{80}$	Furnace melting; electrodeposition; sputtering	$HCl+NH_4Cl$ NaOH and HCl	Passive: 15–48 h, 70°C Passive: 24 h (with e-less plating)	120 ± 30 150 ± 30	Relative density: 40% Hardness: 24–90 MPa
Cu-Al[88,89]	$Cu_{33}Al_{67}$, $Cu_{35}Al_{65}$, $Cu_{40}Al_{60}$, $Cu_{50}Al_{50}$	Melt spinning	HCl+ NaOH	Passive: 2–4 h, RT—90°C	100–300	Yield strength: 80 MPa
Cu-Mg[90]	$Cu_{33}Mg_{67}$, $Cu_{40}Mg_{60}$, $Cu_{50}Mg_{50}$, $Cu_{60}Mg_{40}$, $Cu_{67}Mg_{33}$	Melt spinning	5% HCl	Passive 0.5 h, 90°C	150 ± 35	NA
Mg-Cu-Y[15,82]	$Mg_{60}Cu_{30}Y_{10}$ $Mg_{50}Cu_{40}Y_{10}$	Melt spinning	H_2SO_4	Passive (1.5 h)	60–100 Pore size: 30–60	Relative density: 60%
Cu-Zr-Al[91]	$Cu_{30}Zr_{65}Al_5$ $Cu_{40}Zr_{55}Al_5$ $Cu_{50}Zr_{45}Al_5$ $Cu_{60}Zr_{35}Al_5$ $Cu_{70}Zr_{25}Al_5$ $Cu_{80}Zr_{15}Al_5$	Melt spinning	HF	Passive: 24 h at 0°C and RT	RT: 58 nm with pore size of 40 nm 0°C: 47 nm with pore size of 20 nm	180° bendability with 230 nm to 1–3 μm NP Cu thickness
Cu-Zr[91,92]	$Cu_{70}Zr_{30}$	Sputtering	HCl	Active: 10 min ($-0.2V_{SCE}$) RT	Pore size: 500 nm	NA
Cu-Si[5,93,94]	$Cu_{41}Si_{59}$	Sputtering	HF	Active: 3–5 min ($-0.3V_{SCE}$) RT	30–45 nm	Relative density: 55–60%; Hardness: 0.3–1.3 GPa
Cu-Ti[13]	$Cu_{40}Ti_{60}$ $Cu_{50}Ti_{50}$ $Cu_{60}Ti_{40}$	Arc Melting	HF (0.03 M; 0.13 M)	Passive: 10.8 ks RT, 50°C, 75°C	46–79 nm (0.03 M HF) 80–338 nm (0.13 M HF)	Grain size: 14–25 nm

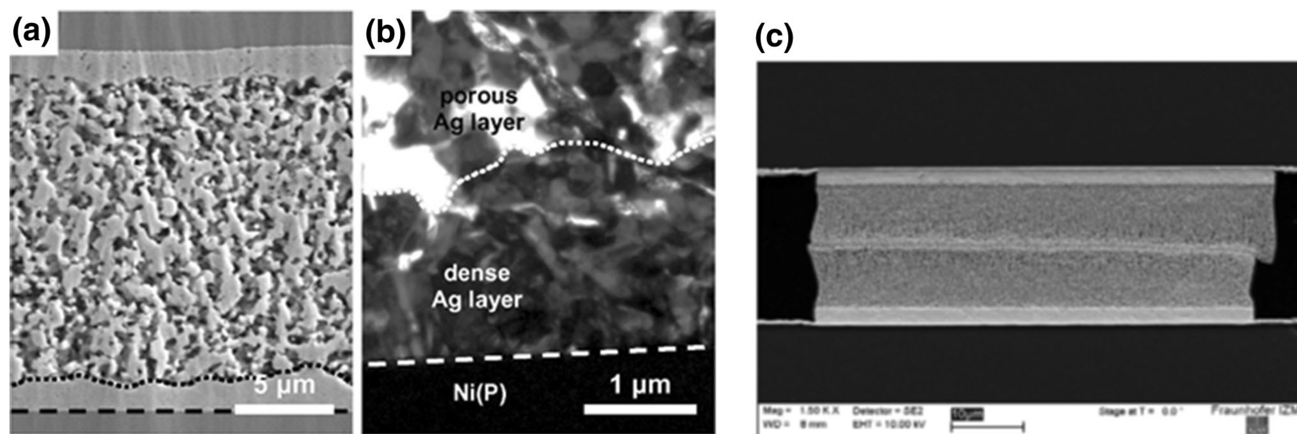

Fig. 8. Examples of sintered NP metals from the literature: (a) SEM backscatter and (b) transmission electron microscopy (TEM) cross-section image of NP Ag joint. The dotted lines show regions where the Ag has densified. (c) NP Au–NP Au joint sintered at 200°C and pressure of 10 MPa. Images (a) and (b) reproduced with permission from Ref. 101. Image (c) reproduced with permission from Ref. 102.

and duration. In our prior work, we reported assembly demonstrations of NP copper from sputtered Cu-Si that resulted in relative densities $> 85\%$ after sintering at 200°C.[24]

A process that is more in line with current interconnected device fabrication protocols is electrodeposition. Coelectrodeposition of Cu-Zn films has been a subject of considerable interest owing to their high corrosion resistance, applications in decorative and protective coatings, and production of shape-memory alloys.[104] For codeposition of alloy films, it is imperative that simultaneous reduction of the two or more constituent metal cations takes place at the cathode. There are systems where the standard reduction potentials are very different, for example, for Cu-Zn alloy, the potentials are + 0.34 V for Cu^{2+} and − 0.76 V for Zn^{2+}.[105] In such systems, codeposition can be achieved by incorporating additives into the electrolyte bath to help modify the deposition kinetics of the two cations. In the last decade or so, several studies proposing various alternatives to cyanide-based electrolytic baths have been reported. The proposed alternative complexing agents/bath chemistries include pyrophosphates,[4] polyligand pyrophosphates, where an auxiliary ligand is also added to pyrophosphate baths,[105] citrates,[106] sorbitol,[107] ethylenediamine tetraacetic acid (EDTA),[108] D-mannitol,[109] and ionic liquid baths.[110] An example of our more recent work is shown in Fig. 10, where Cu-Zn alloy was electrodeposited onto a mask placed on a silicon wafer with a copper seed layer. Figure 10a, b, c, and d shows before and after optical images of the patterned region, revealing excellent preservation of overall features despite some lateral shrinkage after dealloying (Fig. 10c and d). The through-thickness SEM image in Fig. 10e shows NP copper with some remnant Cu-Zn on top of the plated copper.

CHALLENGES AND PROMISE

There has been tremendous progress in understanding how to synthesize NP metals with desired ligament dimensions using different types of electrolytes and environments. The compatibility of NP copper synthesis with existing semiconductor fabrication protocols and the ability to achieve materials with $> 90\%$ densification after low-temperature sintering is highlighted.

At the same time, several challenges remain to be overcome. Some of those include the shrinkage that can occur after dealloying that, if left uncontrolled, may result in crack formation or delamination. Figure 11a shows some of the possible mechanisms to alleviate stress buildup due to substantial shrinkage. Figure 11b and c shows some possible NP copper films that can develop cracks if tensile stress buildup is not carefully controlled. However, it is possible to eliminate or reduce some of the stresses through careful development of residual compressive stresses (Fig. 11d and e). Other proposed solutions, such as gentle dealloying,[111] two-step dealloying,[112] introduction of compressive stresses,[96] or control over dealloying rate,[113] may also allow the sample to undergo the necessary dimensional changes and eliminate crack formation. There may also be possibilities to alleviate tensile stress buildup by patterning instead of employing blanket thin films. With NP metals, there are multiple routes to optimize the pore arrangement, ligament morphology, etc. to achieve desirable functionalities.

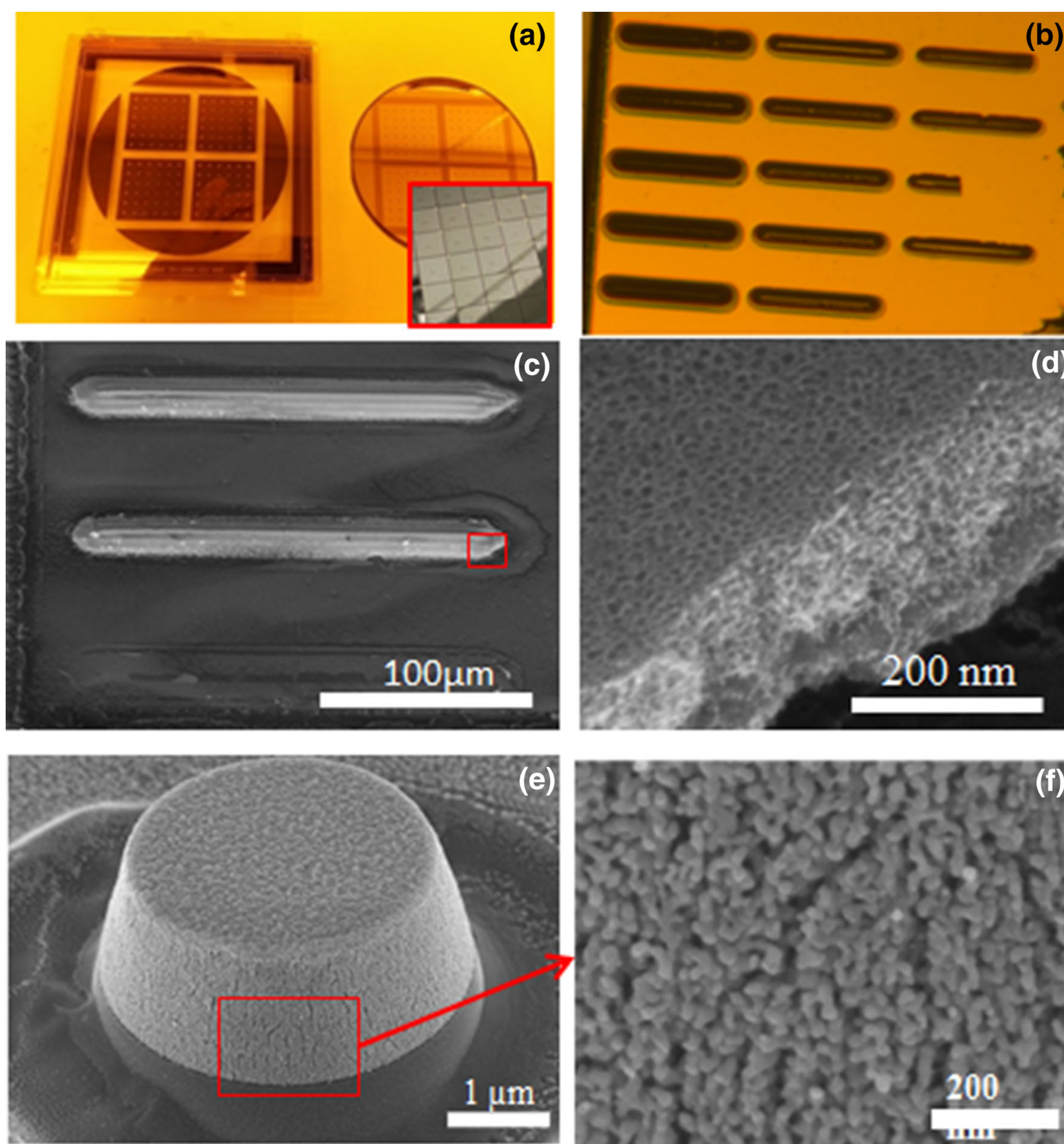

Fig. 9. Amorphous metal silicide films sputter-deposited through a mask on a 100-mm-diameter silicon wafer: (a) optical images of the wafer, with the insert showing smaller square scribed sections, (b) optical image of the amorphous metal silicide after mask removal, (c) SEM image of the features after etching of the amorphous silicide, (d) closeup top-view SEM image of the NP metal formed after etching the amorphous silicide. (e) Example of NP copper bump formed on a silicon substrate by focused ion beam. The precursor alloy was amorphous $Cu_{0.41}Si_{0.59}$ sputter deposited on silicon. The bump height is 2.2 μm with diameter of 3.9 μm. (f) Closeup near the base of the bump shows the NP copper morphology with ligaments of 20 nm in diameter.

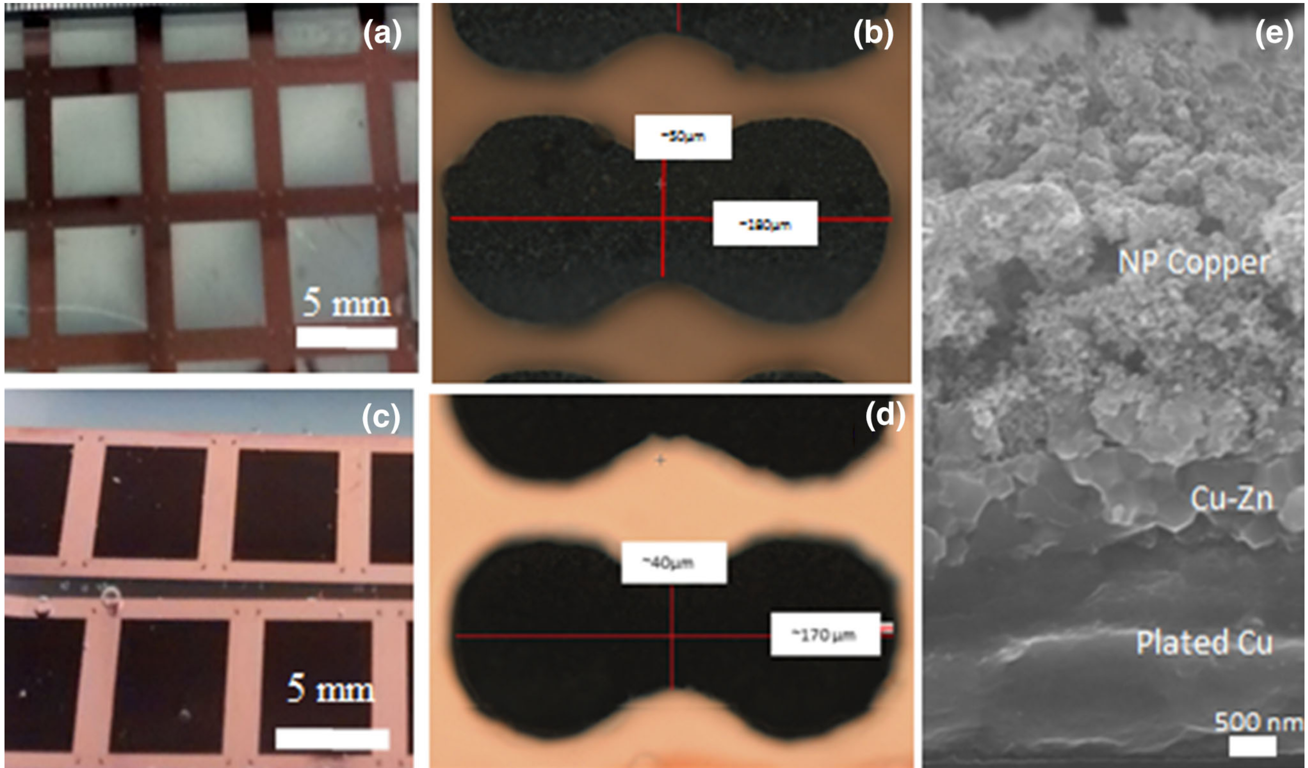

Fig. 10. Electrodeposited Cu-Zn alloy through a mask onto a silicon wafer with a copper seed layer (a) optical images of coupon after electrodeposition. (b) a close up optical view of one of the features with width of 180 μm and neck region of 50 μm (c) optical image of the pattern after dealloying to form NP Copper (d) closeup optical image after dealloying with slightly reduced feature sizes width of 170 μm and neck of 40 μm. (e) SEM image of the through thickness view showing NP Copper with some remnant Cu-Zn on top of the plated Copper.

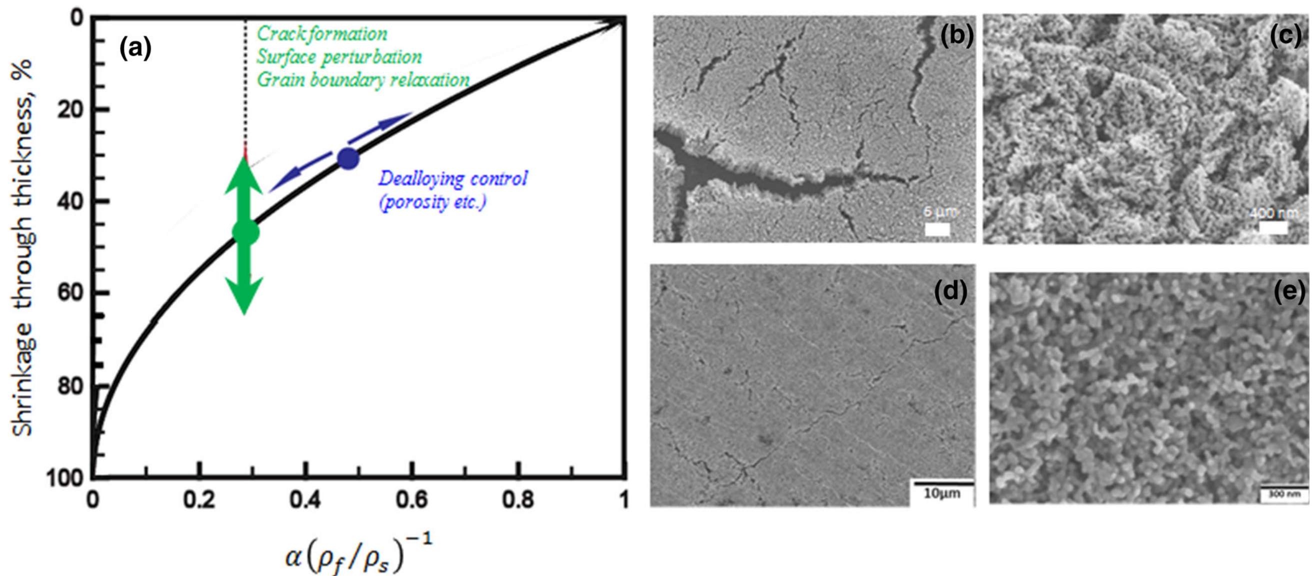

Fig. 11. (a) Dealloying can result in substantial through thickness shrinkage. Such dramatic changes in dimensions can be accommodated either enabling porosity evolution during dealloying. Otherwise, the material may relieve excessive stress buildup by grain boundary relaxation, surface perturbation or even crack formation. (b) Examples of NP Copper blanket films with little control of crack formation. A closeup of a region (c) highlighting NP Copper morphology. (d) Some control over the dealloying process can result in diminished cracks in NP Copper and the resulting closeup shows (e) a more intricate NP Copper morphology.

ACKNOWLEDGEMENTS

Part of this work is funded by the Semiconductor Research Corporation (SRC, Task # 2661) and by the National Science Foundation through Grant Nos. CMMI-1301268 and CMMI-1351705. We are grateful to our SRC liaisons from Texas Instruments, Sadia Khan and Luu Nguyen. Cu-Si alloy deposition was performed at the Center for Integrated Nanotechnologies, an Office of Science User Facility operated for the US Department of Energy (DOE) Office of Science by Los Alamos National Laboratory (Contract DE-AC52-06NA25396).

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