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Bulk GaN Ion Cleaving

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Bulk or freestanding GaN is a key material in various devices other than the blue laser diodes. However, the high cost of bulk GaN wafers severely limits the large scale exploitation of these potential technologies. In this paper, we discuss some engineering issues involved in the application of the ion-cut process to split a thin layer from 2-inch freestanding GaN. This process combines the implantation of light ions and wafer bonding and can possibly be used to reduce the cost of the fabrication of GaN-based devices by allowing the transfer of several bulk quality thin layers from the same donor wafer. To achieve this multi-layer transfer several conditions must be fulfilled. Here issues related to bulk GaN surface irregularities and wafer bowing are discussed. We also describe a method to circumvent most of these problems and achieve high quality bonding.

Key words: Bulk GaN, ion-cut, thin layer transfer, ion implantation, wafer bonding, bow, interfacial stress

INTRODUCTION

Bulk or freestanding (fs) GaN is mostly used in the fabrication of blue laser diodes, providing a wide spectrum of applications in optoelectronic data storage, visual information, medical devices, and biophotonics. Several industries [e.g., power devices, ultra-high brightness light emitting diodes (LEDs), etc.] can also benefit from the availability of fs-GaN.[1] High quality GaN bulk substrates can be produced by the hydride vapor phase epitaxy growth of thick GaN layers on sapphire and subsequent separation from the sapphire substrate.[2] The current cost of these fs-GaN wafers is very high. Therefore, large scale production of these new devices would require an important decline in fs-GaN price to compete with the alternative technologies (e.g., SiC). One of the possible strategies to reduce the cost would be to cleave several thin layers from a single fs-GaN wafer (donor wafer) and transfer them onto different handle wafers. In principle, this can be achieved by the use of the ion-cut process, commercially known as Smart-Cut™.[3–5] The different steps of this process are illustrated in Fig. 1. First, light energetic ions (hydrogen and/or helium) are implanted into a fs-GaN donor wafer at the optimal fluence. After implantation, the implanted wafer is bonded to a handle wafer. During annealing at intermediate temperatures (~500°C), the interaction of the implanted species with the produced radiation damage acts as an atomic scalpel, creating extended internal surfaces.[5] This leads to the splitting of a thin layer with a thickness equivalent to the implantation depth. Therefore, it is possible to tune the thickness of the transferred layer by adjusting the energy of the implanted species.[6] However, layer splitting can only take place if the bonded interface between the donor and handle is sufficiently stable. Indeed, successful bonding of the wafers remains the most critical step and requires the fulfilling of a long list of conditions.[7] Several surface imperfections and flatness deviations of fs-GaN wafers can limit the bonding quality or even prevent the spontaneous bonding and, consequently, prevent the application of the ion-cut process. In this paper we describe the progress in overcoming some of the problems faced in the bonding under ion-cut conditions of 2-inch fs-GaN.

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EXPERIMENT DETAILS

Our experiments were carried out using LED quality ~300 μm-thick 2-inch double side polished undoped fs-GaN wafers. The wafers were subjected

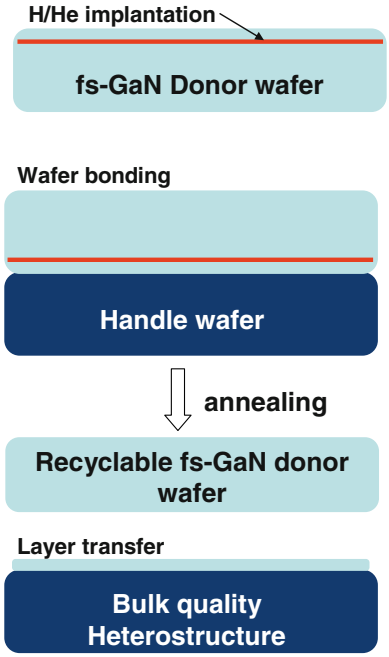

Fig. 1. Schematic illustration of the different steps in the thin layer transfer using the ion-cut process.

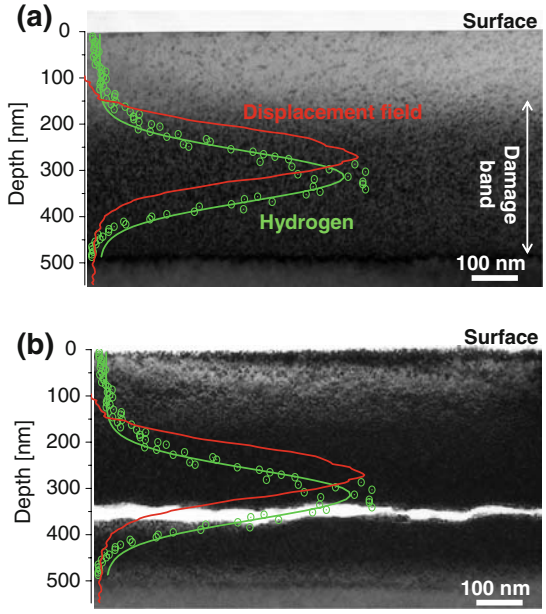

Fig. 2. (a) XTEM image of 50 keV H-implanted fs-GaN at a fluence of 2.6×10^{17} cm^{-2}. (b) XTEM image of H-implanted fs-GaN after annealing at 600°C for 5 min. The measured implantation-induced atomic displacements and H concentration depth profiles are superposed. Note that the subsurface microcracking takes place close to the H concentration peak.

to room temperature implantation with hydrogen (H) ions at 50 keV. During ion implantation, the wafers were tilted by ~7° relative to the incident ion beam to minimize ion channeling. The ion-cut optimal implantation fluence for the H:GaN system is found to be $\sim 2.6 \times 10^{17}$ atoms/cm^2, which is much larger than the fluence needed for other semiconductor materials.[8] Another peculiarity of GaN is that the optimal fluence does not change when He ions (or He + H) are implanted instead of H. Microstructural details of H ion-induced damage were obtained by cross-sectional transmission electron microscopy (XTEM). The XTEM analyses were carried out with a Philips CM 20T machine operated at 200 kV. In order to assess the lattice disorder in the implanted wafers, we carried out high-resolution x-ray diffraction, using a Philips X'Pert materials research diffractometer (MRD) system with Cu K_α radiation. Rutherford backscattering in channeling mode (RBS/C) was used to characterize the implantation-related displacements and lattice distortion in the implanted samples. RBS/C measurements along the [0001] axis of GaN were performed with a 2 MeV $^+$He beam.[5] Using the same setup, with different detection geometry, we measured the H depth profile by elastic recoil detection (ERD). The bow of the wafers was measured with a long range DEKTAK 8 stylus profilometer with a horizontal resolution of 3 μm. Atomic force microscopy (AFM) was employed to probe the surface morphology. In this work, sapphire was chosen as a handle material because its thermal expansion coefficient is relatively close to that of GaN compared with that of other materials such as Si and SiC. However, as demonstrated in our experiment, thermal stress is still an issue in high temperature processing of GaN/sapphire bonded pairs. The bonded interfaces were inspected by infrared (IR) imaging.

RESULTS AND DISCUSSION

H ion implantation produces a complex microstructure in GaN with a variety of radiation damage-related defects, including interstitials, vacancies, hydrogen-point defect complexes, voids, and free hydrogen.[9] Figure 2 displays a XTEM image of the as-implanted fs-GaN wafer. We note that the 50 keV H ion implantation produced a broad damage band extending over ~500 nm-thick layer below the surface. ERD analysis shows that the H-implantation depth is ~450 nm, with a concentration peak of ~13% around 320 nm, and the corresponding atomic displacement distribution reaches a maximum of ~27% at a shallower depth of ~285 nm (Fig. 2a).[5] After implantation, some of the fs-GaN wafers were cut into small pieces and annealed under different conditions to optimize the ion-cut annealing parameters. We found that annealing up to 450°C did not lead to any significant change in the morphology of the damage band. Above this temperature, however, nanoscopic cracks form around the concentration peak of H. Large cracks and extended internal surfaces appear only after annealing at a temperature higher than 500°C for durations longer than 5 min (Fig. 2b). A detailed study of the kinetics of this process can be found in Ref. 10.

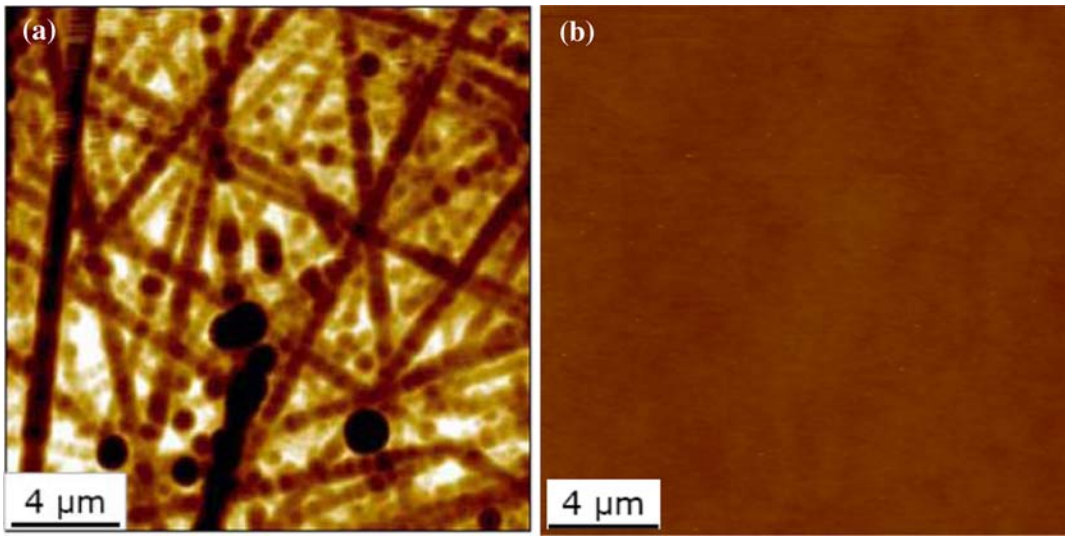

Fig. 3. (a) AFM image of the Ga face of fs-GaN wafer (RMS roughness ~21 nm). (b) AFM image of CMP-prepared 100 nm SiO_2 layer deposited on fs-GaN (RMS roughness ~0.18 nm).

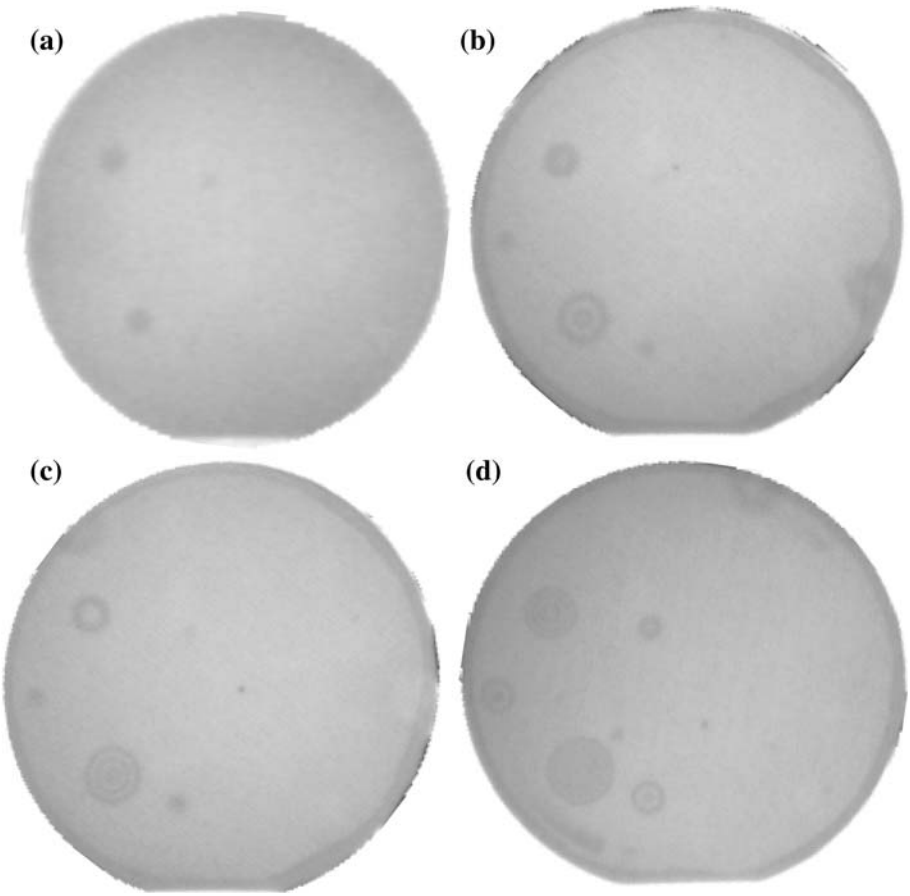

Fig. 4. IR images of the bonded SiO_2/sapphire interface. (a) Immediately after bonding at room temperature; (b) after annealing at 200°C for 24 h; (c) after annealing at 700°C for 2 h; (d) after annealing at 1050°C for 2 h.

Surface roughness and waviness are critical factors in determining the quality of wafer bonding. In fact, spontaneous bonding can only be achieved for mirror-polished surfaces with a root mean square (RMS) roughness on the order of 0.5 nm or less and in the absence of any micron-scale irregu-

larities. Our AFM analysis showed that the fs-GaN wafers have a RMS roughness in the range of 15 nm–50 nm/20 × 20 μm^2 far above the required flatness. Figure 3a displays an AFM image of the Ga face of a fs-GaN wafer. This figure indicates clearly that the GaN surface has important imperfections which will affect the contact at the interface, with harmful consequences for the bonding. Recently, Hayashi and co-workers developed a chemical mechanical polishing (CMP) process by which the RMS roughness of a GaN surface can be reduced to below 0.5 nm.[11] This process can be used for the direct bonding of GaN wafers, which would require annealing at a very high temperature (>1000°C) in order to strengthen the bonded interface.[12] In our case this direct bonding cannot be used, as the splitting takes place at temperatures as low as 500°C. Therefore, low temperature processing is required. To circumvent this difficulty, we deposited an SiO_2 cap layer on the fs-GaN wafers. In addition to the fact that the SiO_2 layer can be easily polished, leading to smooth surfaces, the SiO_2/sapphire interface exhibits high bonding energy following annealing below 200°C.[13] This makes a SiO_2 interlayer suitable for the ion-cut process. A 100 nm-thick SiO_2 layer was deposited on fs-GaN by plasma-enhanced chemical vapor deposition (PECVD). To prevent undesired outgassing from the PECVD oxide layer during subsequent heat treatments of the bonded wafer pairs, we annealed the fs-GaN wafers at 850°C in a N_2 atmosphere after deposition of the SiO_2 layer. Oxide-deposited wafers were subsequently mirror-polished by CMP using syton solution. The surface RMS roughness was on the order of 0.2 nm/20 × 20 μm^2 after CMP (Fig. 3b), ensuring the short range flatness required for wafer bonding.[7] The polished fs-GaN wafers with the SiO_2 layer and sapphire wafers (handle wafers) were cleaned for 15 min in a piranha solution (H_2O_2:H_2SO_4 = 1:3), followed by a de-ionized water rinse, and dried with an N_2 gun. After these cleaning steps the surfaces were terminated with hydroxyl (OH–) groups necessary to initiate the bonding. For successful thin layer splitting, the bonded interface must be sufficiently strong to sustain annealing at 500°C used in ion-cut experiments. Additionally, the interface should also remain stable at temperatures as high as 1050°C, which are used in the growth of GaN-based devices. Figure 4 confirms the thermal stability of the SiO_2/sapphire interface. Indeed, apart from a few cavities, the wafers remain bonded after annealing at 1050°C for 2 h.

Based on the analysis above, the parameters for the surface preparation leading to high quality bonding were determined. However, there is still another critical factor that needs to be solved in order to bond fs-GaN: the wafer bow. In general, the commercially available 2-inch fs-GaN wafers already exhibit an important bow, as shown in Fig. 5a. This figure displays a two-dimensional (2D) profile map of

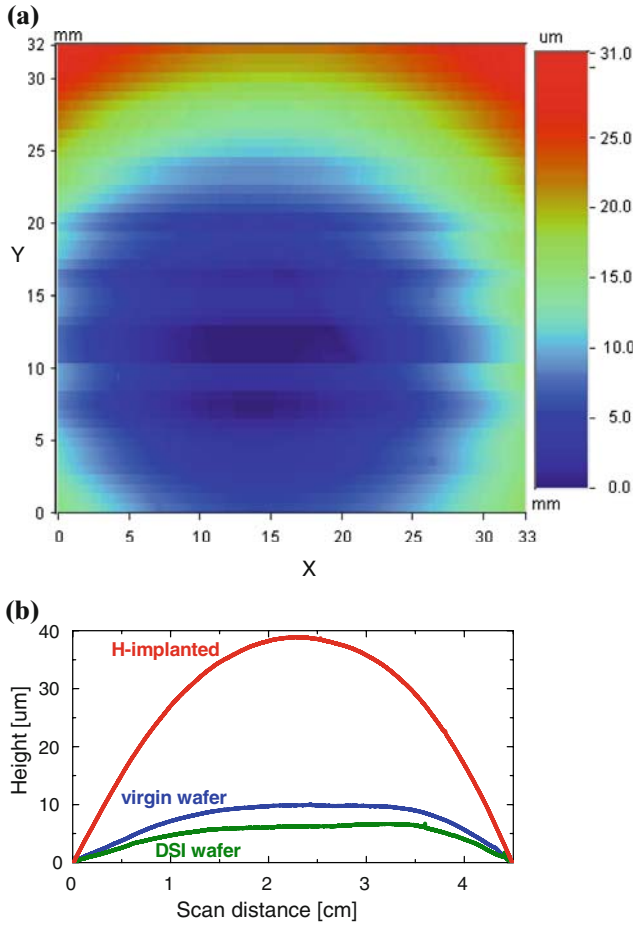

Fig. 5. (a) A 3.3 cm × 3.2 cm 2D profile map of a 2-inch fs-GaN wafer (Ga face). (b) Bow measurements on a 2-inch fs-GaN wafer before implantation (virgin), after H implantation, and after double-sided implantation (DSI).

a virgin 2-inch fs-GaN wafer measured at the Ga face. This bow becomes even larger after H implantation, as can be seen in Fig. 5b, which shows the bow as measured on the N face for a different virgin wafer. Prior to ion implantation, the wafer bow was ~10 μm and reached ~40 μm after implantation. This bowing of H-implanted fs-GaN wafers can strongly limit, or even prohibit, the bonding and, consequently, the application of the ion-cut process to transfer thin layers of high quality fs-GaN onto other host materials. The tolerable bows depend sensitively on the material properties and wafer thickness. Unfortunately, the observed post-implantation bowing is too high to allow any contact of the wafers to be paired and bonded. Indeed, our bonding experiments on as-implanted wafers showed that the gap between the two surfaces was too large to permit van der Waals forces to come into play to initiate the bonding process. It is also worth mentioning that our bonding tests under compressive forces (e.g., a load in the bonding machine) have led to a systematic breakage and cracking of the wafers to be bonded and, therefore, cannot be considered to be a reliable solution to the bowing problem.[14]

The origin of the post-implantation bowing of fs-GaN resides in the stress generated by the implantation damage. Typical x-ray diffraction data of fs-GaN before and after H implantation are presented in Fig. 6. We notice that H implantation created a significant out-of-plane tensile strain, which was detectable as a broadening at the left side of the (0002) GaN diffraction peak. Close examination of the spectrum shows that the as-implanted diffraction spectrum consists of two different features shifted by approximately 0.015° and ~0.14° from the (0002) diffraction peak. These two features revealed that the implantation damage induces two distinct strained regions. The highly strained region is characterized by a relatively broad peak. We attribute this peak to a highly defective zone. Such a defective zone can be seen in Fig. 2a, which shows a XTEM micrograph of the as-implanted sample. As a consequence of this out-of plane stress, the wafer bends upwards at the implanted face, which leads to the observed enhancement of the bow.

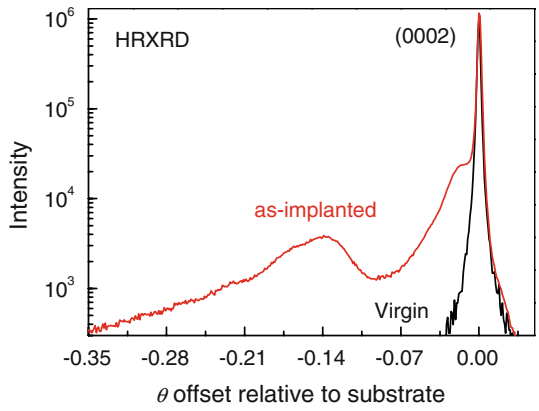

Fig. 6. High resolution x-ray diffraction (HRXRD) spectra of (0002) GaN before and after H implantation with a fluence of 2.6×10^{17} cm^{-2} at an ion energy of 50 keV.

As addressed above, the strain at or below the surface strongly influences the wafer bow. Similarly, a strained layer at the back side (Ga face) of the H-implanted fs-GaN wafer (implanted at the N face) can enhance the bow at the Ga face of the wafer, thereby compensating for the bow enhancement at the N face of the wafer. The final value of the bow depends directly on the amount of strain induced at the Ga face. The finite element calculations shown in Fig. 7 demonstrate that the bow can be effectively reduced by ~87% when the strain is locally manipulated at the back side of the implanted 2-inch fs-GaN wafers. However, this remains a simple theoretical approach, which can be hardly realized experimentally. Recently, we demonstrated that double-sided implantation (under the same conditions) is an effective approach to obtain relatively flat H-implanted fs-GaN wafers.[4] Moreover, we found that the final bow can be reduced

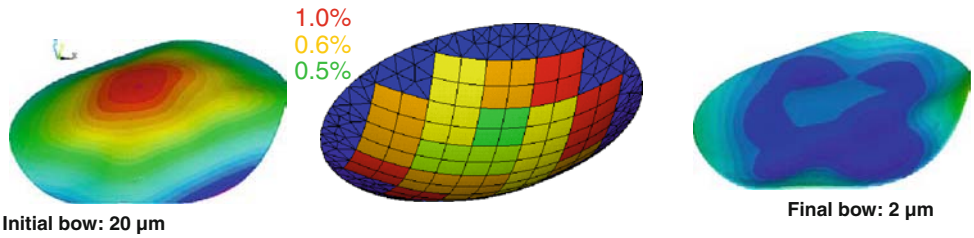

Fig. 7. Finite element modeling of bow reduction by wafer back side stress manipulation (Ref. 14).

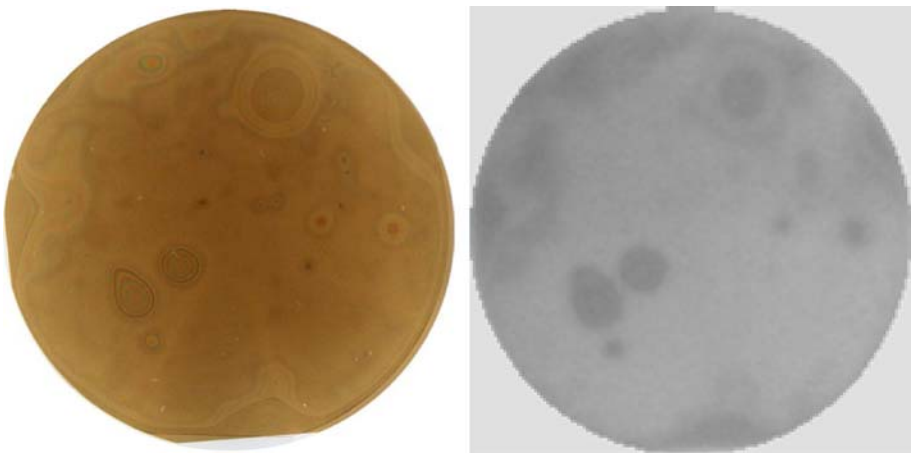

Fig. 8. Optical (*left*) and IR (*right*) micrographs of H-implanted fs-GaN bonded to a 2-inch sapphire wafer. Note that, due to radiation damage, the fs-GaN wafer exhibits a change in color from transparent to golden-brown after hydrogen implantation.

below its initial value by a slightly deeper implantation at the back side of the wafer (Fig. 5b). Indeed, as shown in Fig. 5b, a final bow of ~6 μm was obtained after a second implantation at the back side of H-implanted fs-GaN wafers. In the second implantation, H ions were implanted ~50 nm deeper but at the same fluence of 2.6×10^{17} cm^{-2}. Based on this approach, successful bonding of H-implanted 2-inch fs-GaN onto sapphire was achieved (Fig. 8).[4]

Since the main motivation behind the use of the ion-cut process is to reduce the cost of bulk quality GaN layers, the second implantation needed to adjust the bow is an additional step which can increase the cost of the ion-cut process. Here, we believe that it could be possible to take advantage of the second implantation. Indeed, the Ga face is also implanted at the optimal fluence; therefore, the bonding of both sides of the fs-GaN wafers to two handle wafers can lead to a simultaneous transfer of two thin GaN layers by ion-cutting (Fig. 9). Work is underway to optimize and realize this process of double-sided splitting.

The method described above of wafer bow manipulation by stress adjustment at the back side of the implanted fs-GaN led to fairly flat H-implanted 2-inch GaN wafers, making possible the bonding to handle wafers. In spite of this achievement, complete transfer of a 2-inch thin layer was not yet demonstrated. One of the major problems faced was the partial or total debonding of the fs-GaN/sapphire pairs upon annealing at temperatures above 300°C. Figure 10 displays the optical images of an fs-GaN/sapphire pair immediately after room temperature bonding and after annealing at 325°C. We note that, upon annealing, a significant area at the interface was debonded and became larger when we increased the annealing temperature. This reduced the transferred area to millimeter-scale regions in the best cases. Layer transfer was achieved by a slow increase of temperature (~1 °C/min) up to 500°C to anneal the partially bonded wafers or pieces for ~30 min. We attribute this observation to the thermally induced interfacial stress, which can be reduced by performing the bonding at a relatively high

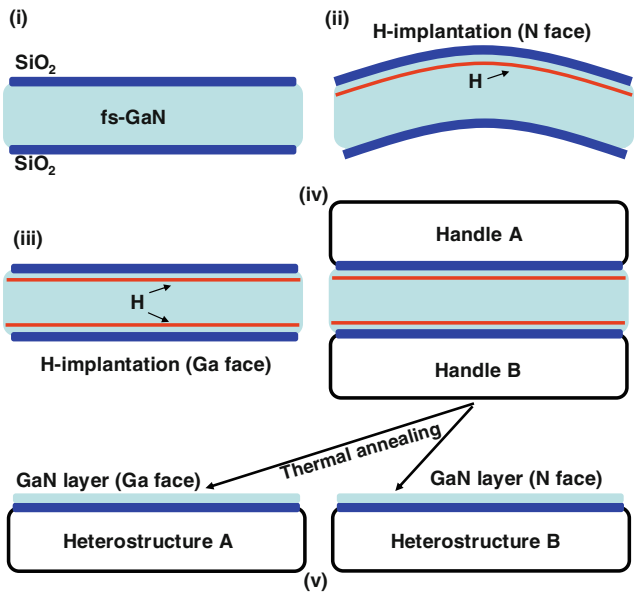

Fig. 9. Schematic illustration of the double-sided bonding and splitting processes. (i) Deposition and polishing of the oxide on both sides of the wafer; (ii) N face H-implantation; (iii) Ga face H-implantation and wafer bow reduction; (iv) direct bonding to two handle wafers; (v) thermal annealing and simultaneous transfer of two thin films from the fs-GaN wafer. Two different handle wafers can be used, leading to different heterostructures in a one step process.

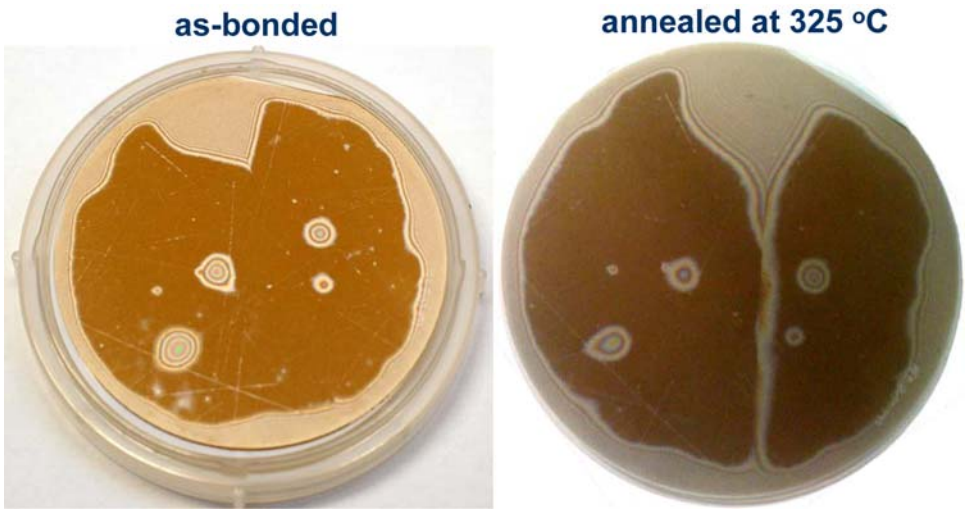

Fig. 10. Optical images of a 2-inch fs-GaN/sapphire pair immediately after room temperature bonding (*left*) and after annealing at 325°C (*right*). The images were taken at the sapphire side of the bonded pair.

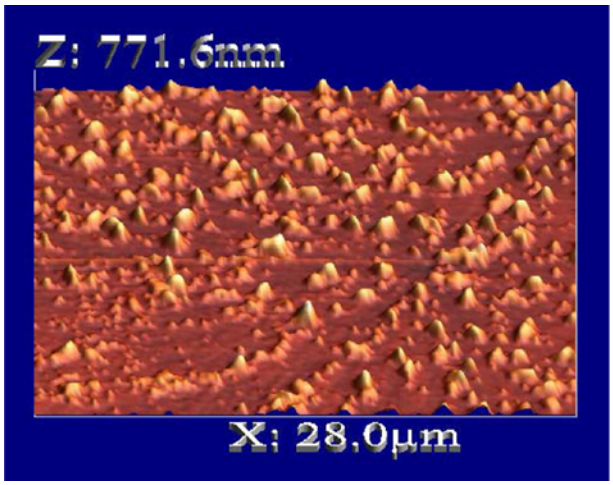

Fig. 11. AFM image of the surface of a transferred fs-GaN thin layer onto sapphire.

temperature (see, for e.g., Ref. 7, pp. 210, 211). Indeed, high temperature bonding was found to be effective in the high thermal mismatches, such as Si bonded to quartz. In this way, the difference between the bonding and annealing temperatures can be reduced, and, consequently, the interfacial shear and peeling stress can be minimized. Finally, the analysis of the morphology of transferred areas showed a very rough surface with a RMS roughness on the order of 50 nm (Fig. 11). Therefore, the use of the transferred thin layers in device fabrication would require a polishing step to prepare the surface for epitaxy.

CONCLUSIONS

The major technical issues faced in the application of the ion-cut process to transfer bulk quality GaN thin layers were reviewed in this paper. The commercially available fs-GaN 2-inch wafers are very rough, with short and long range irregularities. The deposition of thin SiO_2 layers on GaN wafers leads to smooth surfaces suitable for wafer bonding with a stable SiO_2/sapphire interface, allowing low temperature processing. We also showed that the bow enhancement after H ion implantation can be dealt with by stress engineering at the back side of the implanted wafers. This method leads to fairly flat H-implanted GaN wafers. A successful bonding of H-implanted 2-inch fs-GaN onto sapphire was demonstrated. However, a complete transfer of 2-inch layer was not yet achieved, and the transferred regions remained at the millimeter scale. We attributed this limitation in the process to the thermally induced interfacial stress, which led to partial or even total debonding of the bonded pairs. Work is in progress to control the bonding process and reduce the problem of thermal stress by performing the wafer bonding at relatively high temperature.

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