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Spatial Localization of Carrier Traps in 4H-SiC MOSFET Devices Using Thermally Stimulated Current

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Carrier traps in 4H-SiC metal–oxide–semiconductor (MOS) capacitor and transistor devices were studied using the thermally stimulated current (TSC) method. TSC spectra from *p*-type MOS capacitors and *n*-channel MOS field-effect transistors (MOSFETs) indicated the presence of oxide traps with peak emission around 55 K. An additional peak near 80 K was observed due to acceptor activation and hole traps near the interface. The physical location of the traps in the devices was deduced using a localized electric field approach. The density of hole traps contributing to the 80-K peak was separated from the acceptor trap density using a gamma-ray irradiation method. As a result, hole trap density of $N_{t,hole} = 2.08 \times 10^{15}$ cm^{-3} at 2 MV/cm gate field and $N_{t,hole} = 2.5 \times 10^{16}$ cm^{-3} at 4.5 MV/cm gate field was extracted from the 80-K TSC spectra. Measurements of the source-body n^+–p junction suggested the presence of implantation damage in the space-charge region, as well as defect states near the n^+ SiC substrate.

Key words: Thermally stimulated current, hole traps, 4H-SiC MOSCAP, 4H-SiC MOSFET, threshold voltage, implantation damage, acceptor activation

INTRODUCTION

Techniques for defect analysis based on the measurement of luminescence or electrical current due to thermal generation of electron–hole pairs during ionization are well known to the semiconductor research community. Nicholas and Woods characterized electron traps in CdS by measuring its luminescence as a function of temperature.[1] Buehler and Phillips measured the thermally stimulated current (TSC) spectra of intentionally introduced Au acceptors in the base region of bipolar devices in their studies of lifetime suppression in transistor–transistor logic (TTL) circuits.[2] Extensive work has been performed by Fleetwood et al. on nitrided oxides[3] and irradiated MOS devices.[4,5] The experimental results from their work advanced the theoretical understanding of thermally activated processes.[6–9]

A contributing factor to the low field-effect mobility of SiC metal–oxide–semiconductor field-effect transistors (MOSFET) has been suggested to be traps near the SiC/SiO_2 interface. However, the physical nature or location of these interface traps is still under investigation in the SiC community. Energetically spread throughout the bandgap of the material, carrier traps behave as additional acceptors near the conduction band or donors near the valence band. When located near the SiO_2/SiC interface, their influence on the transport properties of the device can be detrimental.[10]

Previous reports of TSC measurements on SiC have focused on metal–oxide–semiconductor (MOS) capacitors fabricated on *n*- and *p*-type 4H- and 6H-epitaxial layers.[11–14] Studies of *p*-type 6H-SiC MOS capacitors by Lysenko et al.[11] and Ólafsson et al.[12] showed two main peaks in the TSC spectra, located

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at approximately 50 K and 70 K. The origin of the former peak was attributed to interface states, whereas the latter was concluded to be due to Al acceptors (E_A = 160 meV to 230 meV).[15–17] On *n*-type 4H-SiC, Rudenko et al. observed TSC peaks near 40 K, 90 K, and 150 K.[13,14] The 40-K peak was attributed to N donor ionization, and the other two peaks were due to the presence of interface states near the conduction band. In addition, Fang et al. have performed TSC characterization of 4H-SiC substrates, identifying Al, B, and V defect levels at 0.22 eV, 0.28 eV, and 0.91 eV, respectively.[18]

To the authors' knowledge, TSC experiments on MOS transistors have not been previously reported in the literature. Here, we characterize the TSC spectra of MOS capacitors and then present a method for separation of the observed traps. We do so by using transistor samples, where separate electric fields could be localized to the oxide and the bulk of the device. Furthermore, we present a method for separating the contribution of different emission mechanisms to peaks at the same temperature using gamma-ray irradiation. Both methods are described in the "Experimental Procedures" section.

EXPERIMENTAL PROCEDURES

In this work, we used 5-μm-thick epitaxial *p*-type (Al-doped, $N_A = 1 \times 10^{16}$ cm^{-3}) 4H-SiC MOS capacitor (MOSCAP) and *p*-channel lateral DMOSFET (LDMOSFET) samples with circular metal contacts, provided by Cree, Inc. The thickness of the thermally grown SiO_2 was 500 Å, NO-annealed using standard post-oxidation techniques. Details about device fabrication can be found elsewhere in the literature.[19]

Specifying the temperature for entering the carrier freeze-out regime is essential for interpreting TSC spectra. In this work, we did this by observing the decrease of the accumulation capacitance at cryogenic temperatures. The capacitance–voltage (*C–V*) measurements were performed using a Keithley 590 capacitance meter. Figure 1 shows the temperature-dependent *C–V* behavior of a 4H-SiC MOS capacitor swept at 100 kHz from accumulation to depletion. At temperatures lower than 160 K, the device entered the freeze-out regime, and the hole accumulation layer density was very low. For comparison, shallow N donors with an activation energy of around 50 meV in *n*-type SiC samples ionized at around 50 K.[13]

A similar *C–V* measurement was performed on a capacitor-connected MOS transistor with source, drain, and body connected together. The resulting curves are shown in Fig. 2. The accumulation layer behavior is identical to that observed in Fig. 1. However, due to the presence of a source and drain in the device, an inversion layer was maintained at all temperatures, including below the lowest temperature shown in Fig. 2, down to 16 K.

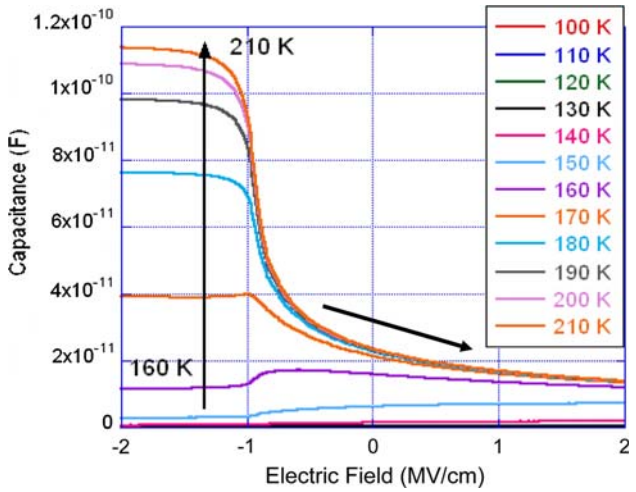

Fig. 1. High-frequency (100-kHz) *C–V* characteristics of an epitaxial *p*-type 4H-SiC MOS capacitor as a function of temperature.

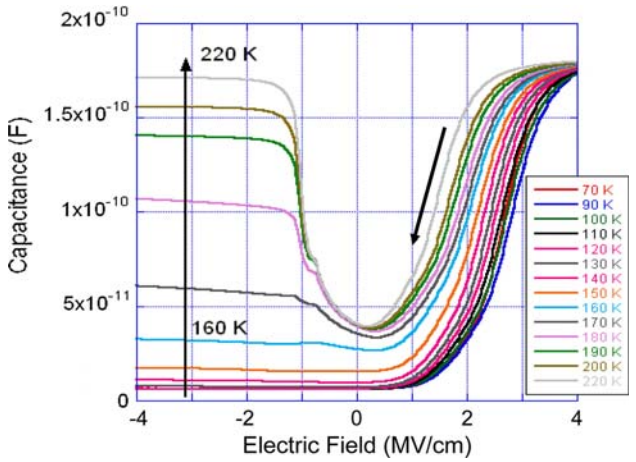

Fig. 2. High-frequency (100-kHz) *C–V–T* characteristics of the *n*-channel 4H-SiC MOSFET device. Source, drain, and body of the FET were connected together.

The samples were mounted on an insulating AlN pad, wire-bonded to a chip carrier, and placed in a flow-through Janus dewar. The TSC spectra were measured using Keithley 617 and 6517 electrometers. No curve-smoothing algorithms have been applied to the TSC spectra reported in this work. Each cycle of cooling and warming was completed in approximately 2 h, with custom software automating the tasks of a Lakeshore 91-C temperature controller and a liquid-He tank pressure control setup.

Samples were cooled down to 250 K, at which point a gate bias was applied, with either positive or negative polarity.[13] While maintaining the bias on the gate, the samples were cooled down to about 20 K, at which point the polarity of the gate bias was reversed and the heater inside the dewar was turned on. As the temperature increased back to 250 K, the current was recorded and any peaks observed were reported as TSC spectra.

Table I. Summary of device setup and TSC measurement conditions

Device	Figure	Details	Cooldown	Warmup
MOSCAP	3	Electrometer on gate	$E_{cooldown}$ = −2 MV/cm Accumulation	E_{warmup} = 1 MV/cm to 5 MV/cm Depletion
MOSCAP	4	Electrometer on gate	$E_{cooldown}$ = −2 MV/cm to −4.5 MV/cm Accumulation	E_{warmup} = 2 MV/cm Depletion
MOSFET	6	Electrometer on gate	$E_{cooldown}$ = −2 MV/cm Accumulation	E_{warmup} = 2 MV/cm to 5 MV/cm Inversion
MOSFET	7	Electrometer on back-side contact (body)	V_{body} = −10 V to −25 V $E_{cooldown}$ = −4 MV/cm Accumulation	V_{body} = −10 V to −25 V E_{warmup} = 2 MV/cm Inversion
MOSCAP	9a	Electrometer on gate; 100 krad γ-irradiation with 2 MV/cm gate field (depletion) prior to TSC	$E_{cooldown}$ = −1 MV/cm to −4 MV/cm Accumulation	E_{warmup} = 2 MV/cm Depletion
MOSCAP	9b	Electrometer on gate; 100 krad γ-irradiation with −2 MV/cm gate field (accumulation) prior to TSC	$E_{cooldown}$ = −1 MV/cm to −4 MV/cm Accumulation	E_{warmup} = 2 MV/cm Depletion
MOSFET	10	Gate and drain floating, electrometer on source-body junction	$V_{S/B}$ = 2.5 V Forward bias	$V_{S/B}$ = −20 V to −100 V Reverse bias

Table I summarizes the conditions under which the TSC measurements were performed. The magnitude and polarity of the gate field, approximated by $E = V_G/t_{OX}$, were varied during cooldown ($E_{cooldown}$) or warmup (E_{warmup}). As a result, the device would be in either accumulation or depletion/inversion during cooldown and the opposite condition during warmup. For the MOS transistors (source and drain tied together), additional variables were the body bias (V_{body}) and the source/body junction bias ($V_{S/B}$). The heating rate (β), though not specifically controlled, was consistent among all measurements. It was highest at cryogenic temperatures (0.19 K/s) and decreased as room temperature was approached (0.04 K/s at 160 K, the highest temperature at which a TSC peak was observed). This variation was taken into account when calculating trap densities.

RESULTS AND DISCUSSION

Spatial Separation of Carrier Traps (Localized Electric Field Method)

Two methods for TSC carrier trap characterization are presented in this work. The first method, described in this section, allowed us to obtain information about the physical location of traps in the device by comparing the TSC spectra of an MOS capacitor and an FET from the same die. We first measured the TSC spectra of an MOS capacitor, biased in accumulation during cooldown and depletion during warmup. Two peaks were observed, near 55 K and 80 K, as presented in Figs. 3 and 4. During the warmup cycle, the gate field terminated on the back-side metal contact due to the lack of an inversion layer at the SiO_2/SiC interface.

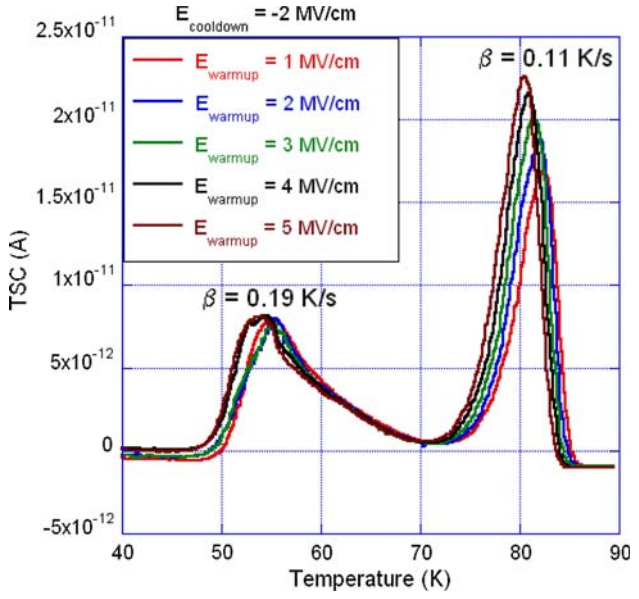

Fig. 3. TSC spectra of a *p*-type epitaxial 4H-SiC MOSCAP biased in accumulation during cooldown ($E_{cooldown}$ = −2 MV/cm) and depletion during warmup.

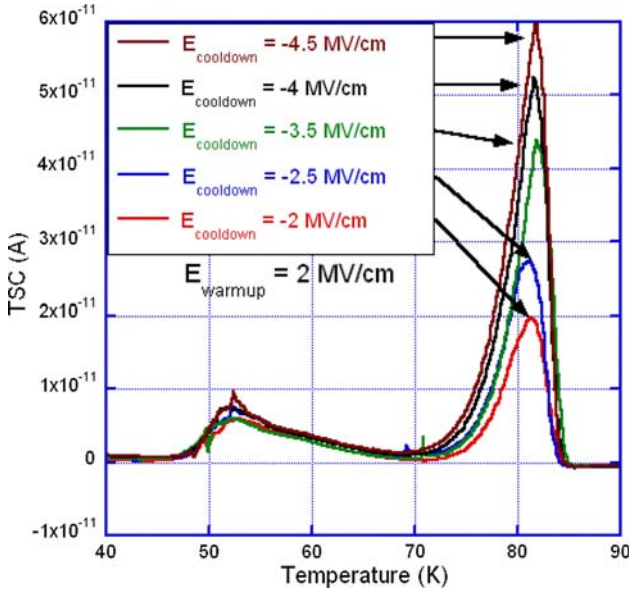

Fig. 4. TSC spectra of a *p*-type epitaxial 4H-SiC MOSCAP biased in accumulation during cooldown and depletion during warmup with a constant warmup field of E_{warmup} = 2 MV/cm.

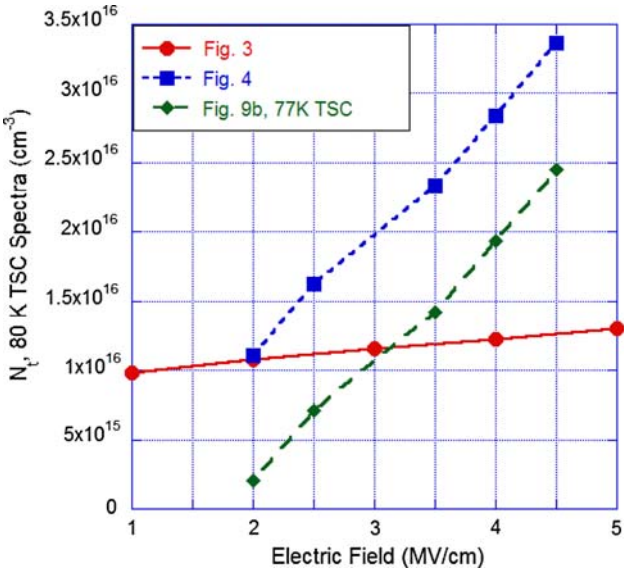

Fig. 5. N_t as a function of gate field for the 80-K TSC spectra from Figs. 3 and 4, as well as the 77-K TSC spectra in Fig. 9b.

As a result, TSC spectra obtained using this arrangement originate from traps located throughout the entire device.

Next, we measured an adjacent MOS transistor. Two electrometers were connected to the device, one to the gate and one to the back-side body contact, as shown in Fig. 6. First, we held the body bias steady and varied the gate bias. During warmup, the inversion layer of the MOSFET acted as a gate field termination layer, thus isolating the emission of any resulting TSC to the area between the gate metal and the bottom of the inversion electron sheet. Figure 6 shows that only the 55-K peak was measured by the gate electrometer in the temperature range covered. Peaks similar to those shown in Fig. 7 were registered near 80 K by the body electrometer. Therefore, the 55-K peaks originated from traps localized within the gate electric field terminating on the inversion layer, and the 80-K peaks obtained from the capacitor measurements should originate from the SiC bulk or epilayer. To verify this hypothesis, the MOSFET was measured again, this time with constant gate bias and variable body bias. Figure 7 verified that only the 80-K peaks were registered by the body electrometer, whereas the gate electrometer only registered peaks at 55 K (identical to Fig. 6, not shown for brevity).

The following sections provide further insight into this technique, as well as some additional artifacts that could influence the results.

TSC Spectra of MOS Capacitors

To verify the validity of the local electric field approach described above, we considered the configuration where the capacitor was biased in accumulation during cooldown and inversion during warmup. By using a capacitor instead of a transistor, the formation of a gate field terminating inversion layer was avoided when the gate bias was switched from accumulation to depletion at 20 K. During warmup, the hole accumulation layer remained frozen out, and the gate field terminated on the n^+ SiC substrate rather than the oxide/epi interface. The resulting TSC spectra, shown in Figs. 3 and 4, exhibited two peaks of positive current near 55 K and 80 K. Since there were virtually no electrons present in the SiC epilayer ($n_{i,4H\text{-}SiC,80K} = 4.95 \times 10^{-84}$ cm^{-3}),[20] the TSC must have been due to positive charge flowing away from the gate and into the substrate.

The density of traps, N_t, associated with the 55-K and 80-K peaks, was calculated by integrating the TSC spectra using Eq. 1,

$$N_t = \frac{1}{\beta A q}\int_{T_1}^{T_0} I(T)\mathrm{d}T, \qquad (1)$$

where A is the device area and q is the electron charge.[21]

For the 55-K peak in Fig. 3, $N_{t,55K} = 1.35 \times 10^{12}$ cm^{-2} at 4 MV/cm gate field, and similar values for the other fields. The trap density as a function of gate field for the 80-K peaks in Figs. 3 and 4 is presented in Fig. 5. The 5-MV/cm TSC peak in Fig. 3 (23 pA at 80.5 K) yielded a trap density of $N_{t,80K} = 1.3 \times 10^{16}$ cm^{-3} (3.25×10^{12} cm^{-2}).* Even

*When expressing $N_{t,80K}$ as a volume density, we used a value of 2.5 μm (half of the 5 μm SiC epilayer thickness) for the depletion width, since at cryogenic temperatures a depletion region did not exist. Using half the SiC epilayer thickness accounted for the average contribution to the measured current of carriers traversing the epitaxial region.

though this was very close to the *p*-type epilayer Al doping level of $N_A = 10^{16}$ cm^{-3}, it must be noted that only a small fraction of the Al acceptors were electrically active at 80 K.[22] Neither peak of the TSC spectra in Fig. 3 exhibited strong dependence on the depletion bias during warmup. One interesting observation was the shift of the 80-K peak temperatures (T_{max}) to lower values as the depletion bias increased. This shift is caused by the Poole–Frenkel effect, where the traps' energy level shifted towards the valence band as the gate field increased ($E - E_t \propto E_{gate}^{1/2}$).[23]

In Fig. 4, when the device was biased at different accumulation levels during cooldown, $N_{t,55K}$ remained almost constant (1.33×10^{12} cm^{-2}), whereas $N_{t,80K}$ depended strongly on the density of the accumulation layer. $N_{t,80K}$ at 4.5 MV/cm had increased to 3.36×10^{16} cm^{-3} (8.41×10^{12} cm^{-2}), which suggested an excess hole trap concentration of 5.6×10^{12} cm^{-2} near the SiO_2/SiC interface, where the hole accumulation layer was formed. The presence of hole traps near the valence band in bulk SiC has been previously observed by Danno et al., who reported minimal influence of these traps on the carrier lifetime.[24] Rozen et al. have attributed the higher density of hole traps in NO-annealed oxides to the increased nitrogen incorporation at sites near the interface.[25]

TSC Spectra of MOS Transistors

To determine the physical location of trap emission within the device, we performed a TSC measurement on an MOS transistor biased in accumulation during cooldown and inversion during warmup. To do so, we had to ensure that the applied gate bias was high enough to keep the device in inversion as the threshold voltage increased at cryogenic temperatures.

Several groups have previously explored the temperature dependence of the threshold voltage in 4H-SiC MOSFET devices at high temperatures.[26–28] Due to the dramatic decrease in effective carrier concentration in SiC over the measured temperature range, the sample exhibited V_{th} increase from about 0.73 V at room temperature to 7.4 V at 40 K, as extracted from the *x*-intercept of the I_D versus V_{GS} curve at $V_{DS} = 0.1$ V. This change in V_{th} indicated a net *negative* charge of 3×10^{12} cm^{-2} present in the oxide. The field-effect mobility (μ_{FE}) decreased from 26.9 cm^2/V s at room temperature to less than 5 cm^2/V s below 100 K, as previously reported in the literature.[29]

As shown in the inset of Fig. 6, the method of spatial separation of traps involved using two electrometers during TSC characterization. Traps located within the oxide were isolated by attaching the positive lead of the first electrometer to the MOSFET gate and the negative lead to the source, drain, and body terminals. As a result, the measured TSC in the gate electrometer was due to

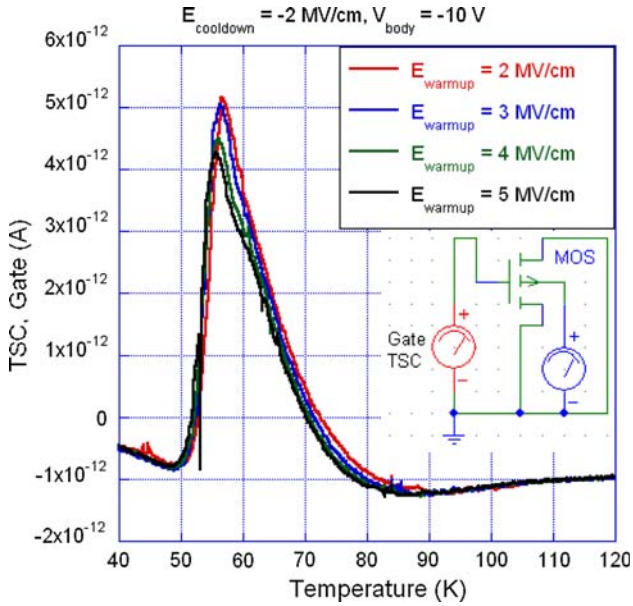

Fig. 6. An *n*-channel 4H-SiC MOSFET biased in accumulation during cooldown and inversion during warmup.

detrapping between the top of the polysilicon gate and the bottom of the inversion layer.

The resulting TSC peaks at 55 K are presented in Fig. 6. At 20 K, when the negative gate field was changed to positive, the source and drain instantaneously provided a source of inversion electrons, and the gate field terminated on the inversion layer. Regardless of the value of the warmup field, i.e., how strongly in inversion the device was biased, the magnitude of the TSC peaks remained between 4 pA and 5 pA. The measurement was repeated using a variable cooldown field ($E_{cooldown} = -2$ MV/cm to -5 MV/cm) and a constant warmup field ($E_{warmup} = 2$ MV/cm). The resulting peaks, not shown here for brevity, were virtually identical to those shown in Fig. 6. Therefore, the density of the hole accumulation layer during cooldown also did not influence the magnitude of the TSC peaks. Using Eq. 1, a trap density of 4.87×10^{11} cm^{-2} was calculated for the 2-MV/cm curve in Fig. 6.

Next, we varied the body bias while keeping the gate field constant. The field induced by V_{body} was separated from the oxide by the same inversion layer that separated the oxide peaks in Fig. 6. The TSC spectra from the body-connected electrometer are provided in Fig. 7. During warmup, the positive gate field terminated on the inversion layer, which had formed instantaneously at 20 K, as was the case in Fig. 6, and naturally the gate electrometer registered the same 55 K peaks as before (not shown to avoid redundancy). The negative body bias drew positive charge from beneath the inversion layer, which resulted in TSC peaks around 85 K.

In summary, the result of having two separate local electric fields within the device was the separation of the spatial origin of the 55 K and 80 K

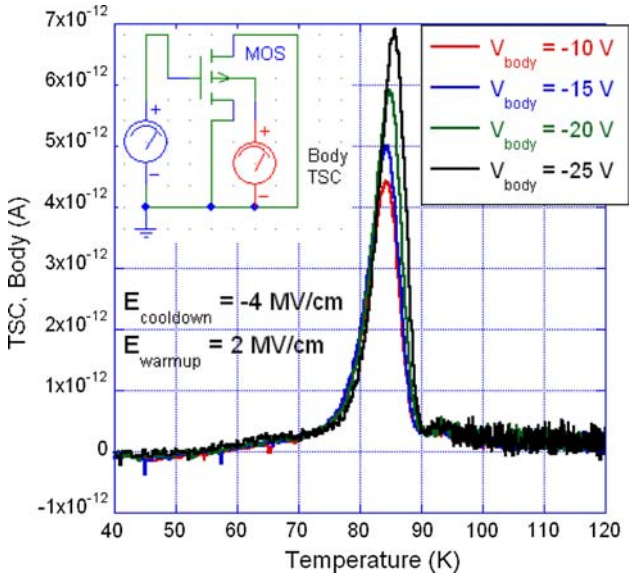

Fig. 7. TSC spectra of an *n*-channel 4H-SiC MOSFET biased in accumulation during cooldown and inversion during warmup. The TSC spectra were measured from the body of the MOSFET, with a variable V_{body} bias applied by the electrometer.

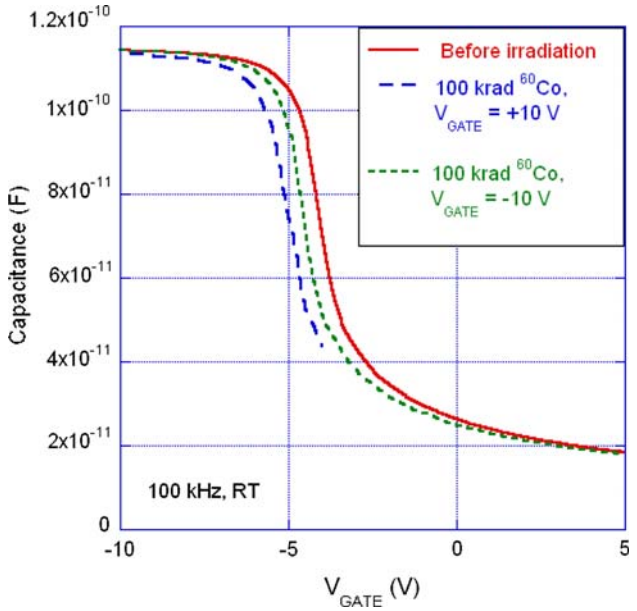

Fig. 8. Post-γ-ray irradiation room-temperature high-frequency *C–V* characteristics of a *p*-type epitaxial 4H-SiC MOSCAP.

peaks. However, this technique was insensitive to the different types of traps emitting from a given region. Curiously, detrapping from hole traps occurred at the same temperature as detrapping from Al acceptors, as observed from the excess trap concentration near 80 K in Fig. 4. Assuming an Al activation energy of 0.23 eV, a capture cross-section of $\sigma_{P,80K} = 4.02 \times 10^{-14}$ cm^2 was obtained for emission peaking at 80 K.[30] The method for separation of the 80-K peak into its constituent trap types is the subject of the next section.

Energy Separation of Carrier Traps Near 80 K (γ-Ray Irradiation Method)

In the previous section we observed that the density of traps emitting near 80 K could not be accounted for only by the acceptor concentration of the samples. We concluded that there was an additional trap present at an overlapping energy level and determined it to be a hole trap. In this section, we support this hypothesis using a γ-ray irradiation technique to separate the two types of traps in the TSC spectra.

Two MOS capacitors with TSC spectra identical to those shown in Figs. 3 and 4 were irradiated with a total dose of 100 krad using a ^{60}Co source. During irradiation, one capacitor was biased in depletion with 2 MV/cm gate field (sample A), whereas the other capacitor was biased in accumulation with −2 MV/cm gate field (sample B). The high-frequency *C–V* characteristics of the devices before and after irradiation were measured at room temperature and are presented in Fig. 8. The more negative shift in flatband voltage for sample A indicates that the radiation-induced positive net oxide charge was closer to the SiO_2/SiC interface due to the positive field during irradiation of sample A. Conversely, the negative gate field during irradiation of sample B caused the oxide charge to be pulled away from the interface, thus inducing a lower flatband voltage shift.

While further experiments are necessary, we believe that the absence of TSC peaks at 55 K in Fig. 9 suggests that the gamma irradiation had emptied any oxide traps isolated by the localized electric field method described above. On the other hand, emission from the 80-K range was distinctly different for the two samples. The 80-K peaks in Fig. 9a (sample A) did not depend on the cooldown field after irradiation, suggesting emission from a fixed density of charge in the epitaxial region. Integration of the 80-K peaks in Fig. 9a using Eq. 1 produced a trap density of 9.05×10^{15} cm^{-3}, which was very close to the nominal Al doping level of 1×10^{16} cm^{-3}. Identical measurements under 0 V warmup bias caused this trap density to decrease by about 50%, suggesting that ionization of Al dopants was assisted by the positive gate field.

The TSC spectra for sample B, shown in Fig. 9b, illustrates the effect of the negative gate field during irradiation. While the TSC spectra of sample A (Fig. 9a) suggests that the hole traps were filled by the radiation-induced charge, the shift of this charge away from the interface in sample B lowered the potential barrier, causing emission from the hole traps to be observed at a slightly lower temperature (about 77 K). The emission from the acceptor states near 80 K was nearly identical in magnitude to that observed in Fig. 9b. One could thus subtract the acceptor state density calculated

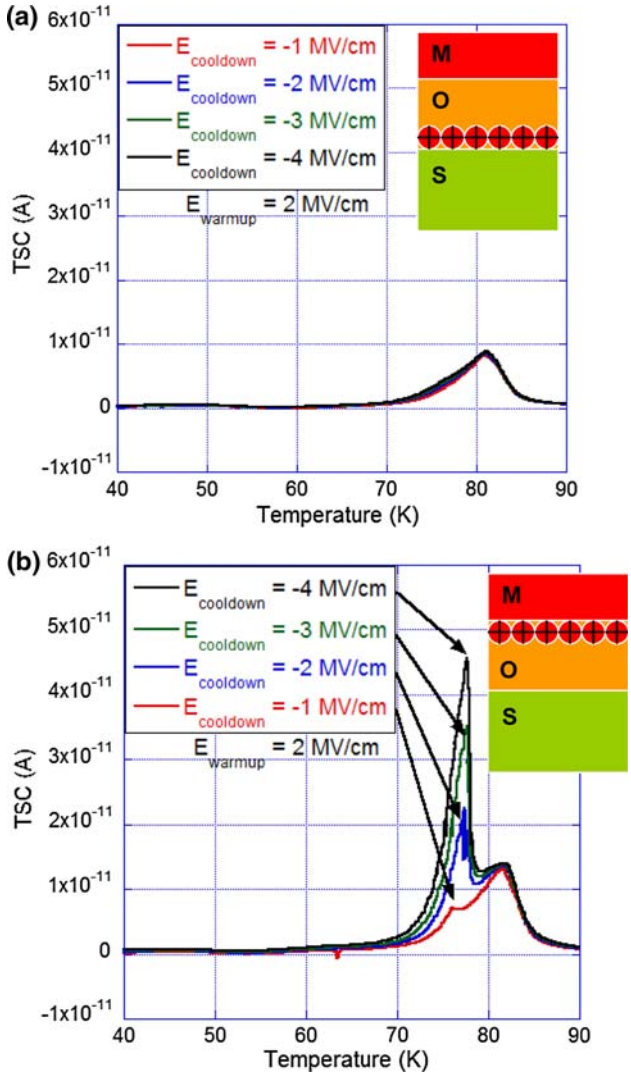

Fig. 9. Post-γ-ray irradiation TSC spectra of a *p*-type epitaxial 4H-SiC MOSCAP biased in accumulation during cooldown and depletion during warmup with a constant warmup field of E_{warmup} = 2 MV/cm. The gate bias during irradiation was (a) 2 MV/cm and (b) −2 MV/cm.

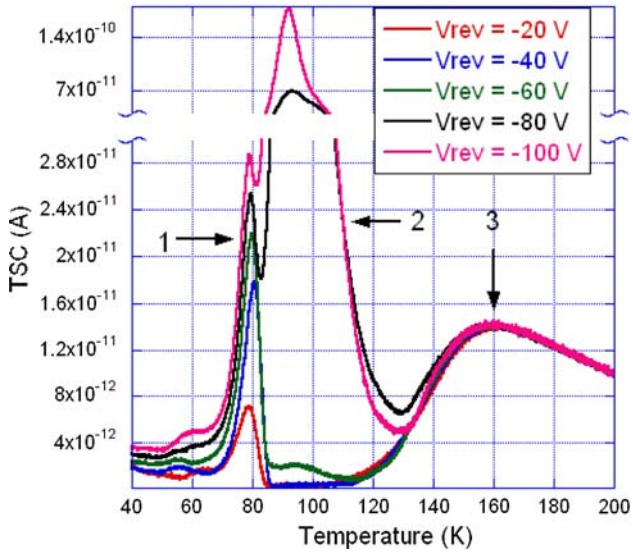

Fig. 10. TSC spectra of the source-body n^+–p junction of an *n*-channel 4H-SiC MOSFET with the gate and drain of the device floating.

from Fig. 9a from the total trap density calculated from the 80-K peaks in Fig. 4 to estimate a field-dependent hole trap density of $N_{t,hole} = 2.08 \times 10^{15}$ cm^{-3} at 2 MV/cm gate field and $N_{t,hole} = 2.5 \times 10^{16}$ cm^{-3} at 4.5 MV/cm gate field (as plotted in Fig. 5).

As a result, we have not only separated the origin of the 55-K and 80-K peaks from different regions of an MOS device using the localized field technique but have also separated the trapping mechanisms contributing to the 80-K peaks using a γ-ray irradiation technique.

TSC Spectra of MOSFET Source/Body n^+–p Junction

Another way to verify that the 55-K peaks were due to traps located within the oxide (or the polysilicon) was to obtain TSC spectra from an electric field which was (a) localized to regions of the device where neither oxide nor poly-Si were present and (b) not terminated on a SiO_2/SiC interface. This configuration was achieved by connecting an electrometer to the source-body n^+/p junction of the MOSFET, while leaving the other device terminals floating. Room-temperature current–voltage measurements were performed on the junction after each TSC measurement cycle. During cooldown, the junction was weakly forward biased (1 nA forward current at 2.5 V bias). During warmup, the junction was reverse-biased from $V_{rev} = -20$ V to -100 V, which produced the TSC spectra shown in Fig. 10. It can be seen that the magnitude of the peaks at 50 K to 55 K was negligible compared with those in Fig. 6. Their presence was attributed either to residual nitrogen donors present during epitaxial growth and compensated by the Al acceptors, or to oxide traps located in the gate overlap regions. This result supports the hypothesis that the origin of the 50-K peaks was in states not physically located in the epitaxial SiC.

The temperatures at which significant TSC was observed were 80 K (group 1), 90 K to 100 K (group 2), and 160 K (group 3). The respective trap densities calculated using Eq. 1 from TSC curves measured at $V_{rev} = -100$ V were $N_{t,1} = 2.25 \times 10^{17}$ cm^{-3} (5.62×10^{13} cm^{-2}), $N_{t,2} = 3.45 \times 10^{18}$ cm^{-3} (8.62×10^{14} cm^{-2}), and $N_{t,3} = 2.38 \times 10^{18}$ cm^{-3} (5.95×10^{14} cm^{-2}).

The three TSC peak groups varied differently with bias. The magnitude of the group 1 peaks increased with reverse bias, from -7 pA at $V_{rev} = -20$ V to -28 pA at $V_{rev} = -100$ V. This behavior is consistent with the hypothesis that TSC peaks around 80 K were partially caused by the Al

acceptor states. Their spatial distribution in the depletion region suggested that, as it expanded due to the higher reverse bias, more acceptor states would be located in the space-charge region, and the magnitude of the resulting TSC peak would be higher.

TSC peaks in group 2 were not observed at low reverse biases (−20 V and −40 V). A small peak of about 2 pA was observed at 95 K at V_{rev} = −60 V. At high reverse biases (V_{rev} = −80 V and −100 V), this peak split into two peaks at 93 K and 105 K, and their maximum current levels increased by about two orders of magnitude. The magnitude of the 93-K peak was 175 pA at −100 V reverse bias. The depletion region width, calculated at about 3 μm for this peak, suggested that the group 2 peaks were due to either substrate defect states or implantation damage deep into the epilayer.

Independent of the reverse bias applied to the source/body junction during warmup, the group 3 peaks maintained a constant magnitude of about 14 pA. However, increasing the forward bias during cooldown (2.0 V, 2.5 V, and 3.0 V) caused their magnitude to increase. Therefore, the diffusion current in forward bias during cooldown might have caused carriers to trap into defect states in the space-charge region, where the diffusion current density was high. The peaks' constant magnitude at variable depletion width in reverse bias during warmup indicates that the spatial distribution of these defect states did not extend far from the space-charge region.

Based on the TSC data presented in this work, the two TSC peaks observed on SiO_2/SiC structures were attributed to traps in the oxide (55-K peak) and to Al acceptor ionization and hole traps near the interface (80-K peak). Lysenko et al.[11] and Ólafsson et al.[12] observed for the case of 6H-SiC a dependence of the 40-K peak on the accumulation field. In our work, this dependence was observed for the 80-K peak in 4H-SiC (e.g., Fig. 4). Additionally, unlike the conclusion made by Lysenko, our data suggest that the hole traps emitting near 80 K were on the epitaxial side of the interface rather than the oxide side.

CONCLUSIONS

In this work, we reported on the application of the thermally stimulated current method to study traps in n-channel epitaxial 4H-SiC MOSFET devices. TSC spectra were first observed in p-type MOS capacitors near 55 K and 80 K. The same spectra were measured on MOSFET devices and spatially separated by utilizing electrical connections which applied separate electric fields to the oxide and bulk regions of the device. The 55-K peaks were attributed to charge in the oxide or its interface with the polysilicon layer. Using γ-irradiation, we determined that emission near 80 K was contributed by Al acceptor ionization and hole traps in the SiC epilayer near the SiO_2/SiC interface. After irradiation, the contributions from these two sources could be split into two peaks. Previous studies of MOS capacitors on 6H-SiC observed TSC spectra at similar temperatures. Defects in the source-body n^+–p junction confirmed the presence of peaks due to Al acceptor states and suggested the presence of implantation damage near the metallurgical junction, as well as defects near the n^+ SiC substrate.

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