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Simulink Behavioral Modeling of a 10-bit Pipelined ADC

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Abstract: The increasing architecture complexity of data converters makes it necessary to use behavioral models to simulate their electrical performance and to determine their relevant data features. For this purpose, a specific data converter simulation environment has been developed which allows designers to perform time-domain behavioral simulations of pipelined analog to digital converters (ADCs). All the necessary blocks of this specific simulation environment have been implemented using the popular Matlab simulink environment. The purpose of this paper is to present the behavioral models of these blocks taking into account most of the pipelined ADC non-idealities, such as sampling jitter, noise, and operational amplifier parameters (white noise, finite DC gain, finite bandwidth, slew rate, and saturation voltages). Simulations, using a 10-bit pipelined ADC as a design example, show that in addition to the limits analysis and the electrical features extraction, designers can determine the specifications of the basic blocks in order to meet the given data converter requirements.

Keywords: Behavioral modeling, analog to digital converters (ADCs), pipelined ADC, multiple digital to analog converter (MDAC), sample and hold (S/H).

1 Introduction

Data converters, analog to digital converter (ADC) and digital to analog converter (DAC), play a fundamental role in interfacing the digital processing core with the outer real analog world. ADCs can be found in a wide range of applications, spanning from imaging to ultrasound and communication systems. In particular, pipelined ADC architecture[1, 2] offers a good trade-off between conversion rate, resolution and power consumption.

Traditionally, modeling of analog and mixed signal blocks, such as data converters, has been realized at device level or at a lower functional level. This gives good accuracy and allows good modeling of the non-ideal effects present in the data converter (noise, distortion, mismatching, etc.), but the simulation time increases drastically and technology and architecture independence can be lost. However, with the increasing complexity of designs, the need for accurate and speedy models has produced a change to the current trend towards behavior modeling. Out of different approaches, the so-called "behavioral modeling" reproduces the required behavior of the original analyzed system.

This approach is motivated by the aim of obtaining a model for analysis and synthesis that respects the underlying physics and sets up the appropriate mathematical concepts from there.

Behavioral modeling uses the mathematical characteristics of each block to describe the behavior of the whole pipelined ADC. It achieves one of the best trade-offs between speed and accuracy because pre-calculated, parameterized closed-form expressions, instead of state equations, are employed to capture the dynamic behavior of analog blocks. The larger the number of non-idealities embedded into these closed-forms expressions and the more the analysis of the impact of these non-idealities involved, the better the behavioral models[3].

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Research groups working in the area of behavioral modeling for pipelined ADCs use different high level languages and alternate approaches like Matlab simulink[3−6], VHDL-AMS[7, 8] and Spice[9]. Event-driven behavioral models have been previously employed to support the design of pipelined ADCs[3−6]. However, these previous models have some drawbacks as they mostly take into account only a few sources of error. In this paper, the purpose of modeling is analyzing the non-idealities in the pipelined ADC for optimizing accuracy and linearity parameters of the converter to predict static and dynamic performance.

This paper focuses on the behavioral modeling of pipelined ADCs implemented in the very popular Matlab simulink environment. The new toolbox includes a complete set of pipelined ADC circuit models that take into account the main non-idealities which degrade the converter performance considerably. These models are implemented by combining elementary simulink library blocks in order to keep the computational cost minimum. The most significant non-idealities are modeled and building blocks for modeling sampling jitter, noise, and operational amplifier parameters (white noise, finite DC gain, finite bandwidth, slew rate (SR) and saturation voltages) are proposed.

This paper is organized as follows. In Section 2, the corresponding behavioral model blocks are presented. The major non-idealities of pipelined ADCs are described in Section 3. Finally, in Section 4, we report the simulation results obtained using the proposed blocks for a 10-bit pipelined ADC.

2 Behavioral modeling of pipelined ADCs

The pipelined ADC is constructed using switched capacitor (SC) circuits, which exploit the charge storing abilities of complementary metal oxide semiconductor (CMOS) to

achieve precise signal processing and which is preferred in mixed signal and analog-to-digital converter (A/D) interfaces. The conceptual block diagram of a generic pipelined ADC, consisting of an arbitrary cascade of k stages and a sample-and-hold (S/H) circuit at the front[3] is shown in Fig. 1 (a). Each stage resolves partial code words of length $n_i, i = 1, \cdots, k$, which are all re-ordered and combined at the digital correction block to obtain the output of the converter. The inner structure of a pipeline stage comprises of four blocks, as illustrated in Fig. 1 (b) a flash sub-ADC with $N_i \leqslant 2_i^n$ output codes, a sub-DAC with N_i output levels, a substractor, and an S/H residue amplifier with gain G_i. The latter three blocks are implemented in practice by a single subcircuit which is often referred to as multiplying digital to analog converter (MDAC). We combine the blocks of the sub-ADC and the MDAC together to get a single pipelined stage.

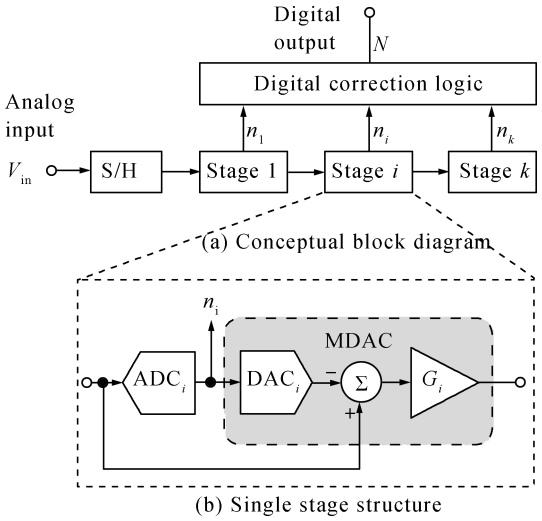


Fig. 1 Block diagram of a pipelined ADC

2.1 Sample-and-hold circuit

The S/H circuit samples the analog input and then holds the input stable for a certain time so that it can be used. The sampling capacitor (C_s) stores the sampled input signal first and then transfers the signal charge to the feedback capacitor (C_f). The S/H circuit is shown in Fig. 2[10].

The flip-around S/H circuit is shown in Fig. 2 (a). In this configuration, only one capacitor is used for both sampling and feedback. This configuration can achieve high speed because the feedback factor (the ratio of the feedback capacitor to the total capacitance at the summing node) can be much closer to one. The output voltage of the S/H is given by

$$V_{\text{out}} = 1 \times V_{\text{in}}. \tag{1}$$

2.2 Multiplying digital-to-analog converter

The MDAC is a single switched capacitor circuit that can also implement the function of S/H operation, D/A conversion, subtraction and amplification of the remainder. The MDAC circuit in the 1.5-bit/stage architecture is very simple as shown in Fig. 3 (a). The ideal behavioral model of this configuration is shown in Fig. 3 (b)[9].

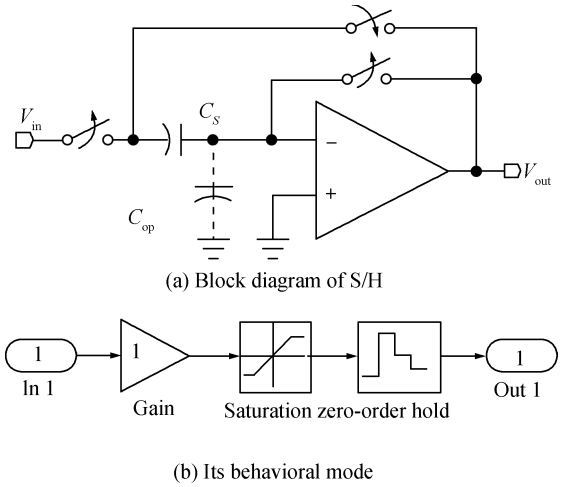


Fig. 2 The S/H circuit

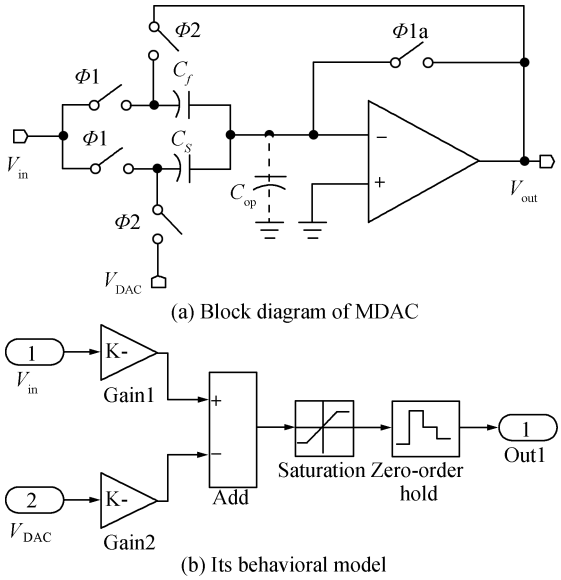


Fig. 3 The MDAC circuit

According to the charge conservation principle, the output in the hold phase is given by[11]

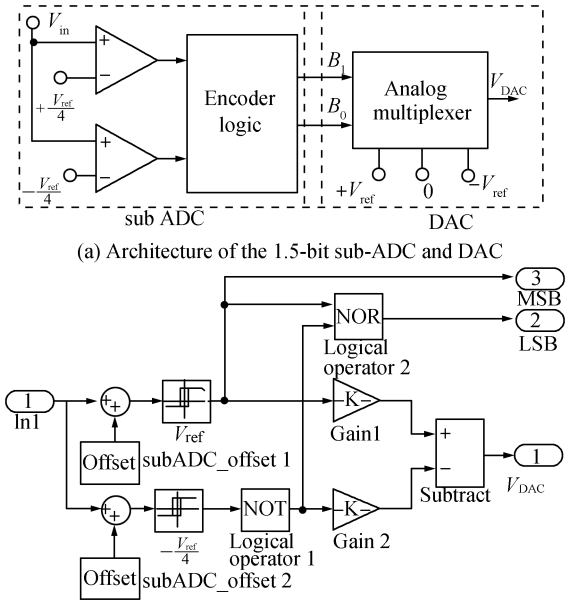
$$V_{\text{out}} = \left(\frac{C_f + C_s}{C_f}\right) \times V_{\text{in}} - \left(\frac{C_s}{C_f}\right) \times V_{\text{DAC}} \tag{2}$$

where C_s is the sampling capacitor, C_f is the feedback capacitor, and V_{DAC} is the output voltage of the sub-DAC circuit in MDAC as seen in Fig. 3 (b).

2.3 1.5-bit sub-ADC and DAC

Fig. 4 (a) presents the architecture of the 1.5-bit sub-ADC and DAC. The 1.5-bit sub-ADC consists of two comparators, the reference level of the comparators are optimally placed at $+\frac{V_{\text{ref}}}{4}$ and $-\frac{V_{\text{ref}}}{4}$. The 1.5-bit ADC has an encoder circuit to transfer the code from the comparator latch output to the binary code. Each sub-ADC stage gives a 2 bit most significant bit (MSB) and least significant bit

(LSB) with only three useful codes 00, 01 and 10 depicting the "3-level ADC" formed by two comparators. Finally, the 1.5-bit DAC converts back the digital signal of sub-ADC into an analog signal $V_{\rm DAC}$. The behavioral model for the 1.5-bit sub-ADC and DAC is shown in Fig. 4 (b).



(a) Architecture of the 1.5-bit sub-ADC and DAC

(b) Behavioral model of the 1.5-bit sub-ADC and DAC

Fig. 4 The l.5-bit sub-ADC and DAC circuit

2.4 Digital logic

The digital circuitry in the pipelined converter performs the functions of digital error correction by combining the binary results of each stage into a final N-bit binary number. It contains delay logic and correction logic. The delay logic part is composed of the delay elements used to model the function of the synchronized digital circuit. The output of each stage is given a delay block where the first stage has more delay whereas the last one has less delay. The behavioral model of the digital error correction logic mainly consists of a full adder to compose the ripple carry adder and one exclusive or (XOR) gate. In the 10-bit pipelined ADC, 16 bits (2 from each of the 8 stages) are generated and 10 effective bits are yielded, with digital correction technique at the output.

3 Pipelined ADCs non-idealities

In this section, the main non-idealities and their effects in the pipelined ADC are introduced.

3.1 The non-idealities of the operational amplifier

A major component of a switched capacitor pipelined ADC is MDAC which is made by using an operational amplifier (op-amp). An ideal op-amp has an infinite DC gain, an infinite bandwidth, no slew rate limitation, and no saturation limits.

3.1.1 Nonlinear op-amp DC gain

Ideally, the DC gain of the op-amp is infinite, theoretically its transfer function is

$$V_{\rm out} \cong A_0 \times V_{\rm in} \tag{3}$$

where $V_{\rm in}$ and $V_{\rm out}$ are the differential input and the output voltages of the op-amp, and A_0 is the amplification factor. Theoretically, A_0 is very large, near infinity, absolutely constant, and independent of frequency signal amplitude.

Unfortunately, the actual open loop gain A is limited by circuit constraints and depends on its output. The transfer function can be approximated by (4)[12]:

$$A \cong A_0 \times \left(1 + \alpha_1 |V_o| + \alpha_2 |V_o|^2 + \alpha_3 |V_o|^3 + \cdots\right) \tag{4}$$

where V_o represents the SC op-amp output and $(\alpha_1, \alpha_2, \alpha_3, \cdots)$ forms the set of parasitic nonlinear amplification factors. However, the real op-anp transfer function is shown in Fig. 5.

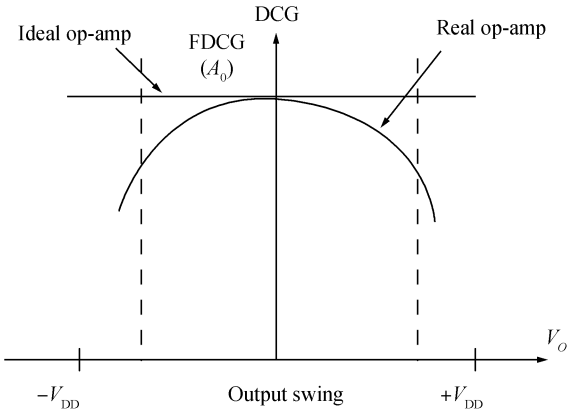


Fig. 5 DC gain of an op-amp as a function of output voltage

The actual gain is usually finite and nonlinear, which induces nonlinearities into the pipelined ADC. The transfer function of the SC circuit (S/H or MDAC) taking into account finite DC gain effect of the op-amp becomes[8]

$$V_{\rm out} = G \times V_{\rm in} \left(\frac{1}{1 + \frac{1}{A \times \beta}} \right) \tag{5}$$

where G is the ideal gain of the SC circuit, and the term inside the parentheses represents the gain error factor, where A is the real DC gain of the op-amp and β represents the feedback factor.

3.1.2 Bandwidth and slew rate

The effect of the finite bandwidth and the slew-rate are related to each other and may be interpreted as a non-linear gain[12]. The typical settling behavior of a step response is shown in Fig. 6.

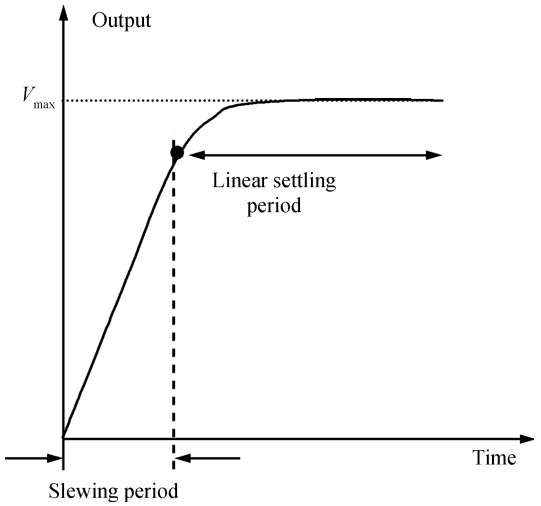


Fig. 6 Typical settling behavior of the step response

In the initial settling period, the slope of the output signal is limited by the SR of the op-amp. Once the slope of output signal is less than SR, the response goes into the linear mode. The transition point in time between them is at t_0. We add the settling error behavior into (3). This response is given by

$$V_{\text{out}} = G \times V_{\text{in}} \left(\frac{1}{1 + \frac{1}{A \times \beta}} \right) \left(1 - \mathrm{e}^{-\frac{t}{\tau}} \right). \tag{6}$$

The exponential term in the second bracket represents the settling error of the single pole op-amp, and $\tau = \frac{1}{2\pi\beta \text{GBW}}$ is the time constant of the SC circuit, where GBW and β are the unity gain frequency and feedback factor of the SC circuit respectively. The slope of this curve reaches its maximum value when $t = 0$, resulting in

$$\left. \frac{\mathrm{d}}{\mathrm{d}t} v_{\text{out}}(t) \right|_{\substack{\max \\ t=0}} = \frac{G \times V_{\text{in}} \left(\frac{1}{1 + \frac{1}{A \times \beta}} \right)}{\tau}. \tag{7}$$

We must consider two separate cases[13]:

1) The value specified by (7) is lower than the operational amplifier SR. In this case, there is no SR limitation and the evolution of V_{out} conforms to (6).

2) The value specified by (7) is larger than SR. The op-amp is in slewing mode. Therefore, the first part of the transient response of V_{out} is limited by SR, and in the other part, it reverts to the linear settling mode behavior after t_0.

$$t < t_0 : \quad V_{\text{out}} = \text{SR} \times t \tag{8}$$

$$t > t_0 : V_{\text{out}} = V_{\text{out}}(t_0) + (V_{\text{in}} G - \text{SR} \times t_0) \times \left(1 - \mathrm{e}^{-\frac{t - t_0}{\tau}} \right). \tag{9}$$

Imposing the condition for the continuity of the derivatives of (8) and (9) in t_0, we obtain

$$t_0 = \frac{V_{\text{in}} \times G}{\text{SR}} - \tau. \tag{10}$$

If $t_0 \geqslant \frac{T_s}{2}$, (8) holds for the whole hold clock period. The allowed total settling time is

$$T_{\text{settling}} = \frac{1}{2 \times f_s} \tag{11}$$

where $f_s (f_s = \frac{1}{T_s})$ is the sampling frequency, and T_s is the sampling period.

3.1.3 Op-amp thermal noise

The intrinsic thermal noise of the op-amp is the most important noise source affecting the operation of both the switched capacity (SC) MDAC and the S/H. The calculation of op-amp thermal noise is dependent on the op-amp architecture. We first assume that the noise sources include only the noises produced by input transistors in the differential pair. Fig. 7 presents a simple one pole model to calculate op-amp noise.

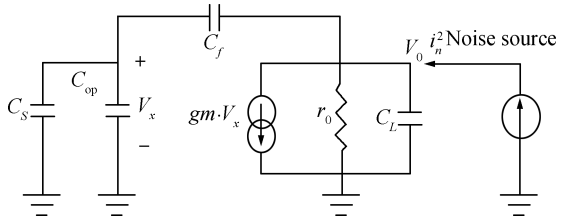


Fig. 7 AC model for op-amp noise calculation

The transfer function of this model is

$$H(s) = \frac{V_0}{\bar{i}_n} = \frac{r_0}{(1 + gm \times r_0 \times \beta) \times \left(1 + \frac{s \times C_{LT} \times r_0}{1 + gm \times r_0 \times \beta} \right)} \tag{12}$$

where β is the feedback factor, i_n is the noise current source which can be seen at the right side of Fig. 7, C_{LT} is the total load capacitance given by $C_{LT} = C_L + \beta(C_s + C_{\text{op}})$, C_L is the load capacitor, C_{op} is the input capacitor of the op-amp, and gm is the transconductance of the metal oxide semiconductor field effect transistor (MOSFET) metal oxide semiconductor field effect transistor.

The noise current source can be written as

$$\bar{i}_n^2 = \gamma \times 4KT \times gm \times \Delta f \tag{13}$$

where γ is a coefficient equal to $\frac{2}{3}$ for long channel transistors, K is the Boltzmann constant, T is the absolute temperature, and Δf is a small bandwidth at frequency f. So the input-referred noise power can be expressed as

$$\overline{V}_{\text{in}}^2 = \frac{\overline{V}_0^2}{G^2} = \frac{\int_0^\infty \left(\left| H\left(s|_{j\omega} \right) \right|^2 \times \bar{i}_n^2 \right)}{G^2} = \frac{2}{3} \times KT \times \frac{1}{\beta} \times \frac{1}{C_{LT}} \times \left(\frac{C_f}{C_s + C_f} \right) \tag{14}$$

where G is the gain of the MDAC. The op-amps in S/H and MDAC are the same. The only difference is that there is only one capacitor for sampling and holding in S/H. However, there are two capacitors C_s and C_f in MDAC ad shown in Fig. 3 (a). So it is easy to get the input-referred noise of S/H if C_s and β in (14) are set to be 0 and 1.

$$\sigma_{\text{MDAC}}^2 = \frac{2}{3} \times KT \times \frac{1}{\beta} \times \frac{1}{C_{LT}} \times \left(\frac{C_f}{C_s + C_f} \right) \tag{15}$$

where $\beta = \frac{C_s}{2^B \times C_s + C_{\text{op}}}$, $C_{LT} = C_L + \beta(C_s + C_{\text{op}})$, and B is

the stage resolution.

$$\sigma^2_{\mathrm{S/H}} = \frac{2}{3} \times KT \times \frac{1}{\beta} \times \frac{1}{C_{LT}}. \quad (16)$$

3.1.4 Flicker noise

Another major noise source for converter design is flicker noise. Flicker noise or $\frac{1}{f}$ noise (whose noise spectral density has a $\frac{1}{f}$ frequency dependence) is present due to the trapping and de-trapping effects at the silicon-oxide interface. Since flicker noise is inversely proportional to transistor gate area, this noise component typically increases with technology scaling[14]. The noise voltage can be roughly expressed in terms of frequency f as

$$V^2 = \frac{K_f}{C_{ox} \times W \times L} \times \frac{1}{f} \quad (17)$$

where K_f is the flicker noise coefficient, C_{ox} is the oxide capacitance, and W and L are the width and length respectively of the MOSFET transistor.

3.1.5 Op-amp input offset

There are two basic forms of offset which have different effects on the ADC transfer function. Firstly, there is the input offset which adds up with the input signal to the stage. This offset is mainly due to the amplifier and to a lesser extent to the switches. The transfer function in this case is of the form[15].

$$V_{\mathrm{out}_i} = G_i \left(V_{\mathrm{in}_i} + V_{\mathrm{off}_i}\right) - D_i \times V_{\mathrm{ref}} \quad (18)$$

where the offset gets multiplied up by the stage gain, V_{off_i} is the offset of the input voltage, G_i and V_{in_i} represent the gain and the input signal of the MDAC circuit, respectively. D_i is an integer which is dependent on the output of the sub-ADC, and V_{ref} is a reference voltage.

The second form of offset is that due to the comparators. This has the effect of shifting either one or both of the decision levels of the sub-ADC. The total offset from all sources must remain within the bounds of $\pm\frac{V_{\mathrm{ref}}}{4}$ [15].

3.1.6 Capacitor mismatch errors

Capacitor mismatch gain errors affect the transfer characteristic. The generalized transfer function of the ADC stage including capacitor mismatch errors is[16]:

$$V_{\mathrm{out}} = 2 \times V_{\mathrm{in}_i} \times \left(1 + \frac{\Delta_c}{2}\right) - D_i \times V_{\mathrm{ref}} \times (1 + \Delta_c) \quad (19)$$

where Δ_c is the term due to capacitor mismatch. The capacitor matching requirement for a standard 1.5-bit stage can be derived as

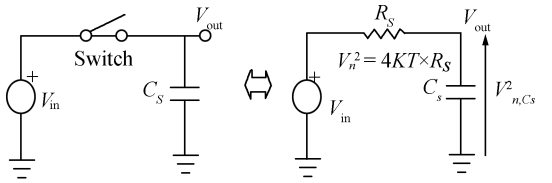
$$\sigma_{\Delta_c} \leqslant \frac{1}{3.2^{N-i-1}} \quad (20)$$

where i is the stage number and N is the number of bits. Inequality (20) shows that the capacitor mismatch error is low in the front-end, but it is superior in the higher stage resolutions.

3.2 The non-idealities of switches

3.2.1 Switching noise

The most important noise sources affecting the operation of an SC op-amp is the thermal noise associated with the sampling switches and the intrinsic noise of the operational amplifier. Fig. 8 (b) provides an equivalent circuit for noise estimation. The spectrum of the thermal noise contributed by R_s is white, $V^2_{n,Rs} = 4KT \times R_s$[16].



(a) Simple model of the samplings switch (b) Noise equivalert model of the sampling switch

Fig. 8 The sampling swith

The spectrum of $V_{n,Cs}$ is given by[16]

$$V^2_{n,C_s}(\omega) = \frac{4K \times T \times R_s}{1 + (\omega \times R_s C_s)^2}. \quad (21)$$

The noise power in the base-band is given by the integral of the noise power of all the folded bands.

Therefore, the total noise power stored on C_s when the switch goes off is[16]

$$p_{n,C_s} = \int_0^\infty v^2_{n,\mathrm{out}}(f)\,\mathrm{d}f = 4\pi T \times R_s \int_0^\infty \frac{\mathrm{d}f}{1 + (\omega \times R_s C_s)^2} = \frac{KT}{C_s} \quad (22)$$

where $f_{-3\mathrm{dB}} = \frac{1}{2}\pi R_s C_s$, R_s is the on-resistance of the metal oxide semiconductor (MOS) transistor, C_s is the sampling capacitor value, and the resistance is modeled with a noise source. The total input referred noise power (KT/C noise) of MDAC and the sample and hold amplifer (S/H) shown in Figs. 2 (a) and 3 (a) are given by (23) and (24) respectively.

$$\overline{\sigma}^2{}_{\mathrm{in,MDAC}} = \frac{KT \times (C_s + C_f + C_{\mathrm{op}})}{(C_s + C_f)^2} \quad (23)$$

$$\overline{\sigma}^2{}_{\mathrm{in,S/H}} = \frac{KT \times (C_s + C_{\mathrm{op}})}{(C_s)^2} \quad (24)$$

where C_{op} is the op-amp input parasitic capacitance. From (23) and (24), it is obvious that the sampling capacitors C_f of S/H and C_s, C_f of MDAC, and input capacitor C_{op} have a large influence on the input-referred noise power of the ADC.

3.2.2 Charge injection

Charge injection, one of the non-ideal effects of MOS switches in the input amplifier, results in the residual offset at the output nodes of the amplifier. Fig. 9 illustrates this charge injection phenomenon.

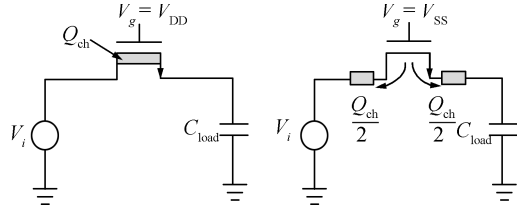


Fig. 9 Charge injection in the N-channel metal-oxide-semiconductor field-effect transistor (NMOSFET)

When the MOS switch is on and its drain-source voltage $V_{\rm ds}$ is small, the charge under the gate oxide resulting from the inverted channel is approximated by[17]

$$Q_{\rm ch} = C_{\rm OX} \times W \times L \times (V_{\rm GS} - V_{\rm TH}). \quad (25)$$

Thus, when the MOS transistor is switched off, half of the channel charge is sent to $C_{\rm load}$. As the accumulated charges in n-channel and p-channel transistors are electrons and holes, respectively, the charge injection of n-channel and p-channel switches will result in negative and positive spikes correspondingly. Their amplitude, for instance, in an N-channel metal-oxide-semiconductor field-effect transistor (NMOS) switch can be calculated by

$$\Delta V_{\rm inj} = -\frac{Q_{\rm ch}}{C} = -\frac{C_{\rm OX} \times W \times L \times (V_{\rm GS} - V_{\rm TH})}{2 \times C_{\rm load}}. \quad (26)$$

Assuming that the clock swings between $V_{\rm DD}$ and $V_{\rm SS}$, we obtain

$$\Delta V_{\rm inj} = -\frac{C_{\rm OX} \times W \times L \times (V_{\rm DD} - V_{\rm in} - V_{\rm TH})}{2 \times C_{\rm load}} \quad (27)$$

where $V_{\rm in}$ represents the input signal.

3.2.3 Clock feedthrough

In addition to channel charge injection, an MOS switch couples the clock transitions to the sampling capacitor through its gate-drain and gate-source overlap capacitance. Depicted in Fig. 10, the effect introduces an error at the output. Assuming the overlap capacitance $C_{\rm ov}$ is constant, the error can be expressed as[18]:

$$\Delta V_{\rm clk} = V_{\rm clk} \frac{C_{\rm ov}}{C_{\rm ov} + C_{\rm H}} \quad (28)$$

where $V_{\rm clk}$ is the clock signal voltage, $C_{\rm ov}$ is the overlap capacitor per unit width, and $C_{\rm H}$ is the hold capacitor. This voltage error is independent of the input level.

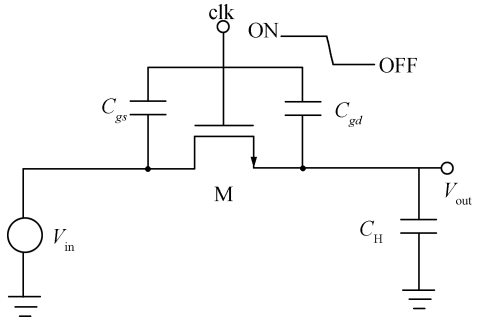


Fig. 10 Clock feedthrough in a sampling circuit

3.2.4 Nonlinear on-resistance

In actual implementations of SC circuits, on-resistance of the MOS switch can have a significant effect on the settling time of the circuit. Nonlinear on-resistance which is a signal-dependent variation of the on-resistance of the switch introduces harmonic distortion into the circuit. In addition, the one pole system composed of the finite turn-on resistance of switch (R) and sampling capacitor (C) shown in Fig. 11 determines the bandwidth of the input signal in SC circuits. The sampled input voltage is given by

$$V_{{\rm in},s} = V_{\rm in} \times \left(1 - {\rm e}^{-\frac{t}{\tau}}\right) \quad (29)$$

where $\tau = R \times C$.

Fig. 11 presents a simple MOS S/H circuit and its equivalent model for calculation of on-resistance noise in the MOS switch.

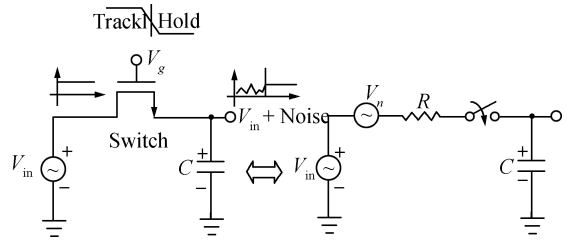


Fig. 11 A simple S/H circuit and its equivalent model for noise calculation

The nonlinear turn-on resistance can be extracted from the plot of switch resistance, and by using curve fitting. We have obtained a polynomial function, which can be used to model the effect caused by the nonlinear "on" resistance of the switch. Fig. 12 shows the behavioral model of the finite turn-on resistance of the switch.

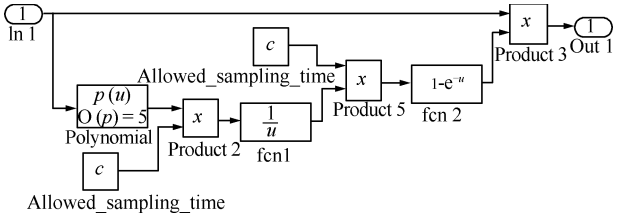


Fig. 12 Modeling the effect of the nonlinear finite turn-on resistance

3.3 Clock jitter

Jitter is defined as a random variation of sampling instants. Clock generator phase noise and sampling circuit are the cause of jitter[18]. Noise introduced by jitter can be assumed to be white, i.e, it is uniformly distributed between frequencies 0 to $\frac{f_s}{2}$. Jitter error can be reduced by oversampling the input signal. The clock jitter value of a sampled signal is represented as[19]

$$x_i'(t) = x_i(t) + \delta \times [x_i(t+1) - x_i(t)] \times f_s \quad (30)$$

where $x_i'(t)$ is the error due to the jitter deviation of δ in sample value $x_i(t)$ with a true sampling frequency f_s. Using Taylor′s series expansion, we have[19]

$$\delta \times [x_i(t+1) - x_i(t)] f_s \approx \delta \times \frac{\rm d}{{\rm d}t} x_i(t). \quad (31)$$

Clock jitter results in a non-uniform sampling time sequence, and produces an error which increases the total error power at the spectrum output of the whole pipelined ADC. This phenomenon can be observed from Fig. 13. This error is introduced when a sinusoidal signal $x(t)$ with amplitude A and frequency $f_{\rm in}$ is sampled at an instant which

is in error by an amount δ and is given by[20].

$$x(t+\delta)-x(t)\approx 2\pi\times f_{\text{in}}\times\delta\times A\times\cos(2\pi f_{\text{in}}t)=\delta\times\frac{\mathrm{d}x(t)}{\mathrm{d}t}. \quad (32)$$

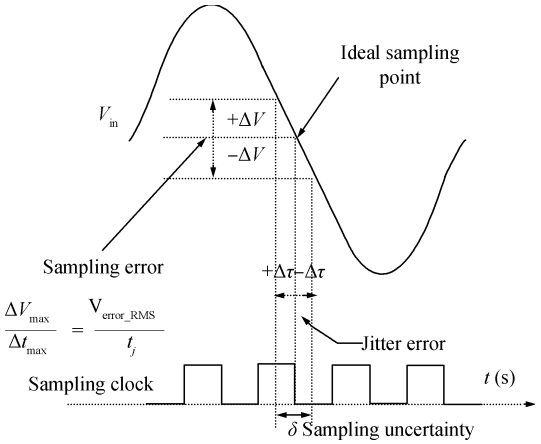


Fig. 13 Clock jitter error

Here, we assumed that the sampling uncertainty δ is a Gaussian random process with a standard deviation $\Delta\tau$[19]. Fig. 14 shows the behavioral model of the effect described by (32).

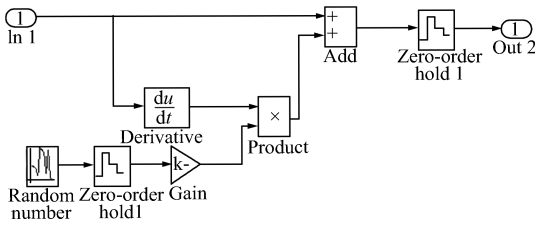


Fig. 14 Clock jitter model

4 Simulation results

To validate the proposed models with the various non-idealities affecting the operation of a pipelined ADC, we have performed several simulations on the ideal and the non-ideal model of a pipelined ADC. Post-processing data manipulation to obtain fast fourier transform (FFT), signal-to-noise ratio (SNR), and other ADC specs has been done. The design of the model was validated by reconstructing the digital output into its original form, the ideal and non-ideal models have been tested with sine wave inputs, as shown in Fig. 15.

The original input and the two digital output waveforms reconstructed are shown in Fig. 15. Figs. 16 and 17 show the FFT output for an ideal model and a non-ideal model of pipelined ADC, respectively.

As we expected, the significant noise sources make an impact on the output signal of the model of the non-ideal pipelined ADC. Fig. 18 shows the simulated differential nonlinearity (DNL) and integral nonlinearity (INL) profiles of a 10-bit ADC including various non-idealities.

It is obvious that by adding errors and variations to the ADC components, the power of the fundamental gets disturbed, and the noise floor along with the harmonic spectra increases significantly. A summary of the specifications for the 10-bit pipelined ADC is shown in Table 1.

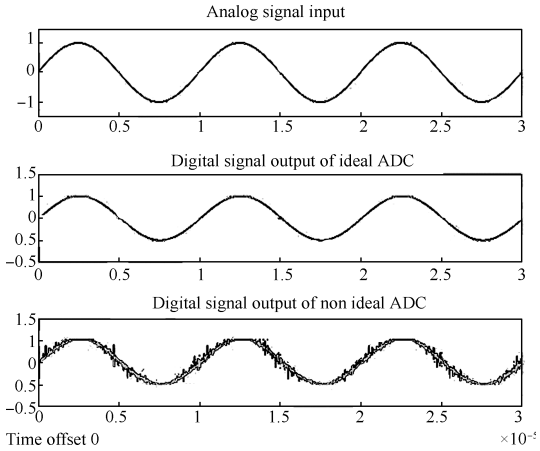


Fig. 15 Analog input and reconstructed outputs

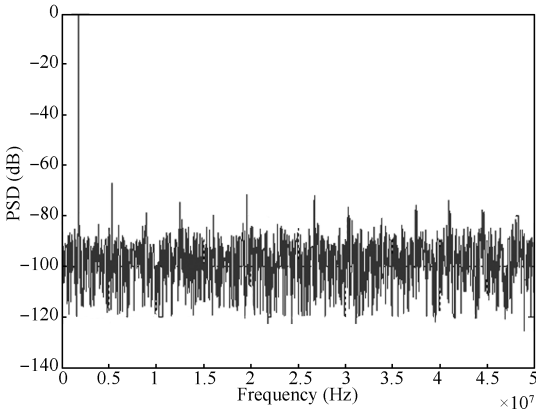


Fig. 16 FFT of the ADC output signal in the ideal case with $F_{\text{in}}=1.78$ MHz, $F_s=100$ MHz

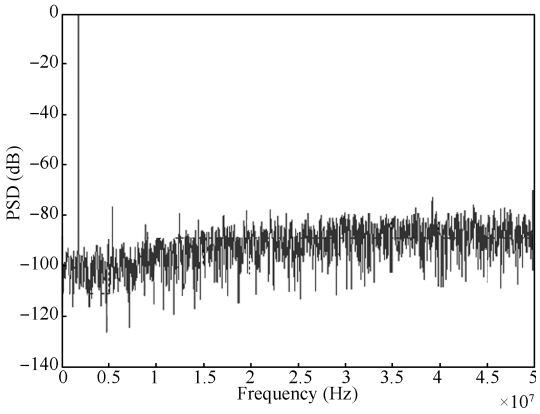


Fig. 17 FFT of the ADC output showing the effect of errors on the fundamental component and on other frequencies with $F_{\text{in}}=1.78$ MHz, $F_s=100$ MHz

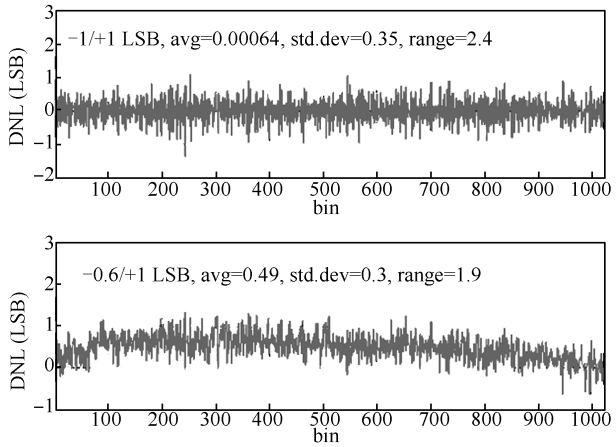


Fig. 18 DNL and INL of the non ideal 10-bit pipelined ADC

Table 2 shows the simulated DNL and INL profiles and other performance such as SNR, signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic ratio (SFDR) The DNL is found to be $-1/+1$ LSB, and the INL is $-0.6/+1$ LSB. The SFDR is around -59 dB. We can notice that the SNR degrades when the sources of noise including clock jitter, the thermal noise of the switches (KT/C) and the op-amp non-idealities (finite gain, finite bandwidth, slew-rate and saturations) are added into the non-ideal model of the ADC. The agreement between the ideal model of ADC and the non-ideal model of ADC simulations is noticeable. The comparison of our behavioral model performance (SNR, SNDR, INL, etc.) to other updated behavior models is not straightforward because very few simulation results can be found in the literature of recent years[4, 5]. A comparison between our behavioral model, including the main non-ideal effects, and real ADCs[1, 2] can be seen in Table 2. There is a good match between the proposed model and the real ADCs with little difference for SNDR and SFDR. This proves the accuracy of our behavior models. Table 2 summarizes the simulated ADC performance.

Table 1 Specifications of the 10-bit pipelined ADC

Parameter	Value
Technology	TSMC 0.18 μm
Length of MOS transistor L	0.180 μm
Width of the MOS transistor W	0.270 μm
Resolution	10 bits
Sample capacitor and feedback capacitor	$C_s = C_f = 0.4$ pF
Input capacitor of the op-amp C_{op}	0.13 pF
Hold capacitance C_{H}	1 pF
Overlap capacitance C_{OV}	0.08 fF
Oxide capacitance C_{OX}	8.78 F/m^2
Sampling frequency f_s	100 MHz
Allowed total settling T_{setling}	5 ns
Feedback factor of MDAC β	0.5
Feedback factor of S/H β	1.42
Time constant τ_{MDAC}	0.30 ns
Time constant $\tau_{\text{S/H}}$	0.17 ns
Flicker noise coefficient K_f	$3.10^{-12}V^2$.pF

Table 2 ADC performance

Parameters	This work/ ideal model	This work/non-ideal model	[1]	[2]
INL (LSB)	$-0.3/+0.3$	$-0.6/+1$	$-0.6/+0.8$	$-0.73/+0.73$
DNL (LSB)	$-0.3/+0.2$	$-1/+1$	$-1/+0.7$	$-1.44/+1.44$
SNR (dB)	66.86	63.66	*	*
SFDR (dB)	62.95	59.66	65	64.8
SNDR (dB)	66.87	63.68	54	53.6
Resolution (bit)	10	10	10	10
Technology (μm)	0.18	0.18	0.18	0.18

5 Conclusions

A design and simulation environment for medium resolution high speed pipelined ADC architectures was proposed. Both its ideal and non-ideal models were implemented and verified successfully in Matlab simulink using a 10-bit pipelined ADC with a 1.5-bit per stage architecture. The proposed set of models takes into account at the behavioral level most of the pipelined ADC non idealities, such as sampling jitter, noise, and operational amplifier parameters (white noise, finite direct current gain, finite band width and slew rate). We have shown that with a proper design environment, we simply define the proper input stimulus and we can perform specific processing of the output data. A library of behavioral models of basic blocks permits to quickly implement the behavioral description of any data converter architecture. If the behavioral model of the basic blocks is customized using key electrical parameters, the behavioral simulation will permit the designer to analyze the contribution of these parameters to the limits and to define specific blocks.

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