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Interface dipole engineering in metal gate/high-*k* stacks

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Although metal gate/high-*k* stacks are commonly used in metal-oxide-semiconductor field-effect-transistors (MOSFETs) in the 45 nm technology node and beyond, there are still many challenges to be solved. Among the various technologies to tackle these problems, interface dipole engineering (IDE) is an effective method to improve the performance, particularly, modulating the effective work function (EWF) of metal gates. Because of the different electronegativity of the various atoms in the interfacial layer, a dipole layer with an electric filed can be formed altering the band alignment in the MOS stack. This paper reviews the interface dipole formation induced by different elements, recent progresses in metal gate/high-*k* MOS stacks with IDE on EWF modulation, and mechanism of IDE.

high-*k* dielectrics, metal gate, interface dipole, MOS stack, effective work function

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As poly-Si/SiO_2 is replaced by metal gate/high-*k* stacks in the 45 nm MOS technological node and beyond, the interface becomes more complicated and there are still many challenges to be solved [1,2], such as the flatband voltage shift (V_{fb} shift) [3]. Hence, the properties of the high-*k* layer must be reconsidered carefully. It has recently been reported that the interface dipole can induce potential difference across the interface and change the band alignment of the MOS stack, and this phenomenon can be exploited to modulate the V_{fb} shift [4–6]. Elemental doping can also improve the performance of the high-*k* layer. Interface dipole engineering (IDE) by varying the dopants or inserting capping layers has attracted much attention in MOS technology. Not only can this technique control the V_{fb} shift, but also the properties of the high-*k* dielectrics can be improved [7]. This paper reviews the formation of interface dipole, recent research progresses on IDE and effective work function (EWF) modulation, as well as mechanism of IDE in metal gate/high-*k* MOS stacks.

1 Interface dipole formation in MOS stack

To control the threshold voltage (V_{th}), work function of a metal gate should be near the conduction band of Si (~4.3 eV) for nMOS and valence band (~5.2 eV) for pMOS. However, only very few metals can satisfy these requirements and furthermore, when a metal is in contact with the high-*k* layer, its Fermi-level will tend to be at the neutral level of the high-*k* layer. This phenomenon is called Fermi-level pinning (FLP) which causes EWF of the nMOS (pMOS) to be much greater (smaller) than the corresponding work function in vacuum [8]. The electron density in the metal gate can also influence the EWF [9]. Stacked metal layers used in the gate structure have been investigated. Misra et al. [10] reported that a metal gate stack using Ru-Ta alloys could yield a work function compatible with nMOS. Lin et al. [11] implanted N into a Mo gate that was

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suitable for nMOS. Cha et al. [12] obtained work functions from 4.36–5.13 eV in $Ti_{1-x}Al_xN_y$ by adjusting the N concentration and the process was applicable to both nMOS and pMOS. Jeon et al. [13] demonstrated that the work function of a metal gate could be varied by inserting a very thin metal layer between the thick metal and gate dielectrics. Unfortunately, it is still seriously restricted by the work function of the incorporated metal elements. Recently, high-*k* dielectrics with a capping layer or dopants have been investigated. The method can effectively modulate V_{th} by forming a dipole at the high-*k*/low-*k* interface. The electronegativity, χ, characterizes the capability of an atom to attract electrons. If the electronegativity difference ($\chi_A-\chi_B$) of two atoms is obvious, the atom with the higher electronegativity will attract electrons towards its nucleus thus possessing a negative polarity. In contrast, the atom with the lower electronegativity will lose electrons and has a positive polarity. The result is that the formation of an dipole can be induced. However, in an amorphous phase as shown in Figure 1(a), two local dipoles A^+-B^- and B^--A^+ in a linear arrangement will cancel each other. The magnitude of a dipole in a dielectric film is given by the product of the dipole in vacuum divided by the dielectric constant [14]:

$$D=\frac{P}{k}. \tag{1}$$

If the dipole is formed between two dielectrics with different *k* values, the local dipole A^+-B^- on the high-*k* side will be smaller than the B^--A^+ one on the low *k* side. In most cases, a thin SiO_2, either native or intentionally grown, exists at the interface between the high-*k* film and Si substrate in the MOS stack. Thus, a net dipole across this high-*k*/low-*k* interface is established as shown in Figure 1(b).

In order to control the interface dipole, dopants (Figure 2(a)) and capping layers (Figure 2(b)) are widely used in metal/high-*k* MOS stacks [15,16]. By determining the vector of the dipole moment $\boldsymbol{P}$ due to diffusion of the dopant or capping atoms, it is possible to modulate V_{th} positively in pMOS and negatively in nMOS, respectively.

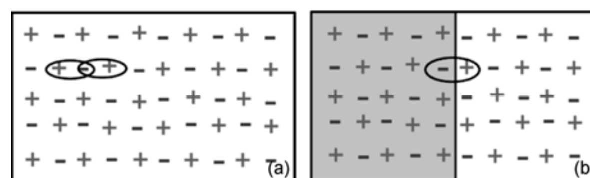

Figure 1 Schematic diagrams of the dipole formation in (a) amorphous materials and (b) at the interface between two materials with different *k* values.

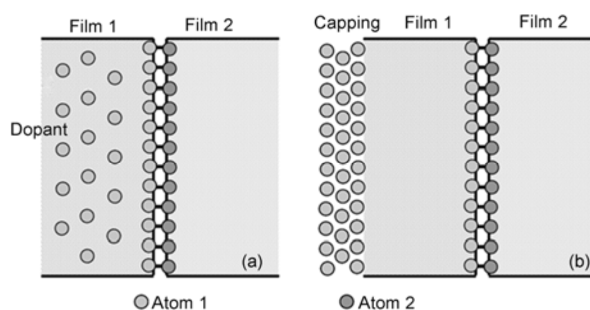

Figure 2 Interface dipole induced by (a) dopant and (b) capping layer.

Recent researches have shown that the influence of band offset by the dipole layer can modulate the V_{th} in MOS stacks. Lin and Robertson [14] have investigated the interface dipole at the high-*k*/SiO_2 interface by taking into account various dopants using *ab initio* methods. The electrostatic potential offset at the junction between the HfO_2 and SiO_2 shown in Figure 3(a) is almost identical to the valence band offsets of the MOS stack observed experimentally in Figure 3(b). Sharia et al. [17] performed a theoretical study on the SiO_2/HfO_2 interface and confirmed that the band offset could indeed be modulated if the dipoles were inserted.

The dipole layer can be regarded as a capacitor plate with the electric field denoted as

$$E=\frac{q}{\varepsilon_0\cdot S}, \tag{2}$$

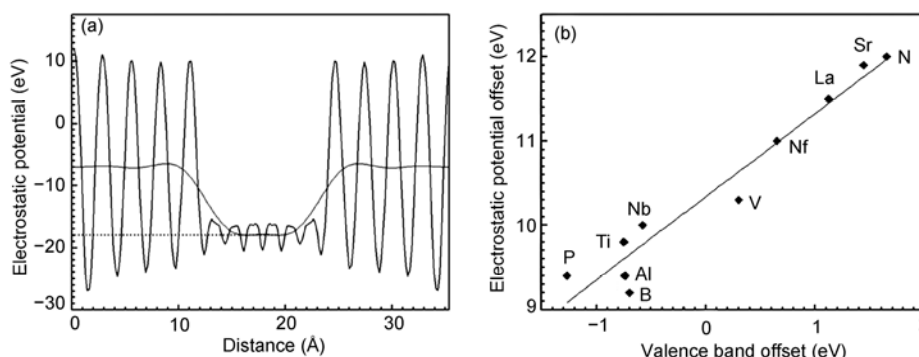

Figure 3 (a) Electrostatic potential plots across the HfO_2:SiO_2 interface; (b) comparison of calculated potential offsets and valence band offsets [14].

where S is the area of the MOS stack. The electrostatic potential difference induced at the interface is

$$\phi_d = E \cdot d = \frac{q \cdot d}{\varepsilon \varepsilon_0 S} = \frac{D}{\varepsilon \varepsilon_0 S}, \quad (3)$$

where d is the thickness of the dipole layer. When there is electrostatic potential at the interface, the potential offset will be changed. Figure 4 presents the schematic diagrams illustrating how the interface dipoles changes the potential offset. $V_{\rm th}$ is directly related to the band offset in a MOS stack and

$$V_{\rm th} = V_{\rm fb} + 2\psi_B - \frac{Q_{\max}}{C_{ox}}, \quad (4)$$

$$V_{\rm fb} = \phi_{m,\rm eff} - \phi_s - \frac{Q_f \times EOT}{\varepsilon_{ox}}, \quad (5)$$

where ψ_B is the difference in the Fermi-level, $\phi_{m,\rm eff}$ is EWF of the metal gate, ϕ_s is the work function of silicon, Q_f represents the fixed charges in the high-k layer, and EOT is the equivalent oxide thickness. In fact, $V_{\rm fb}$ can be modulated by the dipole layer as

$$\Delta V_{\rm fb} = \Delta \phi_s = \phi_d \quad (6)$$

where ϕ_d is the potential difference due to the dipole layer. Thus, if the dipole layers are produced on purpose, the $V_{\rm fb}$ shift can be effectively controlled.

2 $V_{\rm fb}$ shift modulated by interface dipole

2.1 $V_{\rm fb}$ modulation with rare earth doping in nMOS

Boasting a relatively high k value, high crystallization temperature, and good bulk properties, Hf is one of the widely used high-k elements [18]. Some rare-earth elements such as lanthanides also have good properties but they are hygroscopic [19–21]. Generally, lanthanides are incorporated into Hf-based high-k layers to improve the performance, for instance, the k value and crystallization temperature. It has recently been reported that Hf-based high-k materials doped with rare earth elements can induce a dipole layer and modulate $V_{\rm fb}$ in nMOS. Guha et al. [22] controllably shifted $V_{\rm th}$ to an ideal position in nMOS by introducing ultrathin La_2O_3

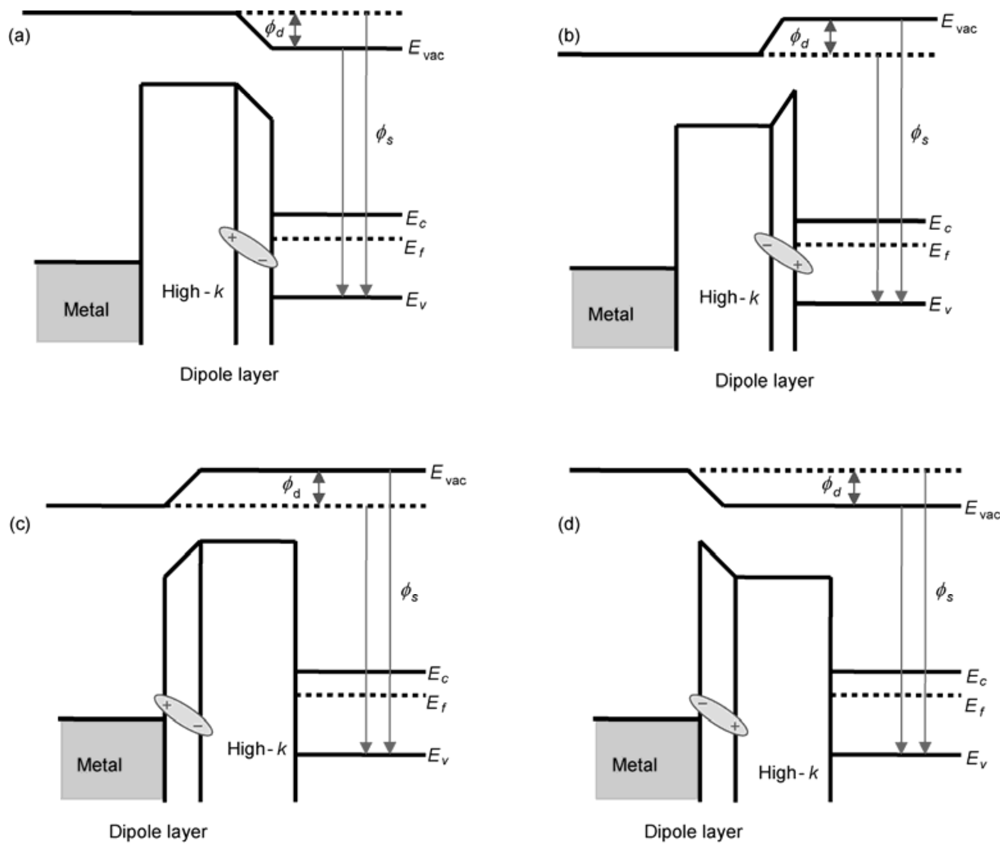

Figure 4 (a) Dipole layer at the interface between the high-k layer and Si substrate to lower the band offset; (b) dipole layer at the interface between the high-k layer and Si substrate to increase the band offset; (c) dipole layer at the interface between the gate and high-k layer to increase the band offset; (d) dipole layer at the interface between the gate and high-k layer to increase the band offset.

capping layers between the HfO_2 dielectric and TiN electrode. Alshareef et al. [23] used a thin La_2O_3 layer for surface passivation of HfSiO dielectrics. Significant shifts in the metal EWF towards the Si conduction band edge were observed. Cho et al. [24] investigated Dy_2O_3 and La_2O_3 as capping layers in Hf-based high-*k* nMOS and found that the caps could reduce V_{fb} by 0.2 V and 0.5 V, respectively.

In order to elucidate the modulation mechanism, many experiments have been performed. Kakushima et al. [25] have investigated the origin of the flat band voltage shift in HfO_2 gate dielectrics with La_2O_3 capping. As shown in Figure 5(a), capacitors with La_2O_3 on SiO_2 show a negative shift in V_{fb} regardless of thickness, but capacitors with HfO_2 on SiO_2 show a positive V_{fb} shift. As shown in Figure 5(b), when the thickness of the La_2O_3 is small (from 0.11 to 0.27), V_{fb} also shifts to a negative direction. It implies that the V_{fb} shift with La incorporation is not induced by the fixed charges. The interface dipole model has been proposed to explain the V_{fb} shift [25]. In fact, there are several reasons for the dipole formation including the group electronegativity, oxygen vacancies, and oxygen ion density.

Guha et al. have proposed that the reaction $La_2O_3 = 2La'_{Hf} + 3O_O^x + V''_O$ occurs when there is a La_2O_3 capping layer between the high-*k* layer and Si substrate. La substitution of Hf forms a negatively charged defect (La'_{Hf}) and a positively charged oxygen vacancy defect to ensure charge neutrality. When there are two kinds of defects in the interface between the high-*k* layer and Si, a dipole forms [22]. The interface dipole model has been investigated using rare earth doped Hf-based high-*k* nMOS [7,26,27]. It has been observed that V_{fb} tuning depends on the rare earth type and diffusion in the MOS stacks. The electronegativity and ionic radii of the rare earth cations determine the magnitude of the interface dipole moment and the following trend of V_{fb} modulation, Sr < Er < Sc+Er < La < Sc< none as illustrated in Figure 6(a), is attributed to the interface dipole due to charge transfer during Hf-O-RE formation as shown in Figure 6(b) [7,28]. Kita et al. [29] have also investigated the origin of electric dipole formed at high-*k*/SiO_2 interface. They propose that the oxygen areal density difference at the high-*k*/SiO_2 interface should be considered an intrinsic cause for the dipole formation. Oxygen movement from the higher-oxygen-density side to the lower-oxygen-density one creates an oxygen vacancy inducing charge transfer and forming the dipole, as shown in Figure 7. Since most rare earth oxides have smaller oxygen areal densities than SiO_2, the interface dipole will modulate the V_{fb} of nMOS to the negative direction [29].

2.2 V_{fb} modulation with Al incorporation in pMOS

In pMOS stack, one of the challenges encountered is the aggressive V_{fb} shift to the negative direction, particularly, the V_{fb} roll-off phenomenon that emerges with scaling of the interlayer SiO_2 (IL SiO_2) [30]. As discussed above, the V_{fb} shift is influenced by the interface dipole. When the SiO_2 layer becomes ultrathin, the V_{fb} roll-off phenomenon emerges. It has been shown that the dissociated O diffuses into the IL SiO_2 during thermal annealing and when the IL-SiO_2 becomes ultrathin, the O=Si dipole will form at the IL-SiO_2/Si interface. Because of its relatively large dipole moment, a sharp V_{fb} roll-off occurs [31]. Besides, there are other dipoles to induce the V_{fb} shift.

Much attention has been paid to control the V_{fb} shift in pMOS. Experiments have indicated that aluminum incorporation into Hf-based high-*k* dielectrics can provide an additional dipole which has the opposite direction to the original dipole to suppress the aggressive V_{fb} shift. Sharia et al. [32] have conducted a theoretical study on the effects of Al doping in the SiO_2/HfO_2 heterostructure. Their calculation suggests that at the interface between the Hf-based high-*k* layer and Si substrate, the Si-O-Hf dipole exists due

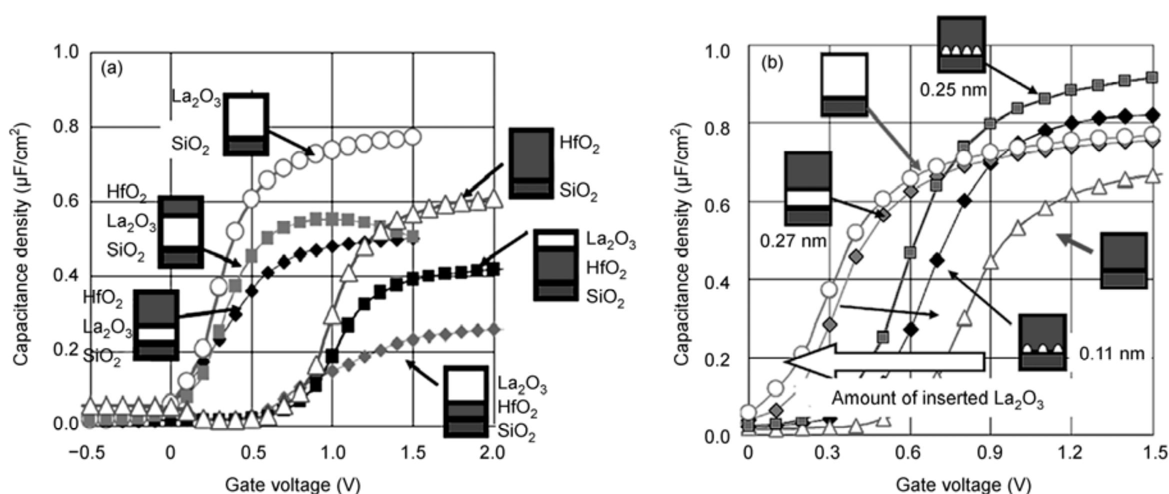

Figure 5 (a) *C-V* characteristics of high-*k* stacked MOS capacitors with SiO_2 IL; (b) *C-V* curves of W/HfO_2/SiO_2/Si capacitors with different ultra-thin La_2O_3 insertion at HfO_2/SiO_2 interface [25].

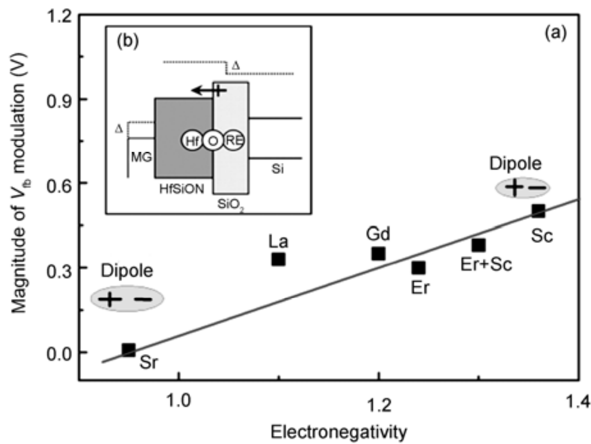

Figure 6 (a) Magnitude of V_{fb} modulated with dopant electronegativity affecting the dipole moment and (b) dipole formation at the high-*k*/low-*k* interface [7].

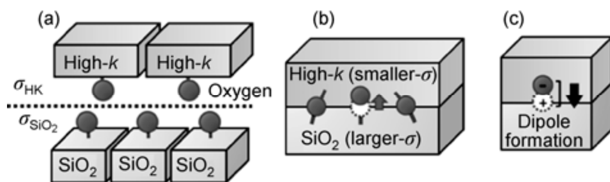

Figure 7 Dipole formation at the high-*k*/SiO_2 interface due to the difference in the areal density of oxygen atoms (σ). (a) Different σ at the interface; (b) movement of oxygen when the two sides make contact; (c) oxygen transfer in the form of negatively-charged ion creating the positively-charged oxygen vacancy in higher-σ oxide and negatively charged center in lower-σ oxide [29].

to the different electronegativity between Si and Hf. The incorporated Al tends to accumulate near the SiO_2/HfO_2 interface to reduce the amount of oxygen in that region. Oxygen is responsible for screening the interfacial dipole formed due to the charge transfer between Hf and Si and hence, a higher oxygen deficiency in the interfacial region increases the Hf-Si interface dipole, as shown in Figure 8 [32,33]. Here, the electronegativity values of Si and Hf are 1.9 and 1.3, respectively. The influence of the dipole on V_{fb} presented in Figure 4(a) modulates V_{fb} to the positive direction.

Several methods to alleviate the V_{fb} roll-off phenomenon adopt the interface dipole engineering technology. It has been reported that a 5 nm Ta remote reactive inserting layer on the W/HfO_2 (3 nm)/beveled SiO_2/Si MOS stack can alleviate V_{fb} roll-off by absorbing oxygen from the gate stack to reduce the O=Si dipole [34]. Besides, inserting a top SiO_2 layer 1–3 nm thick between the metal gate and high-*k* dielectrics is an effective method to alleviate the V_{fb} roll-off [35]. However, when the top interlayer is thicker than ~3 nm, the V_{fb} roll-off phenomenon will reappear. We have studied the mechanism [31]. It can be explained by an opposite dipole layer induced by oxygen diffusion from the high-*k* layer to the top SiO_2 layer when the thickness of the top layer SiO_2 is less than the diffusion depth.

3 Dual-dipole formation in MOS stack

As aforementioned, Al and rare earth doped HfO_2 can modulate the V_{fb} shift in pMOS and nMOS, respectively. These dopants can also improve other MOSFET properties. Umezawa [36] reported that when La was incorporated into HfO_2, the formation energy of a neutral oxygen vacancy in the vicinity of substitutional La in a Hf site was 0.7 eV larger than that in pure HfO_2. This was indicative of reduced oxygen vacancy concentration. Xu [37] reported the fabrication of HfLaON gate dielectrics with an EOT of 0.62 nm to suppress tunneling leakage. La doping was demonstrated to enhance the *k* value of the dielectrics and Alshareef et al. [23] observed that the addition of Al into Hf-based high-*k* materials could passivate the oxygen vacancy V_0^+ which induced midgap states but there was with little influence by other aspects of the defects . Aluminum has also been observed to enhance the crystallization temperature of Hf-based high-*k* dielectrics [38]. It decreases the *k* value on the other side and hence, Al and La co-incorporation into Hf-based high-*k* materials can improve the MOS performance comprehensively. However, how to control the effects of the opposite dipoles on the V_{fb} shift as a result of Al and La incorporation remains a challenge.

It is feasible to use two opposing interface dipoles to shift V_{fb} in a single metal gate/high-*k* stack. Lim et al. [5] used both n-type and p-type in the interface dipole for EWF modulation in the same gate stack. They introduced 14%–19% Al into the Mo gate and the EWF of the gate on HfLaO was increased by ~0.6 eV after rapid thermal annealing at 950°C, as shown in Figure 9. The increased EWF can be explained based on the difference in the polarity

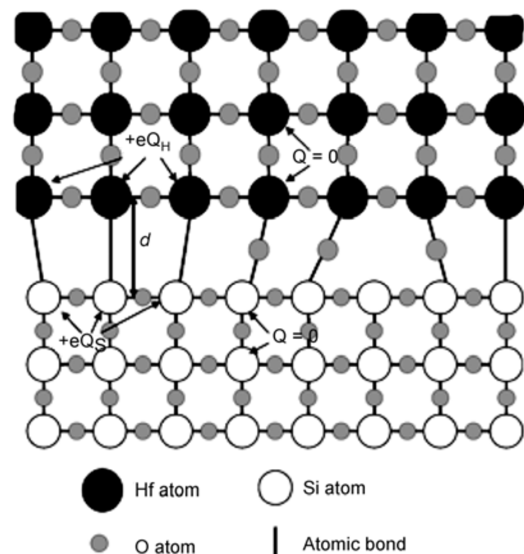

Figure 8 Cross-sectional view of the model of a high-*k*/SiO_2 interface. The dipole is assumed to form only between Hf and Si directly involved in the interface bonds [33].

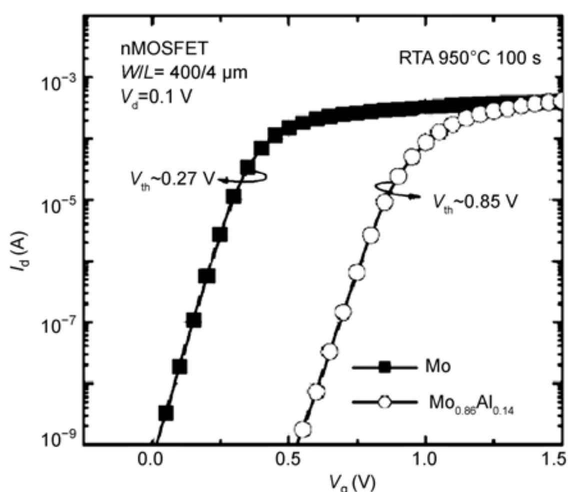

Figure 9 V_{th} shift of ~0.6 V observed from nMOSFETs with Mo/HfLaO and $Mo_{0.88}Al_{0.12}$/HfLaO gates [5].

of the La- and Al-based dipoles at the high-*k*/SiO_2 interface [5]. Ultrathin terbium (Tb) and Al-based interlayers have been utilized in the same MOS stack and the results show that the EWF of the gate can be adjusted to 0.7–0.8 eV by manipulating the interface dipole which is controlled by varying the thickness of the interlayers [21].

The diffusion behavior of Al and La in the TiN/LaN/AlN/$HfSiO_x$/Si MOS stack has been investigated. Recent results show that Al-O replaces Al-N to form the Al-O dipole layer between the TiN and high-*k* layer after annealing. Meanwhile, La diffuses into $HfSiO_x$ and the La-based dipole can be controlled by the Al-based interlayer. As shown in Figure 10(a), a positive V_{fb} shift of about 0.7 V is observed from the annealed sample and the hysteresis is obviously suppressed implying a small charge trapping density. It is proposed that the Al-O dipole is formed in the AlO_x interfacial layer as shown in Figure 10(b). Meanwhile, the La-based dipole is suppressed by the Al-based interlayer. The dominating Al-O dipole in the MOS stack builds up an internal electric field *E* and modulates V_{fb} in the MOS stack as shown in Figure 10(c) [39]. These results provide insights to interfacial dipole engineering.

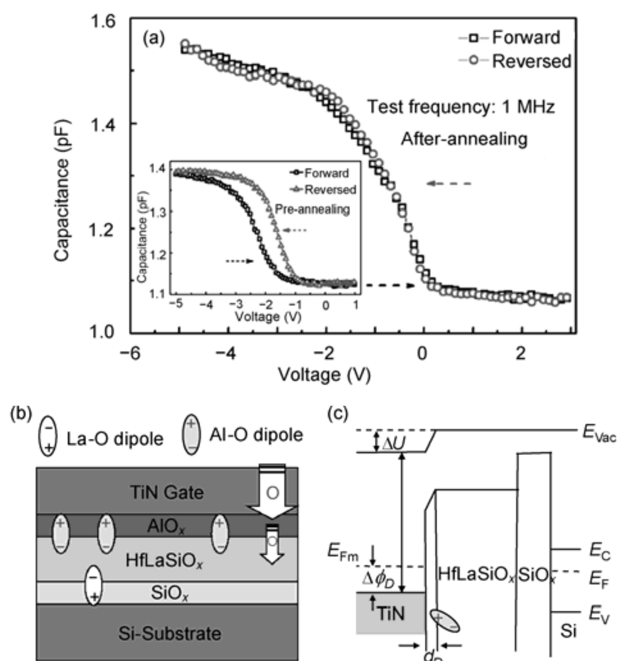

Figure 10 (a) Forward-and-reverse *C-V* curves acquired from the pre-annealed and annealed samples; (b) diagram of the dipole distribution in the MOS stack for the annealed sample; (c) diagram of the band alignment modulated by the Al-O dipole [39].

4 Conclusion

The progresses of IDE in MOSFETs are reviewed. Rare-earth elements (La, Dy) are usually introduced into Hf-based high-*k* layers to modulate the V_{fb} shift in nMOS and Al can modulate the V_{fb} shift in pMOS. IDE also provides a feasible way to introduce both Al and rare-earth elements into Hf-based high-*k* layers. The process not only controls the V_{fb} shift by the interface dipole but also improves the MOS properties comprehensively. IDE is also an effective technique to modulate the properties of materials or devices composed of multilayered thin films.

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