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Guest Editorial: Implementation Issues in System-on-Chip

Peeter Ellervee[1] · **Jari Nurmi**[2]

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We are delighted to present this special issue of the Journal of Signal Processing Systems on Implementation Issues in System-on-Chip.

During the past two decades, System-on-Chip (SoC) has grown from a futuristic idea to a stabilized mainstream paradigm for electronic system design and implementation. However, it keeps posing challenges to the designers and researchers on multiple levels and in multiple disciplines. The aim of this special issue is to provide samples on quality research targeting to solve implementation issues and investigate design case studies from different points of view in SoC design. The issues addressed include power efficiency, complexity management and security in embedded integrated systems.

This issue consists of seven papers that are briefly discussed as follows:

The first article, by Feriel Ben Abdallah, Chiraz Trabelsi, Rabie Ben Atitallah, and Mourad Abed on "Model-Driven Approach for Early Power-Aware Design Space Exploration of Embedded Systems" (10.1007/s11265–016–1144-3) discusses a model-driven engineering approach for SoC design-space exploration. In "Power Mitigation by Performance Equalization in a Heterogeneous Reconfigurable Multicore Architecture" (10.1007/s11265–016–1142-5) by M. Waqar Hussain, Henry Hoffmann, Tapani Ahonen and Jari Nurmi, the authors present a self-aware heterogeneous architecture for dynamically managing power and energy consumption of the computing platform. Martin Broich and Tobias G. Noll tackle energy efficiency and design complexity of communications SoCs in their paper "Optimal Datapath Widths within Turbo and Viterbi Decoders for High Area- and Energy-Efficiency" (10.1007/s11265–016–1140-7).

In the article "A Customized Many-Core Hardware Acceleration Platform for Short Read Mapping Problems Using Distributed Memory Interface with 3D-stacked Architecture," (10.1007/s11265–016–1204-8) the authors Pei Liu, Ahmed Hemani, Kolin Paul, Christian Weis, Mattias Jung and Norbert When apply advanced architecture and implementation techniques to a DNA sequencing problem. Essentially, it is an approach to improve the performance of hash-index based short read mapping algorithm using a hardware acceleration platform. The paper "Design of a Residue Number System Based Linear System Solver in Hardware" (10.1007/s11265–016–1146-1) by Jiri Bucek, Pavel Kubalik, Robert Lorencz and Tomas Zahradnicky is focused on error-free solution of dense linear systems using residual arithmetic in hardware. Their implementation is useful for solving large nonsingular systems of linear equations with integer, rational or floating-point coefficients with arbitrary precision.

Christoforos Kachris, Dionysios Diamantopoulos, Georgios Syrakoulis and Dimitrios Soudris present an energy-efficient scheme for MapReduce that is a programming framework for distributed systems that is used for automatically parallelizing and scheduling the tasks to distributed resources, in their paper "An FPGA-based Integrated MapReduce Accelerator Platform"(10.1007/s11265–016–1108-7). And finally, security issues are addressed by Elena Dubrova, Mats Näslund, Gunnar Carlsson, John Fornehed and Ben Smeets in the paper "Two Countermeasures

✉ Peeter Ellervee
peeter.ellervee@ttu.ee

Jari Nurmi
jari.nurmi@tut.fi

[1] Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia

[2] Tampere University of Technology, Korkeakoulunkatu 1, 33720 Tampere, Finland

Against Hardware Trojans Exploiting Non-Zero Aliasing Probability of BIST" (10.1007/s11265–016–1127-4).

The special issue was preceded by the International Symposium on System-on-Chip, held in Tampere, Finland in October 2014. The articles, hand-picked among the top contributions in the symposium, have been substantially extended and thereafter undergone two rounds of rigorous peer-review according to the journal's high standards. We would like to thank all the reviewers involved for their invaluable input, and to express our appreciation to the authors for their contributions.

We sincerely hope that you enjoy this special issue and can find useful takeaways for your own future research.

Peeter Ellervee, Jari Nurmi March 24, 2017.

Prof. Peeter Ellervee received his Diploma Engineer degree in computer engineering from the Tallinn University of Technology (TTU, Estonia) in 1984, and his Ph.D. degree in electronic systems design from Royal Institute of Technology (KTH, Stockholm, Sweden), in 2000. He has been working as an engineer and researcher at TUT (1984-1992), a guest researcher and Ph.D. student at KTH (1993-2000). Since spring 2000 he works at TTU - researcher and Associate Professor until fall 2004. Today he is a full Professor in digital systems design at Department of Computer Systems. His has taught or is teaching courses about Digital Systems, Computer Hardware, Hardware Description Languages and Modeling, and VLSI Synthesis and CAD. He is head of Computer and Systems Engineering study programs at bachelor and master levels. His research interests include behavioral and system level syntheses, hardware-software co-design, hardware description languages. He has published over 100 internationally reviewed papers in these areas and holds one patent. Member of IEEE from year 2000. He has been SP/CAS/SSC Chapter Chair of Estonia Section (2005-2008) and is currently IEEE Estonia Section Chair.

D.Sc. (Tech) Jari Nurmi works as a Professor at Tampere University of Technology, Finland since 1999, in the Faculty of Computing and Electrical Engineering. He is working on embedded computing systems, System-on-Chip, wireless localization, positioning receiver prototyping, and software-defined radio. He held various research, education and management positions at TUT since 1987 (e.g. Acting Associate Professor 1991-1994) and was the Vice President of the SME VLSI Solution Oy 1995-1998. Since 2013 he is also a partner and co-founder of Ekin Labs Oy, a research spin-off company, now headquartered in Silicon Valley as Radiomaze, Inc. He has supervised 19 PhD and over 130 MSc theses at TUT, and been the opponent or reviewer of 33 PhD theses for other universities worldwide. He is a senior member of IEEE, and member of the technical committee on VLSI Systems and Applications at IEEE CAS. In 2004, he was one of the recipients of Nokia Educational Award, and the recipient of Tampere Congress Award in 2005. In 2011 he received IIDA Innovation Award, and in 2013 the Scientific Congress Award and HiPEAC Technology Transfer Award. He is a steering committee member of four international conferences (chairman in two). He has edited 5 Springer books, and has published over 350 international conference and journal articles and book chapters.