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Guest Editorial: New Frontiers in Signal Processing Applications and Embedded Processing Technologies

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Signal processing technologies increasingly pervade and enable a very large and expanding range of applications including wireless communications, smart cameras, 'big data' analytics systems and many many more. The variety of architectural, algorithmic and design technologies required for their realisation pose a challenging problem to designers of these systems, necessitating consideration of, for instance, computer arithmetic, baseband signal processing for next-generation wireless communications, advanced programmable multicore and heterogeneous processing architectures and programming approaches. This issue includes leading works in each of these areas in exposition of the sheer breadth of design requirements for application-specific embedded signal processing.

A strong theme of achieving high-performance and efficient baseband signal processing architectures is evident in two papers. In "3.2 Gbps Channel-Adaptive Configurable MIMO Detector for Multi-Mode Wireless Communication" (10.1007/s11265-015-1093-2) the authors present a run-time adaptive detector approach for multiple-input, multiple-output wireless communications so fundamental to 4G and 5G communications standards such as Long-Term Evolution (LTE) and LTE-Advanced. This work demonstrates the key role that adaptivity plays in ensuring these systems remain efficient as the number of antennas and modulation density increases. In addition, the paper "A Noise-Robust Convex-Optimized Positioning System Based on Code-Aided RSS Estimation and Virtual Base Station Transform" (10.1007/s11265-015-1082-5) demonstrates a unique realisation of a noise-robust positioning system which employs RSS estimation, particle filtering and embedded convex optimization.

The strong emergence of computer vision as a key enabler in next generation cyber-physical systems is also in evidence, with three papers on this theme. "An Energy-efficient Hardware Implementation of HOG-based Object Detection at 1080HD 60 fps with Multi-scale Support" (10.1007/s11265-015-1080-7) describes realisations of key Histogram of Oriented Gradients (HOG) and Support Vector Machine (SVM) components whilst "PULP: A Ultra-Low Power Parallel Accelerator for Energy-Efficient and Flexible Embedded Vision" (10.1007/s11265-015-1070-9) describes a more general computer vision processing architecture design specifically for system demanding such capabilities on very restricted power budgets. Finally, "A Neuromorphic Architecture for Context Aware Text Image Recognition" (10.1007/s11265-015-1067-4) describes a highly novel brain-inspired approach to intelligent text recognition along with a memristor-based crossbar array for its realisation.

Whilst the needs of new application areas such as these are pressing, it is notable that addressing the fundamental performance and cost of signal processing architectures remains a very important avenue of research. This is evidenced by two papers also included here. In "Dataflow Programs Analysis and Optimization Using Model Predictive Control Techniques" (10.1007/s11265-015-1083-4) the authors describe techniques for analysis of trace graphs derived from autocoded

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realistions of dataflow application models in order to derive implementations with nearly-optimal buffering. In addition, "Instrumentation-driven Validation of Dataflow Applications" (10.1007/s11265-015-1073-6) addresses resolution of disparities between the modelled behaviour of dataflow applications and their realisation brought about by a mismatch between intended dataflow behaviour and that realised in a resulting program.

In addition, four other papers address fundamental operational and efficiency capabilities of embedded signal processing architectures. "Energy-adaptive Signal Processing Under Renewable Energy" (10.1007/s11265-015-1071-8) describes a technique for energy-adaptive embedded signal processing, considering not only energy consumption but also energy harvesting and storage, "Computation-skip Error Mitigation Scheme for Power Supply Voltage Scaling in Recursive Applications" (10.1007/s11265-015-1096-z) proposes mitigation techniques to minimise the effect of voltage scaling beyond critical thresholds. "A Multistage Architecture for Statistical Inference with Stochastic Signal Acquisition" (10.1007/s11265-015-1020-6) describes a technique based on arrays of binary comparison sensors which exploits statistical inference to design signal acquisition interfaces and inference systems with stochastic devices. "Improving Code Density with Variable Length Encoding Aware Instruction Scheduling" (10.1007/s11265-015-1081-6) addresses optimising the use of implicit NOPs in Very Long Instruction Word (VLIW) architectures.

John McAllister received the Ph.D. degree in electronic engineering from Queen's University Belfast, Belfast, U.K., in 2004. He is currently a Senior Lecturer in the same university, where he leads a group of researchers in embedded architectures, and electronic system level design technologies for streaming applications, with a specific focus on FPGA targets. He is a co-founder of Analytics Engines Ltd. Dr. McAllister is a member of the IEEE Signal Processing Society and its Technical Committee on Design and Implementation of Signal Processing Systems (DISPS). He is Chief Editor of SigView, the IEEE SPS tutorial library, an Associate Editor of the IEEE Transactions on Signal Processing and a member of the Editorial Board of Springer Journal of Signal Processing Systems. He serves on the program committees of a number of IEEE conferences, including the International Conference on Acoustics, Speech and Signal Processing (ICASSP), and the Workshop on Signal Processing Systems: Design and Implementation (SIPS).

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