Journal of Electronic Testing (2018) 34:105
https://doi.org/10.1007/s10836-018-5728-7

Editorial

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Received: 8 April 2018 / Accepted: 8 April 2018 / Published online: 16 April 2018
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The articles in this issue feature fault tolerance, technology-dependent faults, test compression, automatic test equipment, machine learning applied to fault diagnosis and hardware security, and RF behavior of semiconductors. Some parts of the second paper were presented at the *Eighteenth IEEE Latin American Test Symposium* (LATS) held during March 13–15, 2017 in Bogota, Columbia.

Authors of the first article are Sun, Lv, Zhang and Xie from Hefei University of Technology, Hefei, China. They give fault-tolerant designs for three-input and five-input majority gates using quantum-dot cellular automata (QCA) cells. Using these gates, they design multi-bit adders that are more economical than the previous QCA implementations.

The second paper proposes a bridge defect criticality (BDC) metric that depends on the degree of detectability and likelihood of occurrence of a bridging defect. The authors, Forero and Champac of National Institute for Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico, and Galliere and Renovell of Laboratory of Informatics, Robotics and Microelectronics of Montpellier (LIRMM), University of Montpellier/CNRS, Montpellier, France, suggest that product quality will improve by putting more effort in testing faults with higher BDC values.

The third paper addresses the problem of unknowns in scan testing when test compression is used. The authors propose a hybrid scan architecture in which a selected set of flip-flops is excluded from the decompressor-compressor test and placed in a separate external scan chain. This results in reduced test pattern count without loss of the fault coverage. Contributors are Shantagiri and Kapur from Jain University, Bengaluru, India.

Authors of the fourth paper are Terao, Nakura, Ikeno, Iizuka and Asada of University of Tokyo, Tokyo, Japan, and Ishida and Kusaka from Advantest Corporation, Gunma, Japan. They address the problem of impedance mismatch between automatic test equipment (ATE) and a device under test (DUT). The mismatch occurs due to dynamic changes in the impedance of the DUT as the test runs. It can cause fluctuations in the supply voltage resulting in failure of a good DUT. The proposed solution involves sensing and filtering of such fluctuations.

El-Mandouh of Mentor Graphics Siemens Business, Cairo, Egypt and Wassal from Cairo University, Cairo, Egypt address post-silicon debugging in the next paper. They monitor a selected set of signals using an FPGA prototype. Map-Reduce, an off-line big-data analysis program, then processes the collected data. Machine learning techniques cluster and classify signal traces to localize design bugs. The authors inform us that Cairo University undergraduates, Laila Maher, Moutaz Samir and Yasmin Hossam, assisted them in building the bug localization module and with experimental trials for training and exercising the clustering module.

Next, Elnaggar and Chakrabarty of Duke University, Durham, North Carolina, USA examine machine learning techniques for hardware security. Security risks addressed in this paper include hardware Trojan, reverse engineering, counterfeiting, side-channel attack and unauthorized overproduction. The paper contains a large number of references.

We end this issue with a letter from Gao, Li and Guo of University of Electronic Science and Technology of China, Chengdu, China. The authors describe an experimental study on the effects of high-energy microwave field (10^5 V/m) on Indium Phosphide (InP). The observed nonlinear behavior is supported by theoretical analysis.

The next issue of *JETTA*, to appear in June 2018, will feature testing of analog, mixed-signal and RF devices.

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