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Editorial

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I am pleased to announce the 2016 JETTA-TTTC Best Paper Award. We congratulate the winning authors, Masahiro Ishida, Toru Nakura, Takashi Kusaka, Satoshi Komatsu and Kunihiro Asada, for their paper "Dynamic Power Integrity Control of ATE for Eliminating Overkills and Underkills in Device Testing," that appeared in *Journal of Electronic Testing: Theory and Applications,* Volume 32, Number 3, pp. 257–271, June 2016. More details follow next to this editorial.

The award selection had two phases. In the first phase, the editorial board examined all papers of volume 32. Then, starting from their recommendations, an awards committee, appointed by the Test Technology Technical Council (TTTC), consisting of Salvador Mir (Chair), Vishwani Agrawal, Nicola Nicolici, Adit Singh and Xiaoqing Wen, selected the winner. The award was presented on November 2, 2017 in Fort Worth, Texas, USA during a plenary session of the International Test Conference. The adjoining photograph shows (left to right) Takashi Kusaka, Toru Nakura and Masahiro Ishida receiving award certificates on behalf of all authors from Yervant Zorian, TTTC President and JETTA Editor.

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Peer reviewing is an essential part of *JETTA*'s editorial policy. We acknowledge the contributions of our reviewers and thank them for devoting their expertise and time to serve the profession. A list of those who completed reviews for *JETTA* in 2016 and 2017 appears in this issue.

This issue contains seven articles. The topics discussed are mixed-signal test and diagnosis, reliability, electromagnetic interference, automatic test pattern generation (ATPG), single event upset (SEU) and FPGA testing. The third and fifth papers were initially presented at the Eighteenth Latin American

Test Symposium, Bogota, Columbia, during March 13–15, 2017 and subsequently rewritten by authors for journal publication. *JETTA* Editor Leticia M. B. Poehls supervised their peer reviews.

We begin with two papers on mixed-signal testing. The first paper introduces *kernel entropy component analysis* (KECA) that facilitates the diagnosis of analog circuits. Additionally, *extreme learning machine* (ELM) is used in this work. Contributors are Z. Yuan, He, L. Yuan and Cheng from Hefei University of Technology, Hefei, China.

In the next paper, Duan of Intel, San Jose, CA, USA and Chen of Iowa State University, Ames, IA, USA examine the inaccuracy in the INL estimation for an ADC by previously published uSMILE (ultrafast segmented model identification of linearity error) algorithm. The source of inaccuracy is traced to quantization noise and the proposed improvement is achieved by adding a dither signal to the test input ramp of the ADC.

The third paper of this issue addresses the reliability problem of CMOS devices. The idea is to identify signal paths that are most likely to slow down with long usage. Delay tests for these paths would provide a reasonable measure for assessing the age as well as the remaining useful lifetime of the device. The authors are Srivastava and V. Singh from Indian Institute of Technology Bombay, Mumbai, India, A. D. Singh from Auburn University, Auburn, AL, USA and Saluja from University of Wisconsin, Madison, WI, USA.

The forth paper deals with electromagnetic interference (EMI). For packages or printed circuit boards consisting of analog, digital and RF components, assessment of EMI is significant. In this paper, near field measurement at locations as close as one-sixth of a wavelength from radiating sources is discussed. Authors Tian, Li, Liu, Wan and Cao are from Chinese Academy of Sciences, Beijing, China and National Center for Advanced Packaging, Wuxi, China.

The fifth paper revisits one of the most important problems in testing, i.e., automatic test pattern generation (ATPG). A Boolean satisfiability (SAT) framework is used for a solution by encoding operations such as backward and forward implications into SAT formulas. Stuck-at and transition delay faults are considered and tests are generated for detection as well as diagnosis. Authors are Raiola, Burchard, Neubauer and Becker from University of Freiburg, Germany, and Erb from Infineon Technologies AG, Neubiberg, Germany.

The sixth article is a Letter contributed by Yi, Liu and Yang from Xidian University, Xi'an, China. Authors present an analytical model of a semiconductor PN junction that allows an efficient and accurate characterization of a MOSFET in the presence of single event transients (SET).

The seventh article, also a Letter, is contributed by Wang, Ma and Xu from China Aerodynamics Research and Development Center, Mianyang Sichuan, China, and Rui from Chongqing Communication College, Chongqing, China. The objective here is to test the resistivity of solder joints associated with a field programmable gate array (FPGA). The presented technique deals with limited availability of pins and reduces the amount of energy used by the test.

JETTA Editorial Board held its annual meeting at Fort Worth, Texas on November 1, 2017. The photograph taken at the meeting shows attending editors and invited guests (standing left to right) Haralampos Stratigopoulos, Chen-Huan Chiang (TTTC Chair), Xiaowei Li, Cheng-Wen Wu, Stephen Sunter, Krishnendu Chakrabarty, Shawn Blanton, Charles Glaser (Editorial Director, Springer), Toru Nakura (Awardee), Naoki Tarao (Guest), Takashi Kusaka (Awardee), Ozgur Sinanoglu, (sitting left to right) Rubin Parekhji, Vishwani Agrawal, Enamul Amyeen, Kuen-Jong Lee, Masahiro Ishida (Awardee) and Hans Manhaeve.