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Editorial

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This issue contains eleven articles, including one letter. The topics discussed are hardware Trojan, system-on-chip test, mixed-signal test, verification, fault tolerance, error resilience, interconnect testing, technology dependent faults, and built-in self-test for FPGA.

The first paper presents a novel technique for detecting a Trojan circuit hidden within a large circuit. The authors, Bazzazi, Shalmani and Hemmatyar of Sharif University of Technology, Tehran, Iran, show that a logical function of suitably selected node signals can effectively identify the presence of the Trojan circuitry.

A modern system-on-chip (SoC) may contain sensors for monitoring temperature, process, noise, aging, skew, jitter, etc. Often, test and other modes must access these sensors. The paper by He and Tehranipoor of University of Florida, Gainesville, Florida, USA proposes a new sensor access mechanism (SAM) consisting of a JTAG interface, clock selection circuit and a wrapper.

In the third paper, Yang and Tian of University of Electronic Science and Technology of China (UESTC), Chengdu, China and Chen of Chengdu College, UESTC, Chengdu, China give an algorithm for selecting a minimal set of tests to attain a target fault detection rate (FDR) in an analog circuit. Their FDR refers to the percentage of modules or fault sources that are covered by tests.

The topic of the fourth paper is verification of a digital circuit design. Typical high-level metrics, such as code coverage, branch coverage or other models that depend on the stage of the design, are used. The authors, Martinez-Cruz, Barrón-Fernández, Molina-Lozano, Ramírez-Salinas, Villa-Vargas and Cortés-Antonio of National Polytechnic Institute (IPN), Mexico City, Mexico and Cheng of University of California, Santa Barbara, California, USA, call their procedure for generating digital tests as binary particle swarm optimization algorithm with re-initialization mechanism (BPSOr).

Next, we have three papers on fault tolerance and error resilience. The first among these responds to a concern often cited with near or below threshold operation of CMOS circuits. Low voltage operation reduces energy consumption but raises susceptibility to noise. Asli and Taghipour of University of Guilan, Rasht, Iran present their design of a soft error resilient SRAM cell in the 20 nm FinFET technology. In the second paper, Gutierrez, Tenentes and Kazmierski of University of Southampton, UK, and Rossi of University of Westminster, UK examine masking of errors by logic circuits. They find that error masking is unlikely for certain patterns and then develop an ingenious way to selectively use triple modular redundancy (TMR) on workloads containing those patterns. The third paper gives a novel design of a multiplier that intentionally compromises full accuracy in favor of energy efficiency by allowing errors only in lower order output bits. This design, contributed by Garg and Sharma of Indian Institute of Information Technology and Management, Gwalior, India, reduces the number of gates and node capacitances over previous work yet shows no degradation in the filtered image of Lena.

The eighth and ninth papers deal with interconnect test. First, Shang, Sun, Li and Ma of Guilin University of Electronic Technology, Guilin, China devise tests for interconnects on high-speed printed circuit boards (PCB) with mechanical defects. Then, Aghaei and Reshadi of Islamic Azad University, Tehran, Iran and Khademzadeh and Badie of Telecommunication Research Center, Tehran, Iran propose

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on-line but non-concurrent built-in self-test for data links of a network-on-chip (NoC).

The tenth paper gives a study of bridging defects in bulk, fully depleted silicon on insulator (FDSOI) and FinFET technologies. For FDSOI devices, variations in body bias voltage and threshold voltage are examined. The authors, Karel, Comte, Galliere, Azaïs and Renovell of Laboratory of Informatics, Robotics and Microelectronics of Montpellier (LIRMM), University of Montpellier, Montpellier, France, compare various technologies and draw useful conclusions.

Finally, in a *JETTA* Letter, Palchaudhuri and Dhar from Indian Institute of Technology, Kharagpur, India address the problem of locating a fault causing hard or soft errors in a field programmable gate array (FPGA) device.