J Electron Test (2016) 32:399
DOI 10.1007/s10836-016-5609-x

Editorial

Vishwani D. Agrawal[1]

Received: 12 July 2016 / Accepted: 12 July 2016 / Published online: 20 July 2016

In October 2012, we published a special issue on mixed-signal test (*JETTA*, volume 28, number 5). Now, four years later, we return to that theme. Several of the industry trends have moved forward. The system-on-chip (SoC) devices are integrating more radio frequency (RF) stuff. The ability to integrate is enhanced with 3D-stacking. As a result, concerns about test time and yield enhancement have deepened.

In this issue these concerns are addressed by papers on built-in self-test (BiST), production test, reliability, debugging and machine learning techniques.

Planning for this special issue began soon after the 20th *International Mixed-Signal Testing Workshop* (*IMSTW* 2015), held in Paris, France during June 24–26, 2015, We issued a call for papers and all submissions went through the journal's peer review process that selected those appearing here. We are grateful to guest editors, Gildas Léger and Carsten Wegener, for organizing this effort and carrying it to completion. Their Guest Editorial gives a summary of the contents. As this issue goes to press, *IMSTW* 2016, the 21st workshop in the series is just being completed in Catalunya, Spain. This time, instead of waiting for four years, you may look forward to our next special issue on mixed-signal test in 2017.

✉ Vishwani D. Agrawal
vagrawal@eng.auburn.edu

[1] Department of ECE, Auburn University, 200 Broun Hall, Auburn, AL 36849, USA