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A Jitter Injection Signal Generation and Extraction System for Embedded Test of High-Speed Data I/O

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Abstract An instrument for on-chip measurement of transceiver transmission capability is described that is fully realizable in CMOS technology and embeddable within an SoC. The instrument can be used to inject and extract the timing and voltage information associated with signals in high-speed transceiver circuits that are commonly found in data communication applications. At the core of this work is the use of ΣΔ amplitude- and phase-encoding techniques to generate both the voltage and timing (phase) references, or strobes used for high-speed sampling. The same technique is also used for generating the test stimulant for the device-under-test.

Keywords High-speed I/O test · Analog test · Mixed-signal test · Design-for-test · BIST · Sigma-delta bit streams

1 Introduction

Transceiver circuits find a multitude of uses in cheap, widely-held data communications applications such as smart phones, tablets, cloud computing, etc. In order to keep component costs down, low-cost test techniques are essential. One strategy is to incorporate test circuits directly on-chip to standardize test equipment access, improve accuracy and repeatability, and to contribute to short test times through parallel test procedures. In some cases, an on-chip instrument may be the only means to capture information associated with some internal core circuit. An important attribute of such on-chip test circuits is a low silicon area overhead. In addition, such on-chip instruments are not bandwidth limited by the test channel, so tests can be performed at the desired operating frequencies and speeds [7]. A software programmable, probabilistic test instrument using ΣΔ-encoded phase/amplitude-signal generators is to be described in this paper.

This work in a shorter form was first presented at the 20th International Mixed-Signal Testing Workshop [14]. In that publication the general concept of the probabilistic instrument was proposed and demonstrated with discrete components. In this publication, our first attempt at integrating the concept into a 130 nm CMOS IC realization. The results of this endeavor will also be described here. While our intent is to use this instrument as part of an embedded instrument for high-speed transceivers, however, at this point in time, the IC results do not operate anywhere close to the 1 Gbps rates required by today's I/Os. This is not meant to be a definitive statement that the approach is not sound but rather the results gather here is a testament of the working principle. It is expected that future work will improve the operating speed and measurement resolution suitable for next generation transceiver ICs.

This paper will begin with a system overview of the probabilistic test instrument (PTI) in Section II, including a description of various methods for phase and voltage signal generation using sigma-delta encoding methods, and CDF extraction. Section III will describe the critical decision-making circuits such as the D-type flip-flops and comparator circuits used in the CMOS IC implementation. Section IV will describe the

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working principle of the PTI and its two main modes of instrument operation. Section V will simulate some practical examples using the PTI. Experimental results for both a discrete and CMOS IC implementations will be provided in Section VI. Finally, conclusions will be drawn in Section VII.

2 System overview

A probabilistic test instrument is proposed and implemented in this paper for transceiver testing. It consists of two main parts: (1) multi-channel programmable bit-stream generator, and (2) a probability extraction unit. Figure 1 shows the system architecture of this test instrument. On the top left-hand side of this figure is the data signal generation blocks used for stimulating a DUT with a pre-defined test pattern, such as a pseudo-random bit sequence (PRBS). The data pattern is held in a 1-bit circular memory and routed to a single flip-flop. This signal generator will be denoted as channel 1. Right below this in channel 2 is another set of blocks that are used to define the timing of the edges of the incoming data stream denoted T_{Data}. This allows for arbitrary test signals (e.g., jitter) to be introduced on the edges of the incoming data stream. The timing of the edge T_{Data} is produced through a phase-modulating encoding process performed in software using a ΣΔ modulator and a digital-to-time converter (DTC), followed by storage in a 1-bit circular memory. The output of this memory is then passed to a time-mode filter (TMF) realized using either a PLL [4], a DLL [6] or time-mode SC reconstruction filter [1] – more on this in a moment. In a similar vein, both the level crossing of a sampling process and timing edge denoted by parameters V_{TH} and T_{STRB} are realized using the bottom two sets of sub-blocks in channels 3 and 4. While T_{STRB} is realized using a phase-modulated ΣΔ encoding process followed by a TMF, V_{TH} is created using a voltage-sensitive ΣΔ encoding process followed by an amplitude-mode filter (AMF), which could be RC in nature. Through the appropriate encoding, both T_{STRB} and V_{TH} can be independently controlled, as illustrated in Fig. 2, to establish the sampling point in the voltage vs. time space using a voltage-based comparator [11]. The second part of this test instrument is the probability extraction unit (PEU). The PEU is used to extract the statistical information associated with the DUT output through the application of two sets of counters, N and N_{Total}.

2.1 ΔΣ-Encoding Signal Generation Methods

Sigma-delta modulation is used to encode a bandwidth-limited signal into a 1-bit digital sequence. Although the schematics show a sigma-delta modulation sequence as being applied directly to the input of an analog circuit, each pulse of this sequence must be reconstructed in both time and amplitude. In other words, each pulse goes through a zero-order hold operation. This zero-order hold operation is the role of the 1-bit digital-to-analog (DAC) or digital-to-time (DTC) blocks that follows the sigma-delta encoding process. As a 1-bit signal is a poor approximation of any real-valued signal with almost-infinite precision, a quantization error results. To minimize the effect of this quantization error, ΔΣ encoding shifts the quantization error to an out-of-band frequency region where it can be filtered out using a frequency-sensitive filter and recovers most of the original signal.

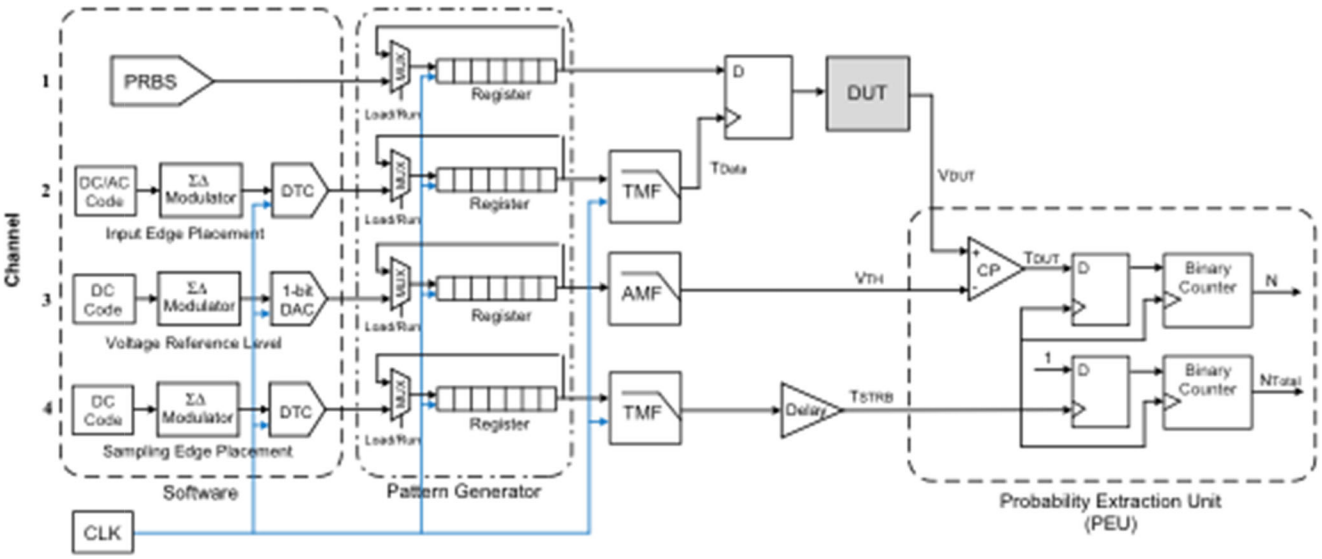

Fig. 1 System architecture of the proposed probabilistic test instrument

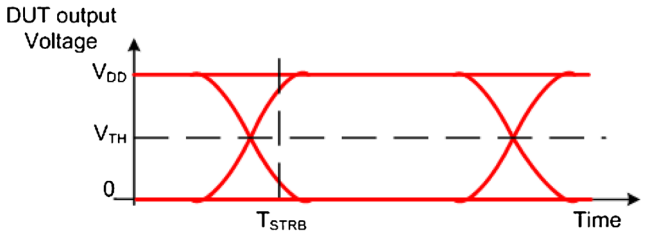

Fig. 2 Illustrating the sampling point with respect to V_{TH} and T_{STRB}

An important aspect of ΔΣ-encoding is that it is not limited to voltage or amplitude levels, as seen along the y-axis in Fig. 2, but can also be used to encode the signal information along the time-axis. These two insights are used as the basis of the signal generator used in the instrument proposed here. Let us consider these two aspects.

2.1.1 Continuous-Time Voltage Signal Generation

N-bits of a band-limited digital signal that is ΔΣ encoded can be indefinitely rotated, converted into a corresponding voltage level (e.g., V_{SS} and V_{DD}) and applied to a voltage-sensitive analog frequency-selective reconstruction filter as depicted in Fig. 3. The filter would remove the out-of-band quantization noise and convert the digital signal into a corresponding continuous-time voltage signal. As this method of signal generation has been well studied and published widely, we refer our readers to [9] for further details.

2.1.2 Continuous-Time Phase Signal Generation

N-bits of a band-limited digital signal that is ΔΣ encoded can be indefinitely rotated, converted into a corresponding phase level (e.g., φ_{MIN} and φ_{MAX} degrees) and applied to a phase-sensitive frequency-selective reconstruction filter as depicted Fig. 4. The filter would remove the out-of-band quantization noise and convert the digital signal into a corresponding continuous-time phase signal. These types of filters are less familiar to most, so we'll spend some time discussing them here. At this time, the authors know of three different ways to implement a phase-sensitive frequency-selective filter circuit: (i) phase-locked loop, (ii) delay-locked loop and (iii) time-mode filter circuit. The genesis of this circuit principle was first described in [16, 17].

(i). Phase-Locked Loop (PLL):

A PLL is a basic element of electronics and is used in many different ways such as jitter suppression, clock synchronization, etc. A PLL can also be used as a phase-sensitive frequency-selective reconstruction filter [17]. A block diagram of PLL is shown in Fig. 5. In the feedforward path of the PLL is a phase-detector, loop filter with transfer function F(s) and a voltage-controlled frequency oscillator. In the feedback path, a divide by N_{PLL} frequency divider block can be seen. By selecting the appropriate loop-filter F(s), frequency-divider ration N_{PLL}, the input-output phase transfer function Θ_o/Θ_i can be adjusted so that the desired frequency response is achieved. This principle was first used to generate test signals for evaluating the frequency response behavior of PLLs [17] and further expanded to high-order PLL design in [5].

(ii). Delay-Locked Loop (DLL):

In much the same manner as the PLL, a type-II DLL shown Fig. 6 can also be used as a time-mode reconstruction filter circuit. Here the DLL consist of a phase-detector front-end, a loop filter with transfer function F(s) and a delay-line driven by a reference clock signal. The first application of a 1st-order DLL as a reconstruction filter can be traced back to [13]. In [6], the application of high-order DLLs as an adjustable frequency-selective reconstruction filter was introduced.

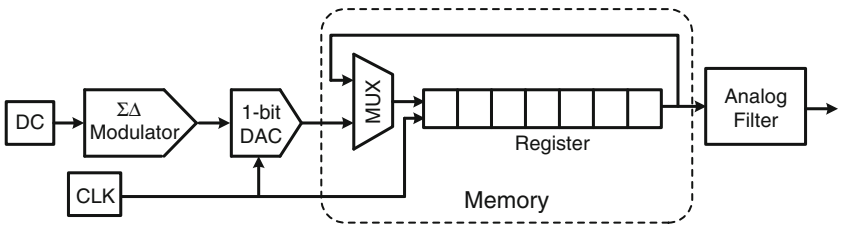

Fig. 3 Synthesizing a continuous-time voltage signal using a circular ΣΔ-delta encoded bit-stream, a digital-to-analog converter and a frequency-selective analog filter circuit

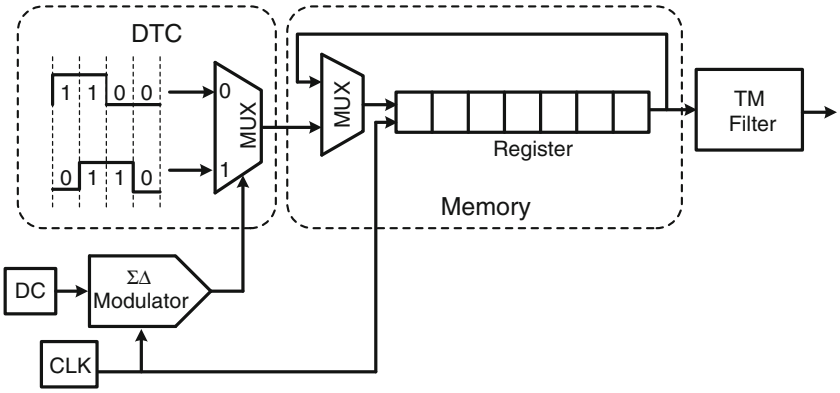

Fig. 4 Synthesizing a phase-modulated signal using a circular ΣΔ-delta encoded bit-stream, a digital-to-time converter and a phase-sensitive frequency-selective filter circuit

(iii). Time-Mode (TM) SC Filter:

Another method that one could use to realize a phase-sensitive frequency-selective filter is the time-mode resonator circuit shown in Fig. 7. This design is very different from a PLL or DLL implementation as it relies on the manipulation of several phase signals using several feedback loops [1]. In this implementation the realization uses several voltage-controlled delay lines and several switched-capacitor phase-to-voltage conversion circuits. This particular area of filter design is rapidly developing and one can expect more area efficient realizations in the very near future.

In general, the IC area required to implement the TMF may be considered excessive in many cases. However, as PLLs and DLLs are blocks commonly found on an IC, a better approach is to time-multiplex these resources as part of the TMF. Alternatively, the TMF could be implemented on the load-board of the device interface board of the ATE. While this degrades the fully integrated approach it does provide greater flexibility in the selection the TMF characteristics thereby optimizing the signal generator performance levels.

2.2 Jitter Injection System/Timing Strobes

The right-hand side of Fig. 1 shows the architecture of the multi-channel programmable bit-stream generator (BSG). It consists mainly of three modules. A software programmable bit generator, a pattern generator and a hardware implementation of a filter bank consisting of voltage-sensitive and phase-sensitive or TM filters. A multiplexing circuit consisting of a D-type flip-flop is also included for re-timing purposes.

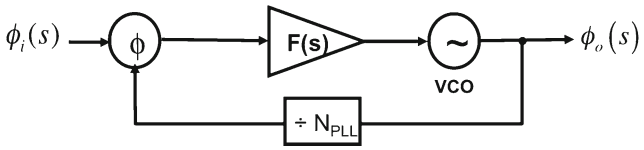

Fig. 5 – A block diagram of a PLL acting as phase-sensitive or time-mode reconstruction filter

Collectively, these circuits realize a pattern signal generator whose phase is controlled by an independent source as depicted in Fig. 8(a).

The BSG has 4 channels: Channel 1 of the programmable BSG is used for stimulating a DUT with a pre-defined test pattern such as a pseudo random bit sequence (PRBS). The data pattern is held in a 1-bit circular memory and routed to the D-input of the flip-flop. Right below this is channel 2, where another set of blocks are used to define the timing of the edges of the incoming data stream, denoted as T_{Data}. This allows for arbitrary test signals (e.g., jitter) to be introduced on the edges of the incoming data stream. The timing of the edge T_{Data} is produced through a phase-modulating encoding process performed in software using a ΣΔ modulator and a digital-to- time converter (DTC), followed by storage in a 1-bit circular memory. The output of this memory is then passed to a time-mode filter (TMF) realized using either a PLL, DLL or time-mode reconstruction filter, as described in Section III. The phase-encoded signal is then passed to the clock input of the D-type flip-flop. Together, channel 1 and 2 produce an arbitrary digital pattern with various edge timings for exercising the DUT.

Channel 3 generates a threshold voltage (V_{TH}) whose level is programmable in software. It consists of a ΣΔ modulator, a 1-bit DAC followed by a 1-bit circular memory. The output is passed through a voltage-mode filter (VMF), which is implemented by some active-RC circuit. Similarly, channel 4 generates the timing strobes (T_{STRB}) associated with a sampling process. Both V_{TH} and T_{STRB} are depicted by the horizontal and vertical dashed lines shown in Fig. 2 depicting the

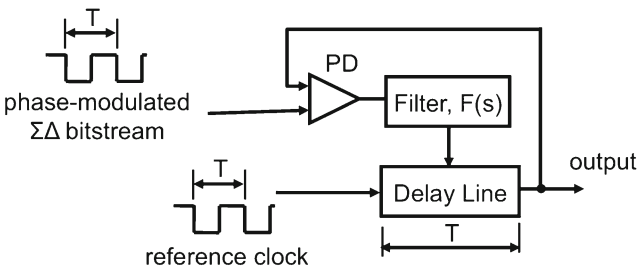

Fig. 6 – A block diagram of a type-II DLL acting as phase-sensitive reconstruction filter

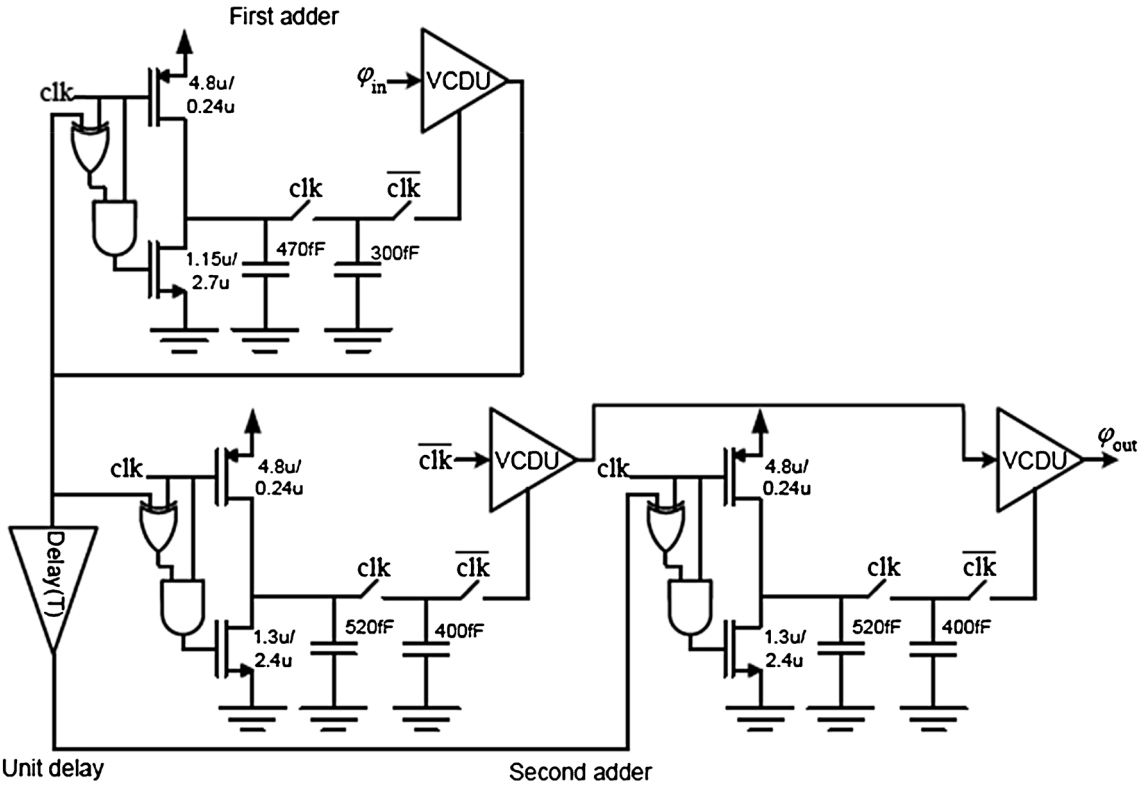

Fig. 7 – A 1st-order time-mode reconstruction filter circuit using switched-capacitor circuits

sampling process. The T_{STRB} is generated using the ΣΔ phase signal generation technique, in much the same way as described for the jittered clocked signal of channel 2. These two strobes (V_{TH} and T_{STRB}) will be used by the probability extraction unit to extract the CDF associated with the DUT output. Through the appropriate encoding, both T_{STRB} and V_{TH} can be independently controlled to establish the sampling point in the voltage vs. time space using a voltage-based comparator.

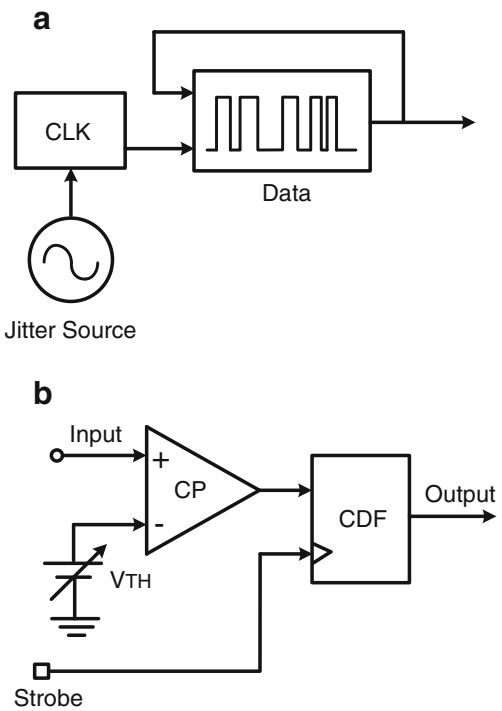

Fig. 8 Illustrating the functional behavior of: (**a**) pattern signal generator and (**b**) PE extraction unit

2.3 Probability Extraction Unit (PEU)

A block diagram of the PEU unit developed in this work is illustrated in Fig. 9. It is based on the work found in [8] but has much earlier roots, such as that related to multichannel analyzers [10]. The PEU consists of four main blocks: (1) voltage-

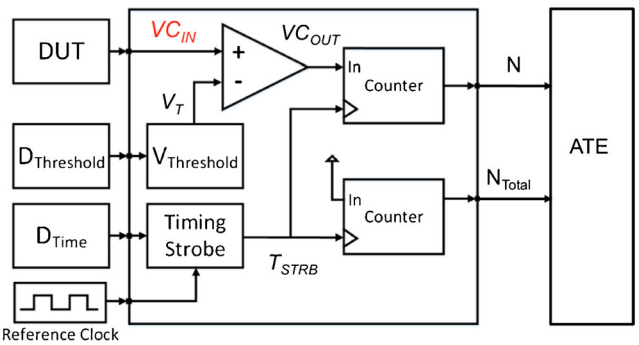

Fig. 9 - Architecture of the probability extraction unit (PEU)

sensitive comparator, (2) a bank of two counters, (3) a voltage threshold generator, and (4) an edge timing strobe generator.

The comparator compares the output DUT edge with respect to the threshold voltage value and sets the output to a logic "1" state if the DUT output is above the threshold or a logic "0" state otherwise. The second block in the PEU is the counter block. Two 16-bit counters will count the logic value presented to it at the time instant set by the timing strobe generator. One counter, attached to the output of the comparator, will count the number of rising edge transitions from the DUT that are ahead of the timing strobe T_{STRB} (whose count value is denoted by N), and the second counter will count the total number of timing strobe rising edge transitions (whose count value is denoted as N_{Total}). Using the output values of these two counters over a range of timing strobe locations; it is possible to extract the DUT output cumulative density function (CDF) as a function of the strobe time T_{STRB}, i.e.,

$$CDF(T_{STRB}) = P(V_{DUT} < V_{TH}) = 1 - \frac{N(T_{STRB})}{N_{Total}} \qquad (1)$$

The third block is a digitally controllable voltage threshold generator. This circuit is used to set the threshold level for the comparator V_{TH}. The forth block is a digitally controllable timing strobe generator used to set the sampling instant of each counter, T_{STRB}. A simple drawing to capture the nature of the extraction unit is shown in Fig. 8(b).

The operation of the PEU can be seen in Fig. 10. Here an incoming signal is compared against two different threshold levels at the moment of the rising edge of the timing strobe signal. The comparator output is then presented to a 16-bit counter which increments its stored value N at the moment the rising edge of the timing strobe occurs. On completion of N_{Total} iterations per timing strobe, the CDF value for that edge time can be deduced according to Eq. (1).

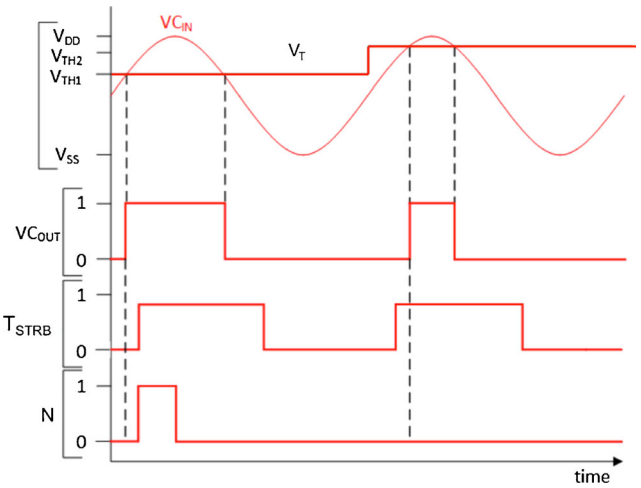

Fig. 10 – Illustrating the working principle of the PEU on a dynamic signal being compared against two different threshold values

3 Circutis Details For Critical Decision-Making Elements

In this section a descriptions of the critical decision-making circuits will be described. Other than the time-mode reconstruction filter circuit, the only other elements that make up the PTI are D-type flip-flops and a comparator circuit.

3.1 D-Type Flip-Flops

The performance of the PEU is highly dependent on the performance of the D-type flip-flop. It is desired to have a flip-flop with a very low setup time. The rising edge triggered D-type flip-flop can be implemented in various ways; one of the implementation is an edge-triggered flip-flop using two level sensitive latches in cascade [12] as shown in Fig. 11. First stage is often called the master stage and the second stage is called the slave stage.

When the clock denoted by Clk is low, the transmission gate T1 and T4 are on and T3, T4 are off. The D input flows through to point A and as well as it's complemented at point B. When the clock goes high, T1 and T4 shut off, while T2 and T3 turn on. This causes the value of the B node to be passed to the Q output in inverted format. At the same time, the B node value is passed back onto itself, thereby holding its value constant. When the clock goes back low, T1 and T4 turn on. The value of D on the Q output is then circulated around the two inverter of the slave section back onto itself. When the clock returns to the high state, the Q output can then take on a new logic value, depending on the D input. The complementary output of Q is also available at the output of the inverter section of the slave stage.

3.2 Comparator

The comparator used in the PEU compares the DUT output signal with a reference threshold voltage V_{TH}, which is varied with time during a measurement cycle. At the appropriate sampling instant, the DUT output signal is compared to the reference threshold V_{TH}, if greater the output will be set to a logic high level. Conversely, when the DUT output voltage is lower than V_{TH} the output will be set low. An op-amp with a latch can be used as a comparator but is limited to low frequency applications. The most important parameter for a comparator design is its input sensitivity (i.e. increases the minimum input signal with which comparator can make a decision) and its propagation delay [12]. It is desirable for our application to have a comparator with a small propagation delay but one with a high sensitivity. A comparator generally consists of a preamplifier and a decision circuit involving a positive feedback loop. The preamplifier is used to amplify the input signal to improve the comparator sensitivity.

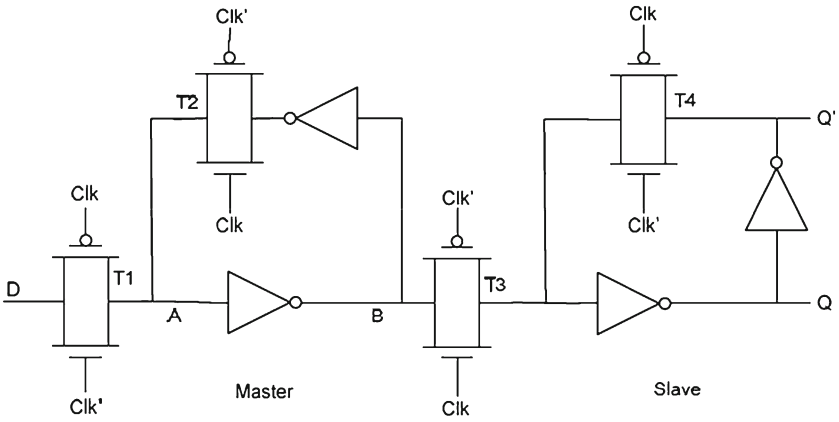

Fig. 11 – Edge-trigger master-slave D-type flip-flop circuit

It also isolates the input of the comparator from switching noise, often called kickback noise coming from the positive feedback stage, when the decision circuit switches state [12]. The decision circuit determines which of the input signals is greatest. An implementation of the comparator is shown in Fig. 12.

4 Working Instrument Principle

The proposed test instrument has two main modes of operation. The first mode of operation is for measuring the jitter distribution of a DUT, such as DLL, PLL or clock and data recovery (CDR) unit subject to a known level of input jitter. Such a test setup is used to perform a jitter tolerance test. The second mode of operation is for measuring the input-output excess phase response of a time-sensitive channel of a DUT, commonly referred to as a jitter transfer function test. The working principles for these two modes of operation are discussed below.

4.1 Jitter Tolerance Measurement

In the first mode of operation we can measure the jitter distribution of a DUT such as PLL or DLL subject to some input phase-modulated test stimulus, e.g., perform a jitter tolerance type test. Both the multi-channel programmable BSG and the PEU are used to perform this measurement. In this mode of operation, all four channels of the multi-channel programmable BSG shown in Fig. 1 are used to generate a phase-modulated test signal with a specific PRBS test pattern superimposed. Figure 13(a) illustrate the arrangement of channel 1 and 2 of the multi-channel programmable BSG, together with the input software setup for generating the Gaussian test signal. A Gaussian noise source is low-pass filtered to band-limit the wideband noise from the random number generator (RN). This signal (consisting of real numbers) is then encoded into a one-bit sequence using a ΣΔ modulator. Subsequently, the output of the ΣΔ modulator is phase modulated using the DTC and low-pass filter in the time-domain using a TMF. The output of the TMF is a Gaussian-shaped phased-modulated clock signal denoted by T_{Data}.

Once the DUT is stimulated by the phase-modulated signal, its output is passed to the PEU for the output signal characterization as described in Section V. The threshold voltage V_{TH} and T_{STRB} inputs to the PEU are set by channels 3 and 4 of the multi-channel programmable BSG. For a jitter tolerance test, V_{TH} is held constant throughout the entire test.

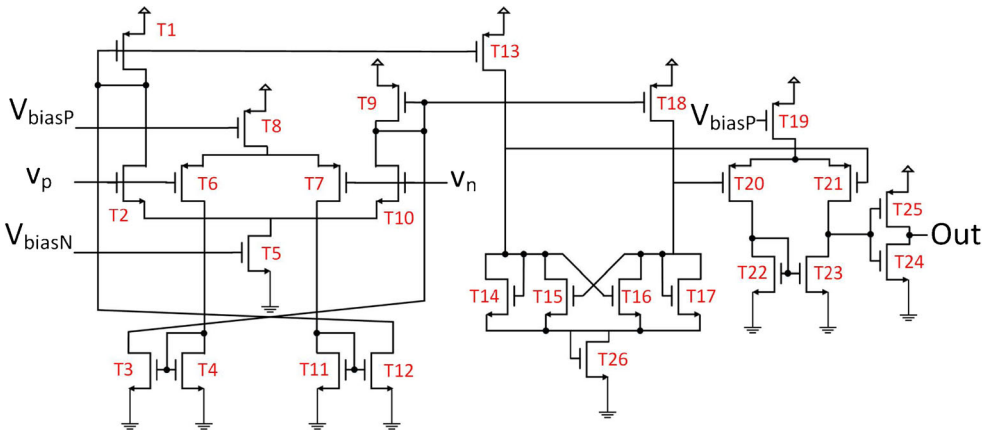

Fig. 12 – Illustrating the working principle of the PEU on a dynamic signal being compared against two different threshold values

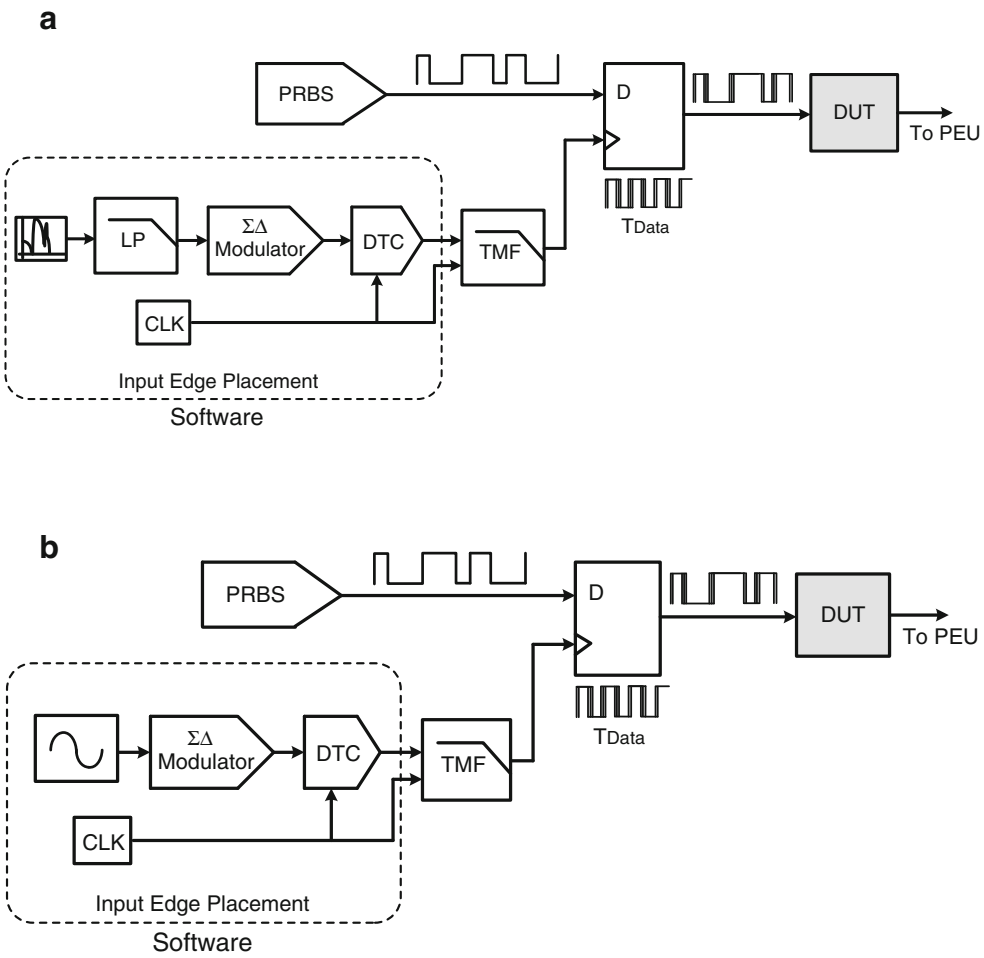

Fig. 13 System setup for performing a jitter tolerance test. A PRBS sequence whose clock signal is: (**a**) phase-modulated with a Gaussian distribution signal for a jitter tolerance test, and (**b**) phase-modulated with a sinusoidal signal for characterizing the phase response of a time-sensitive channel

4.2 Input-Output Phase Transfer Measurement

In the second mode of operation the input-output phase transfer function of a DUT of a time-sensitive channel can be measured. This is performed by exciting the DUT with a 0–1 cyclic bit pattern whose clock is phase-modulated by a sine wave of a specific amplitude, phase and frequency and measuring the amplitude of the output sinusoidal phase response of the DUT. The ratio of the output phase amplitude to the input phase amplitude provides a measure of the system gain at a specific frequency. Repeating this test over a wide range of frequencies provides a measure of the input-output phase transfer for this DUT. In this test mode, all channels of the multi-channel programmable BSG of Fig. 1 are used. Further, a sine wave of known amplitude, phase and frequency is synthesized through channel 2 as opposed to a Gaussian noise signal in the previous test setup.

Figure 13(b) illustrates the test set up for a phase transfer function test. As shown in this figure, a sine wave of known amplitude, phase and frequency is encoded using the ΣΔ modulator and then phase modulated by a DTC. The phase-modulated signal is then low pass filtered using a TMF. The output of the time mode filter is essentially a clock signal with sine wave modulating its phase, as depicted in Fig. 14. This signal

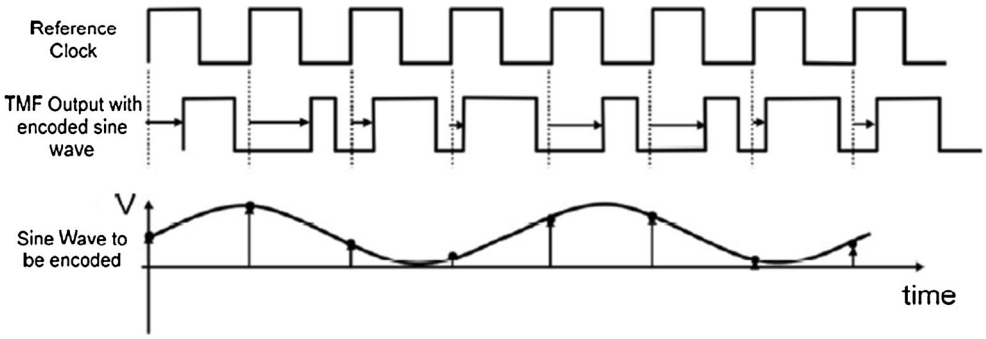

Fig. 14 Illustrating how a sinusoidal signal is incorporated into the phase of a modulated clock signal

is then used to modulate the 01 cyclic pattern from the PRBS generator. This signal is essentially a clock signal whose phase varies according to a sine wave and it will be used as the test stimulus for the DUT. The output of the DUT is then sent to the PEU for signal characterization. Both the threshold voltage V_{TH} and T_{STRB} inputs to the PEU are set by channels 3 and 4 of the multi-channel programmable BSG, identical to that described in the previous test setup.

Once the CDF is derived using the PEU, the amplitude of the output phase signal is then determined by determining the upper and lower limits of the CDF. Normalizing the output amplitude by the input amplitude provides a measure of the gain of the DUT at a particular input frequency. Repeating for different input frequencies provides a measure of the phase transfer as a function of frequency.

4.3 Test Time

A simple estimate of the test time to complete a full characterization of the transceiver operating at a bit rate F_B would be given by

$$\text{Characterization Test Time} = \left(\frac{\phi_{max}-\phi_{min}}{\Delta\phi}\right)\cdot\left(\frac{N_{\text{Total}}}{F_B} + \text{Data Transfer Time}\right) \quad (2)$$

where N_{Total} is the number of points collected for a single CDF point and $(\phi_{MAX} - \phi_{MIN})/\Delta\phi$ is the total number of CDF points collected during the test. Here $\phi_{MAX} - \phi_{MIN}$ represents the input full-scale range of the transceiver and $\Delta\phi$ is the desired resolution of the test. As some time is necessary to transfer the each point of the CDF to the ATE, this is included in the test time as a parameter *Data Transfer Time*.

For a production test, such as one that wanted to verify that the noise level is less than some threshold, then a two CDF points is all that is required, one at the 25 % quartile and the other at 75 % quartile, from which the robust mean and standard deviation [15] can be derived. Thus, the test time reduces to

$$]\text{Production Test Time} = 2\cdot\left(\frac{N_{\text{Total}}}{F_B} + \text{Data Transfer Time}\right) \quad (3)$$

4.4 System Calibration

Any instrument added into the test sequence must undergo a focused calibration process. The approach most familiar to the test engineer is to make use of the digitizer in the ATE to characterize the phase-modulated signal produced by the sigma-delta signal generator. This characterization signature would then be compared to that produced by the PEU from which a set of calibration factors would be generated. This process would be repeated over frequency so that a set of frequency-dependent calibration factors could be derived. A more detail description of this process is outlined in [5].

5 Simulation Results

In this section we present the MATLAB/Simulink simulated results for the two modes of operation of the proposed probabilistic test instrument (PTI) presented earlier. The DUT for this simulation is modeled as an ideal 6th-order PLL with a bandwidth of 100 kHz [5]. The DUT is assumed noiseless.

5.1 Jitter Tolerance Measurement

A known Gaussian jitter is injected into a DUT and its output is measured using the probability test instrument. Figure 13(a) shows the test setup for this measurement. The time-mode filter (TMF) was implemented using another PLL. A known Gaussian noise was band limited using a low pass Chebyshev filter with a bandwidth of 60 kHz. The band-limited Gaussian noise with a standard deviation of 160 ps was then encoded into a one-bit stream using a 5th-order ΣΔ modulator [3], followed by a 90-degree phase encoding with 50 % duty cycle. The phase-encoded signal was then injected into the DUT. The output of the DUT is then passed to the PEU. The threshold voltage V_{TH} was fixed to be 2.5 V as the output of the DUT swings from 0 V to 5 V. By varying the T_{STRB} from 0 to 45 degrees in steps of 1 degree (corresponding a time change of 1000 ps) we can generate the CDF of the DUT output with the help of the PEU as shown in Fig. 15(a). Differentiating the CDF, the PDF of the DUT output can be derived and compared to the pre-programmed PDF of the input signal as shown in Fig. 15(b). We can see from this figure that the standard deviation of the DUT output measured using the PTI is approximately 160 ps, which is essentially the same as the input level. This is not surprising as the input noise bandwidth was well within the bandwidth of the PLL, and left unaffected by the magnitude roll-off of the PLL.

5.2 Phase-Frequency Response of a Time-Sensitive Channel

The phase response of the DUT was simulated using the test setup shown in Fig. 13(b). The time-mode filter (TMF) was again implemented using a PLL. A sine wave with an amplitude of 0.2 and 0.45 LSB DC offset having frequencies ranging from 10 kHz to 1 MHz are phase encoded using the phase signal generation technique. For each sine wave, a 90° phase encoding with a 50 % duty cycle is used. The phase encoded bit stream is then used to stimulate the DUT and its output is passed to the PEU. The reference threshold voltage V_{TH} of the PEU was fixed at 2.5 V. The timing reference T_{STRB} was varied from 0 to 45 degrees in steps of 1 degree. Taking the ratio of the amplitude of the output to input signals for different input frequencies of the

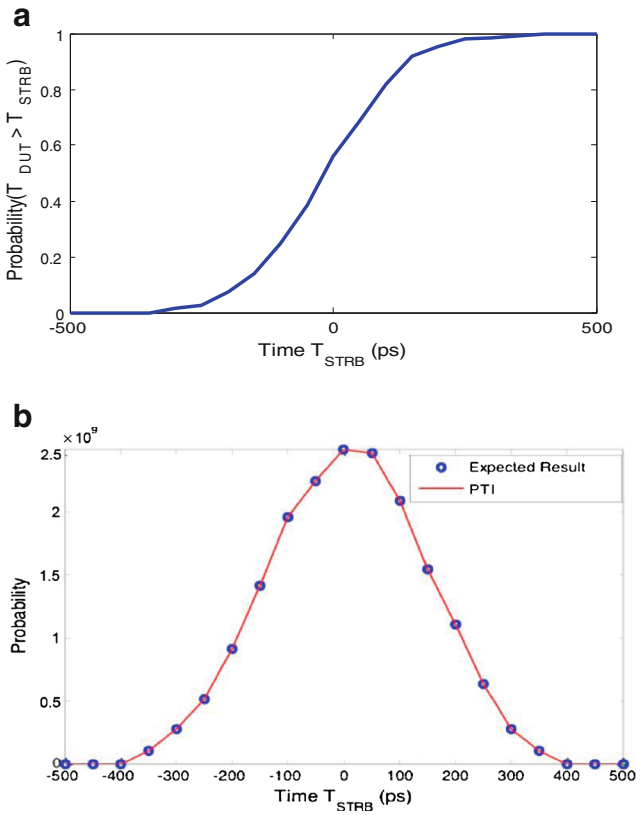

Fig. 15 Simulated behavior of intrinsic noise behavior of a 6th-order PLL: (**a**) extracted CDF of the PLL output timing jitter, and (**b**) mathematically derived output signal PDF vs. input PDF

sine wave results in the excess phase response of the DUT shown in Fig. 16. When compared to the expected PLL response we see that they are in very good agreement.

6 Experimental Results

Two separate implementations of the PTI were constructed. One version was implemented using all discrete components and another involved the use of a PEU constructed in a 130 nm CMOS process. The two implementations provide separate confirmation of the proposed approach.

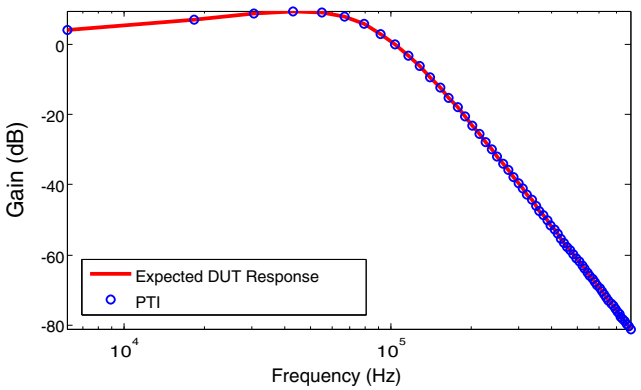

Fig. 16 Simulated frequency response behavior of the time-sensitive channel of the DUT

6.1 Discrete-Implementation of the PTI

The test instrument was prototyped using the configuration shown in Fig. 17 using discrete components. Part (a) illustrates the general block diagram of the test setup and part (b) illustrates the arrangements of the instruments together with the PCB prototype. Here the circular scan-chain registers are loaded with bits derived form a 3rd-order ΣΔ modulator with a noise transfer function having a Butterworth filter function. The bandwidth of the ΣΔ modulator was designed to be 781 kHz with a sampling frequency of 50 MHz. The resulting oversampling ratio (OSR) is set to 32. The DTC was constructed using a 90° phase step with a 50 % duty cycle so that the bit map replaces every 0 bit from the ΣΔ modulator with a 1100 code, and all subsequent 1's by a bit code of 0110 [2]. The DUT was implemented in hardware using a 6th-order PLL designed to approximate a Gaussian filter response. The bandwidth of the PLL was selected to be 300 kHz. The counters were implemented in software. A second-order DLL was used to extract the timing strobe signal from the second circular scan-chain register.

The experimental setup consists of 5 parts: (1) an HP 81130 A pattern generator with two channel outputs, (2) a 6th-order PLL with a 100 kHz bandwidth acting as the DUT, (3) a PCB containing the PEU and a second-order DLL acting as time-mode reconstruction filter (TMF), (4) an oscilloscope, and (5) computer for some signal processing.

The DUT was subject to a repeating 1–0 pattern with a clock jitter set to 160 ps. The corresponding PDF of the DUT output was captured using the PEU and is displayed in Fig. 18. It is also compared to the simulated result found using MATLAB/Simulink. As is evident, the results are quite similar. The RMS jitter had a standard deviation of 170.1 ps as compared to the 160 ps found from simulation.

The phase response of the DUT was also measured using the PTI and an external phase modulated clock source as shown in Fig. 19. We can see from the plot that frequency response of the DUT measured using our instrument has a gain offset. This is because of the limited resolution of the phase signal generator, T_{STRB}. After adding a gain offset we can see from this plot that both tests gives us very similar frequency response. We can see that the bandwidth of the DUT is approximately 100 kHz. For comparison the expected DUT response derived from MATLAB simulation is also provided in the plot of Fig. 19.

6.2 CMOS IC Implementation of the PTI

The PEU portion of the PTI was designed and implemented in IBM CMOS 130 nm technology. The PEU was designed to operate at a clock rate of 114.5 MHz. As previously described,

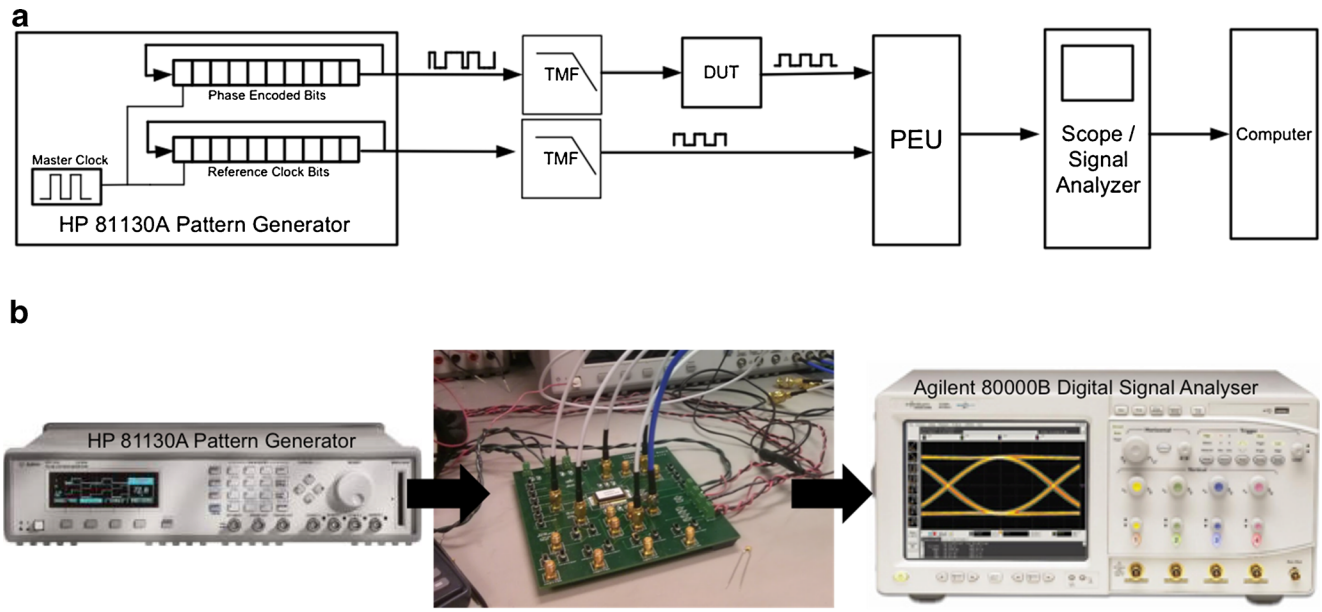

Fig. 17 Measurement test set-up of the discrete implementation of the PTI: (**a**) block diagram, and (**b**) instrumentation set up with PCB prototype

the four main blocks of the PEU are the voltage-sensitive comparator, a bank of two counters, a voltage threshold generator, and an edge timing strobe generator as depicted in Fig. 20. The voltage-sensitive comparator was implemented as a standard two-stage amplifier and the counters were implemented with ripple counters. When the test is completed, the results are stored in the two counters and are serially shifted out and stored in separate off-chip logic registers. In addition, the CMOS chip has a jitter-injector circuit included to act as an on-chip DUT. It is essentially a voltage-controlled delay line as depicted in the top left hand corner of Fig. 20.

A microphotograph of the chip is not shown here, as it is covered with a solid layer of metal. Instead a plot of the Cadence layout is shown in Fig. 21. Here the outline of the various blocks can be seen. The size of the PEU and the timing strobe control circuit is a combined 0.24 mm^2. It should be noted that this particular layout used very area-inefficient D-type flip-flops as part of the circular memory banks. A better approach would be to use a memory array but these were not available to us at the time. On returned from fabrication, the chip was mounted on a custom-built PCB and interfaced to the test equipment for testing purposes in much the same way as illustrated in Fig. 17.

With the DUT implemented in silicon alongside the PEU, the input bit-sequences for the voltage and timing strobe circuits were generated with the HP81130A pattern generator. The reference clock of 114.5 MHz was derived from an external crystal oscillator. Each input bit pattern was a sigma-delta modulated version of the digital inputs, $D_{Threshold}$ and D_{Time}. The digital code $D_{Threshold}$ was kept as a constant, while D_{Time} was varied over its full range. This resulted in the timing strobe being moved across a 90-degree phase range. For each test, the output values of the counters were captured off-chip in external digital registers located in an FPGA. The count cycle begins by setting the first two bits of each counter output

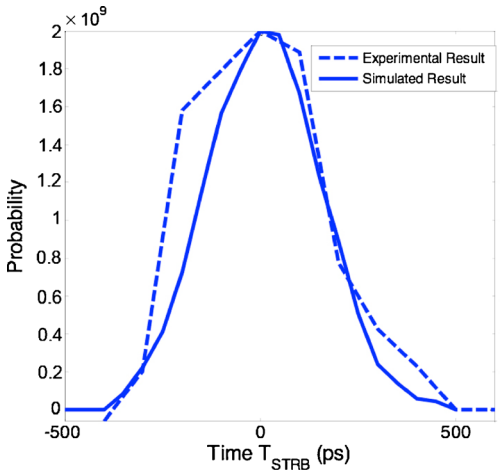

Fig. 18 PDF of test setup as measured with the discrete implementation PTI

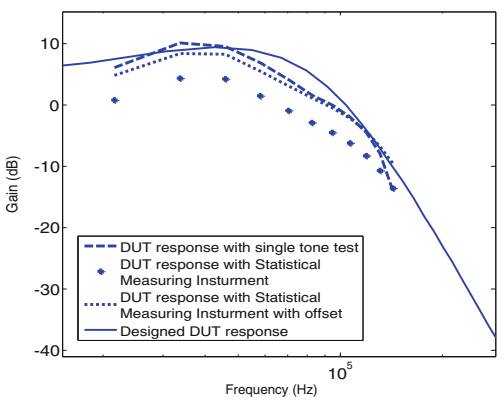

Fig. 19 The measured frequency response behavior of the input phase sensitive DUT as extracted by the discrete implementation PTI

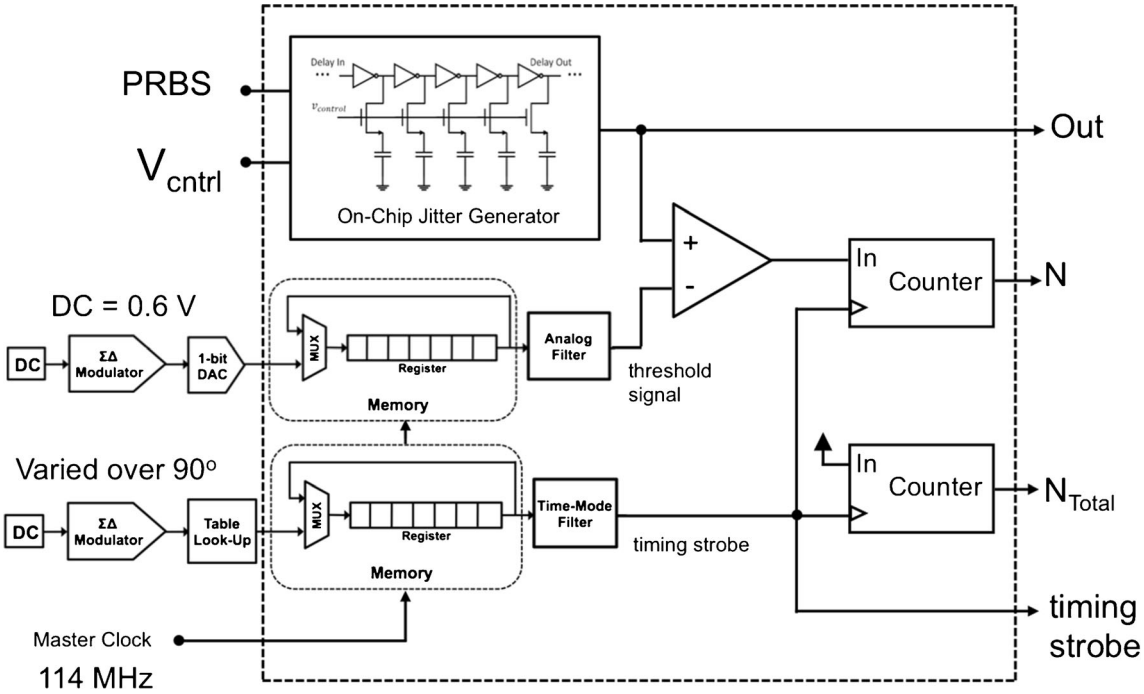

Fig. 20 Block diagram of the experimental CMOS chip and the external signal sources. Note that an on-chip jitter generation circuit is included on the IC to act as an on-chip DUT

high. By lining up these two bits, one can deduce the start of the count value beginning with the MSB.

As the timing strobe is moved across the DUT eye-diagram, the edge locations of the DUT output signal can be accurately determined. Figure 22 illustrates the extracted CDF (dashed green line) corresponding to the DUT output signal when subjected to a series of different timing strobe locations varied across 90 degrees. Mathematically, the PDF corresponding to this signal can be computed by taking the derivative of the CDF signal, resulting in the solid blue line in the plot of Fig. 22. It is important to note that this PDF is an ideal best-fit curve derived from the 4-point CDF and not the actually PDF, as this is not known.

This same measurement was made using an Agilent 9000B oscilloscope, which is capable of displaying a histogram or PDF of a random signal. These results are superimposed on the plot shown in Fig. 22 as a dotted red line. While the signal paths to each measuring instrument are slightly different, i.e., additional buffers are included to drive off-chip signals, the results show similar behavior (same shape), albeit with the on-chip PEU

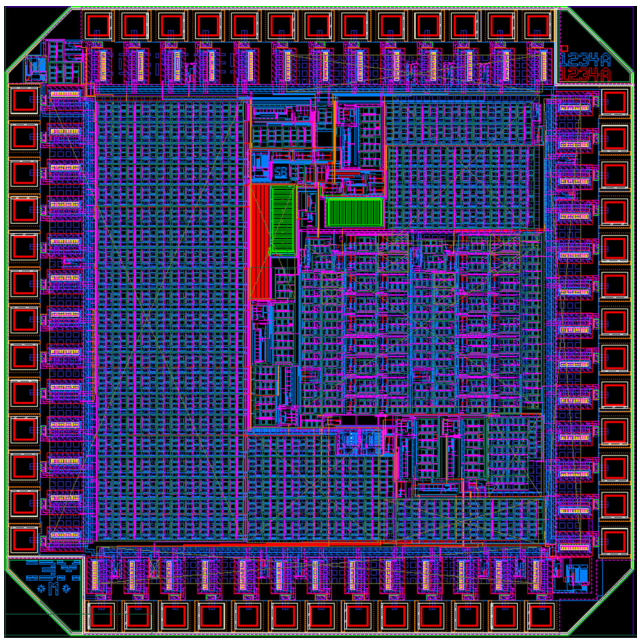

Fig. 21 Screen capture of the Cadence layout of the PEU implemented in a 130 nm CMOS process. The active area of the PEU is 0.24 mm^2

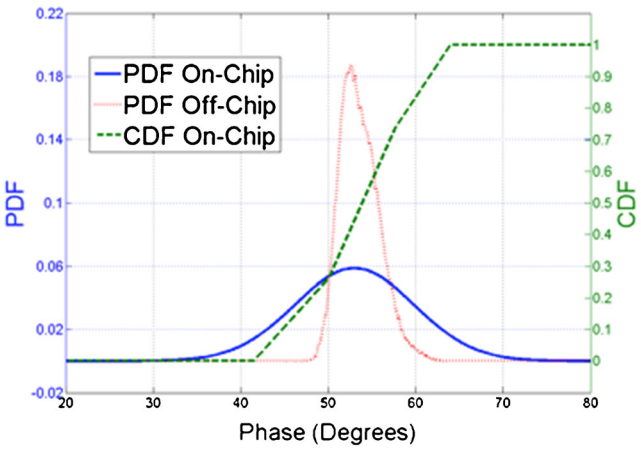

Fig. 22 A comparison of the measured on-chip PDF and the PDF captured by an external high-performance oscilloscope. Also shown is the on-chip measured CDF

having about twice the RMS noise variation (specifically, the on-chip noise standard deviation was found to be 5.4 degrees or equivalently 524 ps and the off-chip noise variation was about 226 ps). The extra noise suggests the PEU is slightly noisier than the high-performance oscilloscope. The exact reason for this error is yet to be determined. One possible reason may be that the comparator is noisier than that which was first thought. Nonetheless, the results do confirm that the PEU is tracking the underlying CDF/PDF of the incoming signal with a 99.7 % confidence interval accuracy of ±1.5 ns. The signal resolution is much lower than 1 ns but on account of the comparator noise level is not usable below 1.5 ns.

7 Conclusion

A design and implementation of a probabilistic test instrument used for injecting and extracting timing information associated with many of todays' communication systems was proposed. With a simple change in software code we showed how we can change the sampling edge T_{STRB}, threshold voltage reference level V_{TH} and the edge of the data stimulant T_{Data} associated with some arbitrary input bit sequence using various $\Sigma\Delta$ encoding techniques. These signals were also shown to be able to extract the CDF/PDF of the DUT output. Two implementations were used to demonstrate the feasibility of the proposed approach. One involved a fully discrete implementation of the PTI and another involved the realization of a fully integrated PEU in a 130 nm CMOS process. While the performance of the discrete implementation showed excellent correlation with the bench set-up, the CMOS implementation suffered higher than expected noise levels. A result that we believe is related to the performance of the on-chip comparator. Future implementations will pay closer attention to the design of the CMOS comparator.

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