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Editorial

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This issue contains ten papers and a *letter*. Topics covered are timing analysis, mixed-signal circuit testing, diagnosis, power constrained testing, reliability and security. Third, sixth and seventh papers are detailed versions of earlier presentations at the *Twenty-second Asian Test Symposium* held at Yilan, Taiwan during November 18–21, 2013. We are thankful to Professor Jiun-Lang Huang, guest editor, for completing *JETTA*'s peer review process for these papers. The fourth paper is from the *Fourteenth IEEE Latin-American Test Workshop* held at Cordoba, Argentina during April 2–5, 2013 and for it we appreciate the guest editing by Professor Leticia Bolzani Poehls.

In the first paper, Bhatnagar and Garg from STMicroelectronics, Greater Noida, India, reexamine the accuracy of the static timing analysis (STA). They emphasize the fact that the delay of a logic gate is strongly influenced by the slope of the input signal. The paper proposes modifications to STA with demonstrated improvements.

Next two papers discuss analog circuit testing. Xie from Hunan University of Science and Technology, Xiangtan, China and He from Hefei University of Technology, China, determine *fault eigenvectors* from voltage and current measurements of analog circuits. They show that these fault eigenvectors provide improved fault diagnosis compared to several previously used methods.

Hsiao, Wang and Chatterjee from Georgia Institute of Technology, Atlanta, Georgia, USA, propose the use of a built-in analog sensor to monitor the performance of a phased-locked loop (PLL).

Fault diagnosis is the topic of the next two papers. Gómez, Cook and Wunderlich from University of Stuttgart, Stuttgart, Germany and Indlekofer and Hellebrand from University of Paderborn, Paderborn, Germany, address the problem of diagnosing intermittent faults. They show that by combining their Bayesian classification technique with the conventional procedure of repeated tests they can identify such faults with more than 98 % probability.

Sun, Bosio, Dilillo, Girard, Pravossoudovich and Virazel from Université Montpellier II, Montpellier, France and Auvray from ST Microelectronic, Grenoble, France, focus on identifying faults that might lie inside standard cells. Their effect-cause procedure conducts critical path tracing (CPT) through a cell after a fault associated with an interconnect of that cell has been found to be a suspect.

Power constrained testing is discussed in next two papers. Eggersglüβ from University of Bremen, Bremen, Germany, proposes a method of filling don't cares (X) in compact testing with the objective of reducing power with minimal increase in test length. The focus is on reducing the switching activity during launch cycles of scan test.

Millican and Saluja from University of Wisconsin-Madison, Madison, Wisconsin, USA, consider the problem of controlling the power consumption of a system-on-chip (SoC) device when several cores on it are tested in parallel to reduce the test time. The authors examine the use of dynamic voltage and frequency scaling (DVFS) in the session-based as well as in session-less test scheduling.

Next three papers focus on reliability and security issues. Cortez, Roelofs and Hamdioui from Delft University of Technology, Delft, The Netherlands and Di Natale from Universit'e Montpellier II, Montpellier, France, discuss challenges of testing a physical unclonable function (PUF) and its secure key extraction mechanism.

The paper by Pahlevanzadeh and Yu from University of New Hampshire, Durham, New Hampshire, USA, analyzes the single event upset (SEU) of a circuit where the error effect

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may last longer than a clock cycle because of very high speed clock.

Zordan, Bosio, Dilillo, Girard and Virazel from Université Montpellier II, Montpellier, France and Badereddine from Intel Mobile Communications, Sophia Antipolis, France, provide solutions for problems of testing and fault tolerance of the power gating mechanism of a low power static random access memory (SRAM).

A *JETTA Letter* is contributed by Wang, Guo, Tian and Liu, University of Electronic Science and Technology of China, Chengdu, Sichuan, China. They propose a time domain method for error measurement and calibration of an analog-to-digital converter (ADC) circuit.