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Editorial

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My editorial in February of this year mentions Helen of Troy while introducing the origin of the term "Trojan" that was featured in articles on security appearing in that issue. Troy was situated near the modern day Turkey and the story took place in the Bronze Age (13th or 12th century BC). Fast forward many centuries through time and we find ourselves in the Byzantine Empire. In 555 AD, Justinian the Great ruled over this enormous region. To defend the Empire he had distributed armies commanded by generals, some loyal and some not so loyal owing to their own personal ambitions. We don't know how exactly Justinian managed his armies, but solutions for the so-called Byzantine Generals' Problem can be found in a 1982 paper:

> Leslie Lamport, Robert Shostak and Marshall Pease, "The Byzantine Generals Problem," *ACM Transactions on Programming Languages and Systems*, Vol. 4, No. 3, pp. 382–401, July 1982.

Consider armies, each under the command of a general, deployed at several fronts against a common enemy. A supreme commander sends an order, possibly "attack" or "retreat" that all generals must carry out correctly for the success of the campaign. The order is conveyed through messengers who can be unreliable. Besides, the generals receiving the order can be malicious or disloyal. The above paper shows that the problem is solvable if and only if more than two-thirds of generals are loyal. It considers several other scenarios and provides solutions. The real objective of solving the modern day Byzantine Generals' Problem is to build fault tolerant systems of networked computers, where some computers and communication links can be faulty. Expanding sizes of digital systems and shrinking device geometries are rejuvenating relevance of fault tolerance. Readers will find the cited reference interesting. For his work on distributed and concurrent systems and other contributions, Leslie Lamport received the 2013 Alan M. Turing Award of the ACM.

The first four papers of this issue discuss topics related to fault tolerance. There are three other papers and a *letter*. Topics covered are fault tolerance against various effects like crosstalk, NBTI and SEU, error correcting codes, analog circuit diagnosis, test programming and microprocessor test.

Authors, Maheswari of J. J. College of Engineering and Technology, Tiruchirappalli, India and Seetharaman of Oxford Engineering College, Tiruchirappalli, India, consider errors due to crosstalk. Their crosstalk avoidance code (CAC) recognizes the fact that the error is maximum when coupled interconnects have opposite signal transitions.

Tran, Virazel, Bosio, Dilillo, Girard and Pravossoudovich from LIRMM, France use a hybrid of redundancy approaches. In addition to signal redundancy they employ temporal redundancy for soft error correction and hardware redundancy for tolerance against permanent faults.

The next paper analyzes two aspects of NBTI, referred to as interface trap and oxide trap. NBTI, or negative bias temperature instability, affects the reliability of semiconductor devices over long term usage. This work throws new light on the understanding of the degradation phenomenon. Authors are Tahanout, Tahi, Djezzar, Benabdelmomene, Goudjil and Nadji from Université M'hamed Bougara de Boumerdès, Algeria.

Ullah and Sterpone from Politecnico di Torino, Italy examine the triple modular redundancy (TMR) used to protect an SRAM-based FPGA from single event upsets (SEU) where periodic write-back prevents accumulation of errors. Their design addresses concerns regarding the write-back time penalty and the multiple error problem of TMR.

Analog circuit test is the topic of the fifth paper authored by El-Gamal, Hassan and Ibrahim of Cairo

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University, Giza, Egypt. Using a simulation before test methodology they pose the fault diagnosis problem as a convex program for which mathematical solutions can be found. The results demonstrate that with reasonable computational effort more fault classes can be diagnosed than is possible with other methods.

The sixth paper is authored by Vock of Infineon Technologies AG, Neubiberg, Germany, and Escalona, Turner and Owens from University of Ulster, United Kingdom. They demonstrate the benefits of applying software engineering concepts to test programming.

Microprocessor test is featured in the next paper by Di Carlo, Gaudesi, Sanchez and Sonza Reorda from Politecnico di Torino, Italy. They test the instruction reorder buffer (ROB) of a superscalar processor that may execute instructions in an out of order sequence. Recognizing that an ROB does not have an easy test access, the authors devise a program that when executed by the processor tests the ROB.

A *JETTA Letter* is contributed by Li, Huang and Wang from Mechanical Engineering College, Shijiazhuang, China. They give a method to derive the nodal admittance matrix for a linear analog circuit that is embedded within a larger network.