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EDITORIAL

Guest Editorial: Special Issue on the 2015 International Conference on Embedded Computer Systems—Architectures, Modeling and Simulation (SAMOS XV)

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This special issue of IJPP presents extended journal versions of the best seven papers from the 2015 IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XV). SAMOS XV was held July 20–23, 2015 in Agios Konstantinos on the island of Samos, Greece. SAMOS is a unique event on embedded computing systems. Every year it brings together researchers from industry and academia in the quiet and relaxing atmosphere of the Mediterranean sea. During four days, formal and intensive technical sessions and lively panels are held in the mornings. Afternoons and evenings are reserved for enjoying informal discussions, good Mediterranean food and the inspiring landscapes of Samos island.

In 2015, 29 high-quality papers were selected out of 62 submissions for presentation at the conference. Out of those 29 papers presented at SAMOS XV, the best seven have been selected for this Special Issue. The authors of these papers have been invited to extend their original conference publication guided by a two-round review process.

Traditionally, the SAMOS conference includes two tracks. The *Applications, Systems, Architectures, and Processors* (ASAP) track is focused on novel architectures and computing methodologies for improving performance, energy or power efficiency, reliability, or dependability of embedded systems. From this track, the following five papers were selected:

- In '3D-stacked Many-Core Architecture for Biological Sequence Analysis Problems', Pei Liu et al. propose the use of many-core and 3D-stacked technologies for

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the computation of biological sequence analysis problems. The proposed architecture is evaluated in terms of throughput and efficiency using different test applications and datasets, and it is compared against alternative FPGA accelerators and GPGPU platforms.

- In 'Generating ASIPs with Reduced Number of Connections to the Register-file', Yosi Ben Asher et al. present a new framework to automatically synthesize application specific instruction set processors (ASIPs). The focus of this paper is on finding a pipeline configuration and a multi-op ISA that maximizes the instructions per cycles (IPC), while minimizing the resource usage and the cost of interconnections to the register-file of the resulting ASIP. For a given set of code kernels, the resulting ASIP obtains higher IPC values than an equivalent compilation to an ARM CPU.
- In 'LACross: Learning-based Analytical Cross-Platform Performance and Power Prediction', Xinnian Zheng et al. present a machine learning-based technique to predict the time-varying performance and power consumption of a benchmark on a target platform from hardware counter statistics obtained while running natively on a different host platform. The results show that the proposed technique can achieve on average over 97% performance and power prediction accuracy at simulation speeds of over 500 MIPS.
- In 'GPU Parallelization of HEVC In-loop Filters', Biao Wang et al. present a novel strategy to increase the amount of parallelism and the resulting performance of the HEVC in-loop filters on GPU devices by performing the HEVC filtering at frame-level and employing intrinsic GPU vector instructions. Implementation results on two embedded NVIDIA GPUs show a significant improvement in decoding performance.
- In 'Runtime Vectorization Transformations of Binary Code', Nabil Hallou et al. present a binary-to-binary optimization framework where loops vectorized for an older version of a processor's SIMD extensions are automatically converted to a newer one. For this purpose, a lightweight profiling to detect frequently executed sections of code is used. This paper also addresses runtime mechanism for vectorizing loops in binary codes that were not originally vectorized.

The *Modeling, Design, and Design Space Exploration* (MDSE) track is focused all aspects of embedded system design processes ranging from system-level specification, modeling, languages, simulation, estimation, analysis and exploration all the way down to hardware/software and system synthesis and compilation strategies. From this track, the following two papers were selected:

- In 'DRAMSpec: A High-Level DRAM Timing, Power and Area Exploration Tool', Christian Weiss et al. introduce a novel tool and a methodology for modeling and evaluating DRAM architectures to compare various tradeoffs in DRAM design. Their approach is based on an abstract model at the level of banks, controllers and DRAM chips that does not require circuit-level details. The proposed model is integrated into the GEM5 full-system simulator, and the final tool is demonstrated for application-specific exploration and optimization of individual DRAM parameters and complete 3D-stacked hybrid memory cube (HMC) architectures.

- In 'Towards Parallelism Extraction for Heterogeneous Multicore Android Devices', Miguel Angel Aguilar et al. propose an approach for automated parallelization of native C code within Android applications targeting performance optimization on heterogeneous multi-processor/multi-core system-on-chip (MPSoC) devices. The presented method combines static analysis with trace-based profiling to extract task-, data-, and pipeline-level parallelism and generate parallel code for different (parallel C, OpenMP and OpenCL) backends. Several experiments on a Nexus 7 Android tablet are conducted to demonstrate the speedups of the proposed auto-parallelizer, including comparisons to manually parallelized code.

Since its inauguration, SAMOS has been acclaimed for not only its relaxed Island location, but also due to the high quality of the material presented and the information and ideas exchanged at the conference. The seven papers included in this Special Issue represent the best of those from SAMOS XV, covering a diverse range of topics spanning from embedded processor and system architectures, over software optimization to high-level performance and power estimation. We hope that you will enjoy reading this Special Issue, and we would like to thank all reviewers that supported the SAMOS XV Conference, in particularly those who continued to participate diligently in the review process for extended papers in this journal.

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