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EDITORIAL

Parallel and Distributed Processing with Applications: Preface

Jesus Carretero · Laurence T. Yang

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1 Introduction

This special issue provides a forum for presenting the latest research on algorithms and applications for parallel and distributed systems, including algorithm design and optimization, programming paradigms, algorithm design and programming techniques heterogeneous computing systems, tools and environment for parallel/distributed software development, petascale and exascale algorithms, novel parallel and distributed applications, and performance simulations, measurement, and evaluations. The success of parallel algorithms-even on problems that at first glance seem inherently serial-suggests that this style of programming will be the inherent to any application in a near future. The relevant research has gained momentum with multicore and many-core architectures, and with the expected arrival of exascale computing. As a result, the space of potential ideas and solutions is still far from being widely explored.

This special issue of International Journal of Parallel Programming contains 7 papers selected from a set of invited papers extracted from the papers presented in The 10th IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA 2012), held in Madrid, Spain, July 10–13, 2012 [1]. ISPA 2012 accepted 32 papers out of 98 full paper submissions covering both foundational and practical issues in parallel and distributed programming and systems.

The objective of ISPA 2012 was to provide a forum for scientists and engineers in academia and industry to exchange and discuss their experiences, new ideas,

J. Carretero (✉)
Computer Science and Engineering Department, University Carlos III of Madrid, Leganés, Spain
e-mail: jesus.carretero@uc3m.es

L. T. Yang
Department of Computer Science, St. Francis Xavier University, Antigonish, Canada
e-mail: ltyang@stfx.ca

research results, and applications about all aspects of parallel and distributed computing and networking. It featured session presentations, workshops, tutorials and keynote speeches. ISPA-12 was sponsored by IEEE Technical Committee on Scalable Computing (TCSC) and IEEE Computer Society.

2 Special Issue Contents

For this special issue, we invited 14 selected papers from ISPA 2012 conference to submit extended versions to IJPP. All of them accepted and made paper submission to the journal. All paper were peer to peer reviewed following the review procedures on the IJPP journal. From them 7 were accepted, 3 in the fist round of the review, and the other 4 were asked for a new revised submission. After the second round of reviews, the 7 papers were accepted. A small introduction to the papers is shown below.

In the paper *Empirical Installation of Linear Algebra Shared-Memory Subroutines for Auto-Tuning*, the authors analyzes the introduction of auto-tuning techniques in linear algebra shared-memory routines to reduce the total execution time, by using routines at different levels (matrix multiplication, LU and Cholesky factorizations and linear systems symmetric or general routines) and with calls to routines in the LAPACK and PLASMA libraries with multithread implementations.

The paper *Bandwidth Adaptive Cache Coherence Optimizations for Chip Multiprocessors* presents two mechanisms to design efficient and scalable cache coherence protocols for CMPs by using an adaptive hybrid protocol to reduce coherence misses observed in write-invalidate based protocols pushing updates to potential consumers based on observed producer-consumer sharing patterns. The protocol is then extended with an interconnection resource aware mechanism.

In the paper *Improved Dynamic Communication for Parallel Sorting on Multicores*, the authors propose an improved Dynamic Communication Parallel Sorting (DCPS) algorithm to reduce the respond time of sorting on multicores for coarse- and medium-grain parallel computing and to improve both high-level communication and low-level communication.

In *Improving Performance of HDF5 Datasets on Multi-core Nodes Using L2 Cache Optimizations* the authors use the TAU toolkit for performance feedback to analyze and recommend methods for effective scheduling of threads on multi-core nodes to augment the performance of scientific applications processing HDF5 data, showing the benefits that can be achieved by using L2 Cache Affinity based and L2 Balanced-Set scheduling algorithms for improving L2 cache performance and effectively the overall execution time.

A Speculative Parallel DFA Membership Test for Multicore, SIMD and Cloud Computing Environments presents techniques to parallelize membership tests for Deterministic Finite Automata (DFAs). Our method searches arbitrary regular expressions by matching multiple bytes in parallel using speculation by exploiting structural DFA properties to minimize the speculative overhead.

Baumann and Resch presents in *Parallel Parameter Identification in Industrial Biotechnology* a comparison of several global as well as local optimization strategies applied to the task of efficiently identifying free parameters of a metabolic network

model. A focus is being set on the ease of adopting these strategies to modern, highly parallel architectures.

In *Parallel Training of An Improved Neural Network for Text Categorization*, an improved BPNN method to overcome the limitations of traditional BPNN is presented. It utilizes parallel computing to speed up the neural network training, so that the parallel improved BPNN together with SVD techniques achieve fast computational speed and high categorization correctness.

The set of accepted papers provide novelty approaches in parallel and distributed algorithms and applications, including optimization techniques for high-performance scientific and engineering computing.

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